IS62C25616EL, IS65C25616EL

256Kx16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

AUGUST 2018

KEY FEATURES

- High-speed access time: 45ns, 55ns
- CMOS low power operation
  - – Operating Current: 22 mA (max) at 85°C
  - – CMOS Standby Current: 5.0uA (typ) at 25°C
- TTL compatible interface levels
- Single 5V ± 10 % power supply
- Package : 44-pin TSOP (Type II)
- Three state outputs
- Commercial, Industrial and Automotive temperature support
- Lead-free available

DESCRIPTION

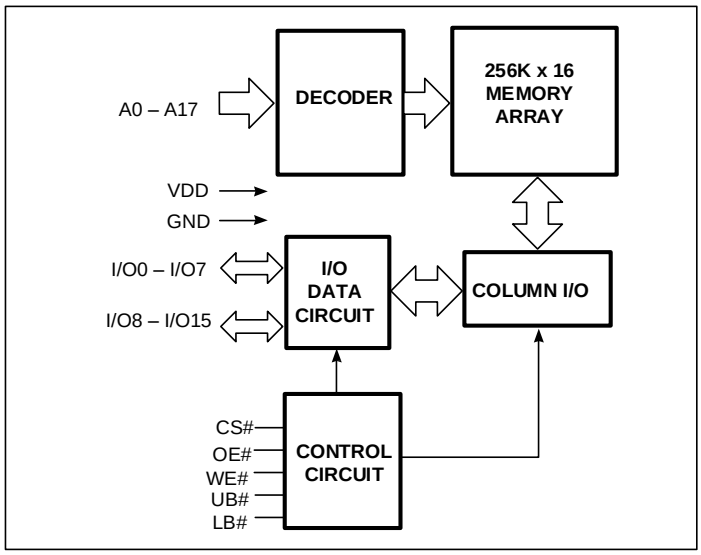
The *ISSI* IS62/65C25616EL are high-speed, low power, 4M bit static RAMs organized as 256K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology.

This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices. When CS# is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

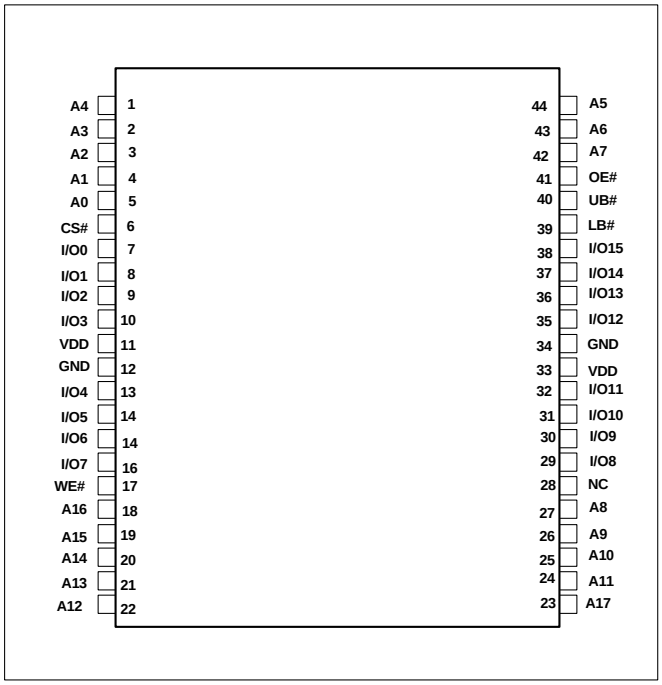
Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE#) controls both writing and reading of the memory. A data byte allows Upper Byte (UB#) and Lower Byte (LB#) access.

The IS62/65C25616EL are packaged in the JEDEC standard 44-Pin TSOP (TYPE II).

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS
44-Pin mini TSOP (Type II)



PIN DESCRIPTIONS

A0-A17	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CS#	Chip Enable Input
OE#	Output Enable Input
WE#	Write Enable Input
LB#	Lower-byte Control (I/O0-I/O7)
UB#	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V_{DD}	Power
GND	Ground

FUNCTION DESCRIPTION

SRAM is one of random access memories. Each byte or word has an address and can be accessed randomly. SRAM has three different modes supported. Each function is described below with Truth Table.

STANDBY MODE

Device enters standby mode when deselected (CS# HIGH). The input and output pins (I/O0-15) are placed in a high impedance state. The current consumption in this mode will be ISB2. CMOS input in this mode will maximize saving power.

WRITE MODE

Write operation issues with Chip selected (CS# LOW) and Write Enable (WE#) input LOW. The input and output pins (I/O0-15) are in data input mode. Output buffers are closed during this time even if OE# is LOW. UB# and LB# enables a byte write feature. By enabling LB# LOW, data from I/O pins (I/O0 through I/O7) are written into the location specified on the address pins. And with UB# being LOW, data from I/O pins (I/O8 through I/O15) are written into the location.

READ MODE

Read operation issues with Chip selected (CS# LOW) and Write Enable (WE#) input HIGH. When OE# is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted. UB# and LB# enables a byte read feature. By enabling LB# LOW, data from memory appears on I/O0-7. And with UB# being LOW, data from memory appears on I/O8-15.

In the READ mode, output buffers can be turned off by pulling OE# HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

TRUTH TABLE

Mode	CS#	WE#	OE#	LB#	UB#	I/O0-I/O7	I/O8-I/O15	VDD Current
Not Selected	H	X	X	X	X	High-Z	High-Z	ISB2
Output Disabled	L	H	H	X	X	High-Z	High-Z	ICC,ICC1
	L	H	L	H	H	High-Z	High-Z	
Read	L	H	L	L	H	DOUT	High-Z	ICC,ICC1
	L	H	L	H	L	High-Z	DOUT	
	L	H	L	L	L	DOUT	DOUT	
Write	L	L	X	L	H	DIN	High-Z	ICC,ICC1
	L	L	X	H	L	High-Z	DIN	
	L	L	X	L	L	DIN	DIN	

ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Vterm	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
tStg	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}(2)	DC Output Current (LOW)	20	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE(1)

Range	Ambient Temperature	VDD	Speed(ns)
Commercial	0°C to +70°C	5V ± 10 %	45
Industrial	-40°C to +85°C	5V ± 10 %	45
Automotive	-40°C to +125°C	5V ± 10 %	55

Note:

1. Full device AC operation assumes a 100 µs ramp time from 0 to VDDmin) and 200 µs wait time after VDD stabilization.

PIN CAPACITANCE (1)

Parameter	Symbol	Test Condition	Max	Units
Input capacitance	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DD}(typ)	6	pF
DQ capacitance (IO0–IO15)	$C_{I/O}$		8	pF

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

THERMAL CHARACTERISTICS (1)

Parameter	Symbol	Rating	Units
Thermal resistance from junction to ambient (airflow = 1m/s)	$R_{\theta JA}$	TBD	°C/W
Thermal resistance from junction to pins	$R_{\theta JB}$	TBD	°C/W
Thermal resistance from junction to case	$R_{\theta JC}$	TBD	°C/W

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

Parameter	Unit
Input Pulse Level	0V to 3.5V
Input Rise and Fall Time	3ns
Input and Output Timing and Reference Level	1.5V
R1	1838 Ω
R2	994Ω
V_{TM}	5V
Output Load Conditions	Refer to Figure 1 and 2

OUTPUT LOAD CONDITIONS FIGURES

FIGURE 1

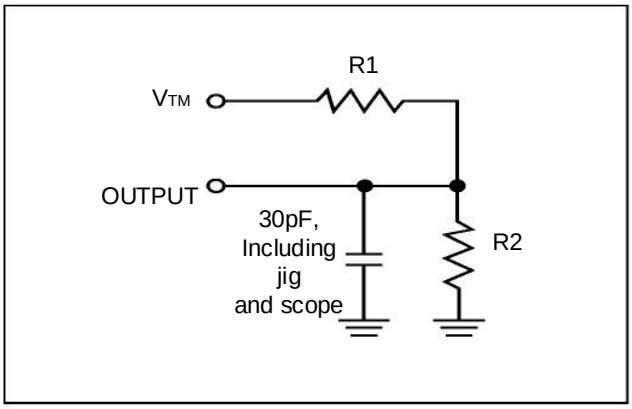
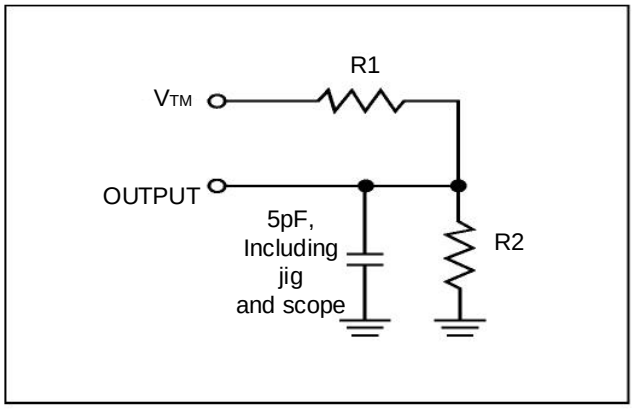


FIGURE 2



ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = -1.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 2.1 mA		—	0.4	V
V_{IH}(1)	Input HIGH Voltage			2.2	V_{DD} + 0.5	V
V_{IL}(1)	Input LOW Voltage			–0.3	0.8	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	Com.	–1	1	µA
			Ind.	-2	2	
			Auto.	-5	5	
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	Com.	–1	1	µA
			Ind.	-2	2	
			Auto.	-5	5	

Notes:
1. VILL(min) = -2.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 2.0V AC (pulse width < 10ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade		45/55ns		Unit
					Typ(1)	Max	
ICC	V_{DD} Dynamic Operating Supply Current	V_{DD} = V_{DD}(max), I_{OUT} = 0mA, f = f_{max}, CS# = V_{IL}	Com.		-	20	mA
			Ind.		-	22	
			Auto. A3		-	22	
ICC1	V_{DD} Static Operating Supply Current	V_{DD} = V_{DD}(max), I_{OUT} = 0mA, f = 0, CS# = V_{IL}	Com.		-	5	mA
			Ind.		-	5	
			Auto. A3		-	5	
ISB2	CMOS Standby Current (CMOS Inputs)	V_{DD} = V_{DD}(max), f = 0, CS# ≥ V_{DD} - 0.2V, VIN ≤ 0.2V or VIN ≥ V_{DD} - 0.2V	Com.	25°C	5.0	8(2)	µA
				40°C	-	9(2)	
				70°C	-	11	
			Ind.	85°C	-	16	
			Auto. A3	125°C	-	30	

Noes:
1. Typical value indicates the value for the center of distribution at V_{DD}=V_{DD} (Typ.), and not 100% tested.
2. Maximum value at 25°C, 40°C are guaranteed by design, and not 100% tested.

AC CHARACTERISTICS[6] (OVER OPERATING RANGE)

READ CYCLE AC CHARACTERISTICS

Parameter	Symbol	45ns		55ns		unit	notes
		Min	Max	Min	Max		
Read Cycle Time	tRC	45	-	55	-	ns	1,5
Address Access Time	tAA	-	45	-	55	ns	1
Output Hold Time	tOHA	10	-	10	-	ns	1
CS# Access Time	tACS	-	45	-	55	ns	1
OE# Access Time	tDOE	-	20	-	25	ns	1
OE# to High-Z Output	tHZOE	-	15	-	20	ns	2
OE# to Low-Z Output	tLZOE	5	-	5	-	ns	2
CS# to High-Z Output	tHZCS	-	15	-	15	ns	2
CS# to Low-Z Output	tLZCS	5	-	5	-	ns	2
LB#, UB# Access Time	tBA	45		55		ns	1,7
LB#, UB# to High-Z Output	tHZB	-	15	-	15	ns	2
LB#, UB# to Low-Z Output	tLZB	5	-	5	-	ns	2

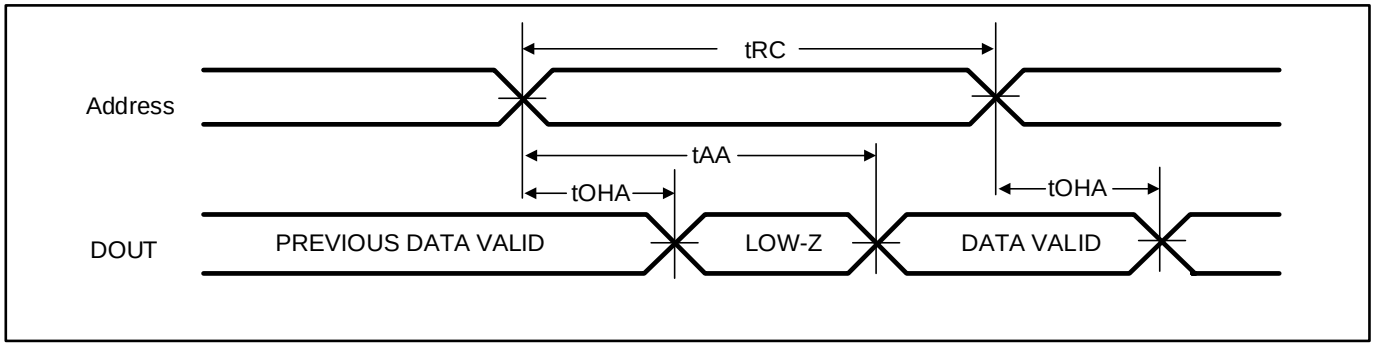
WRITE CYCLE AC CHARACTERISTICS

Parameter	Symbol	45ns		55ns		unit	notes
		Min	Max	Min	Max		
Write Cycle Time	tWC	45	-	55	-	ns	1,3,5
CS# to Write End	tSCS	35	-	35	-	ns	1,3
Address Setup Time to Write End	tAW	35	-	35	-	ns	1,3
Address Hold from Write End	tHA	0	-	0	-	ns	1,3
Address Setup Time	tSA	0	-	0	-	ns	1,3
LB#, /UB# Valid to End of Write	tPWB	35	-	35	-	ns	1,3
WE# Pulse Width	tPWE	35	-	35	-	ns	1,3,4
Data Setup to Write End	tSD	20	-	25	-	ns	1,3
Data Hold from Write End	tHD	0	-	0	-	ns	1,3
WE# LOW to High-Z Output	tHZWE	-	15	-	15	ns	2,3
WE# HIGH to Low-Z Output	tLZWE	5	-	5	-	ns	2,3

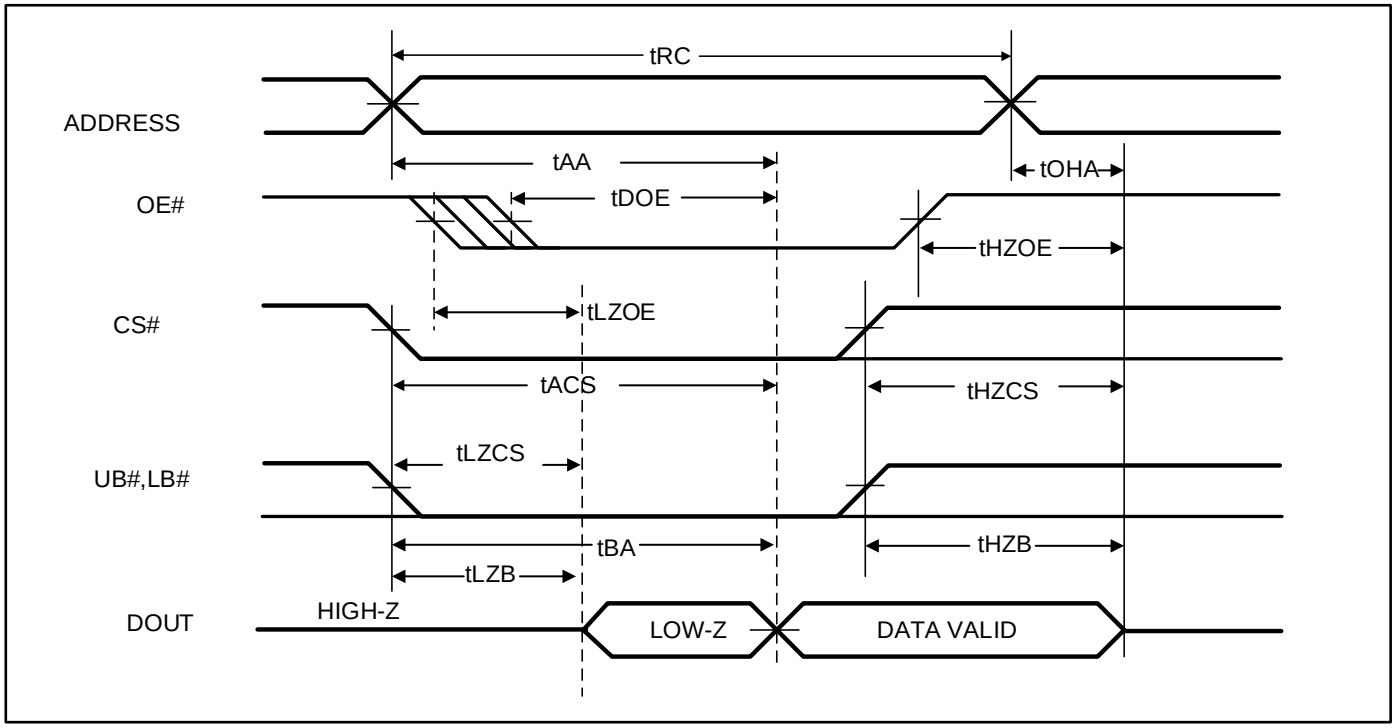
Notes:
1. Tested with the load in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. tHZOE, tHZCS, tHZB, and tHZWE transitions are measured when the output enters a high impedance state. Not 100% tested.
3. The internal write time is defined by the overlap of CS#=LOW, UB# or LB# =LOW, and WE#=LOW. All four conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. tPWE > tHZWE + tSD when OE# is LOW.
5. Address inputs must meet V_{IH} and V_{IL} SPEC during this period. Any glitch or unknown inputs are not permitted. Unknown input with standby mode is acceptable.
6. Data retention characteristics are defined later in DATA RETENTION CHARACTERISTICS.

TIMING DIAGRAM

READ CYCLE NO. 1[1] (ADDRESS CONTROLLED, CS# = OE# = UB# = LB# = LOW, WE# = HIGH)



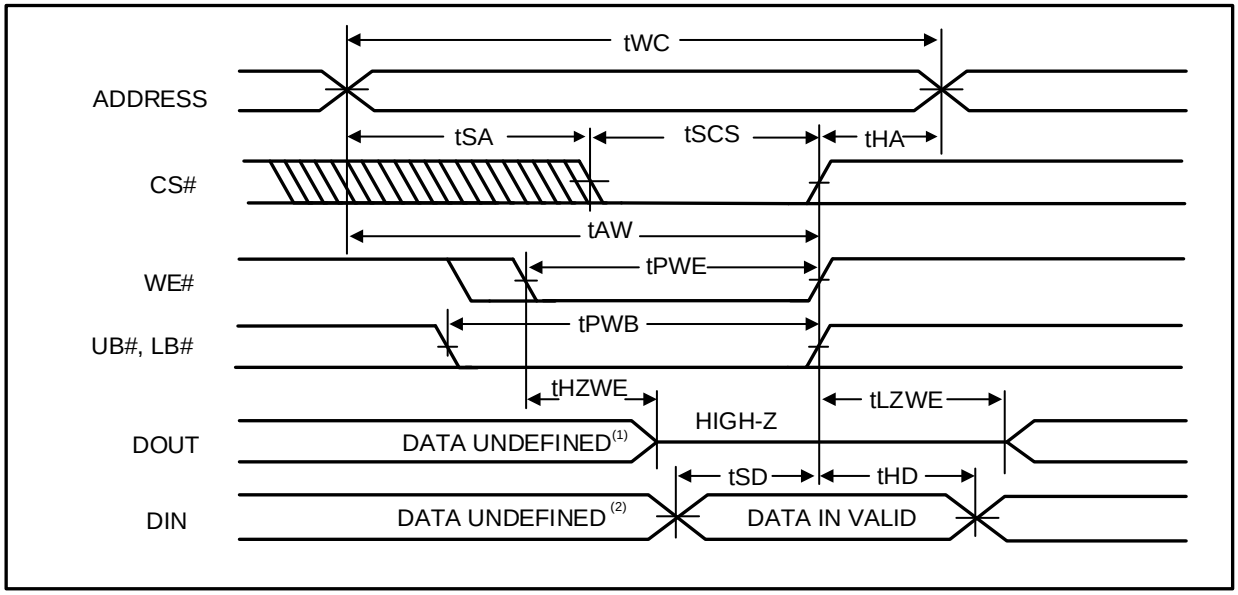
READ CYCLE NO. 2[1] (OE# CONTROLLED, WE# = HIGH)



Note:

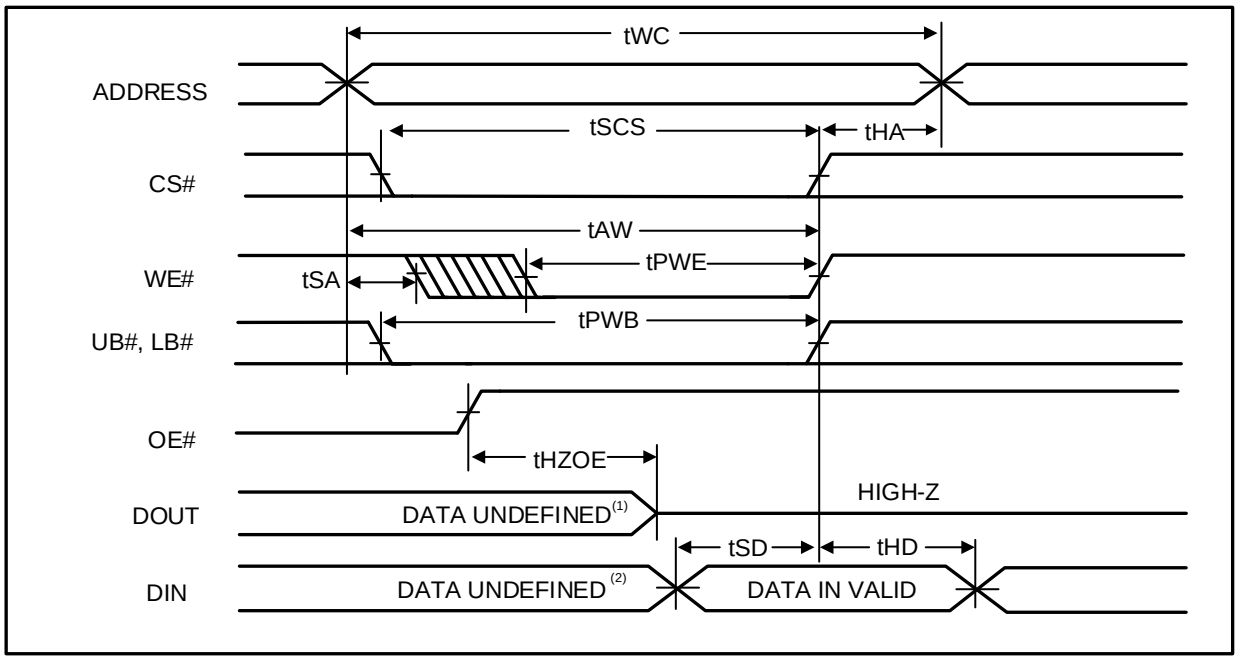
1. Address is valid prior to or coincident with CS# LOW transition.

WRITE CYCLE NO. 1[1, 2](CS# Controlled, OE# = HIGH or LOW)



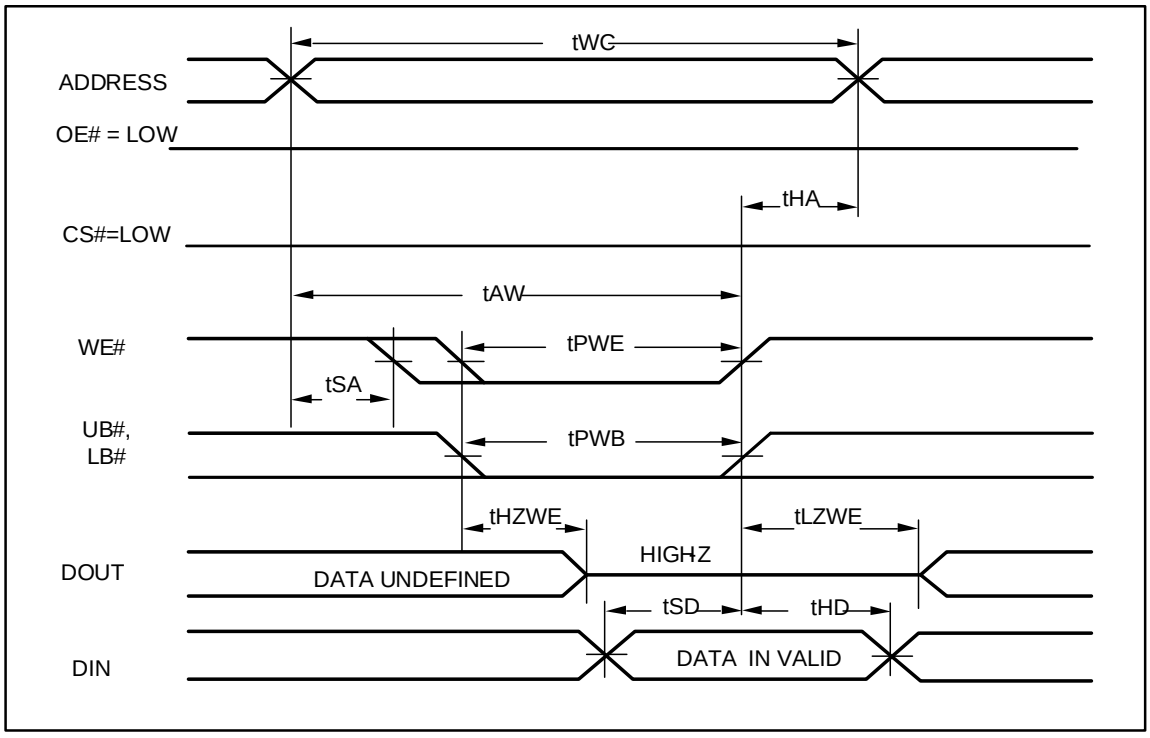
Notes:
1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if OE# goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 2[1,2](WE# CONTROLLED: OE# IS HIGH DURING WRITE CYCLE)



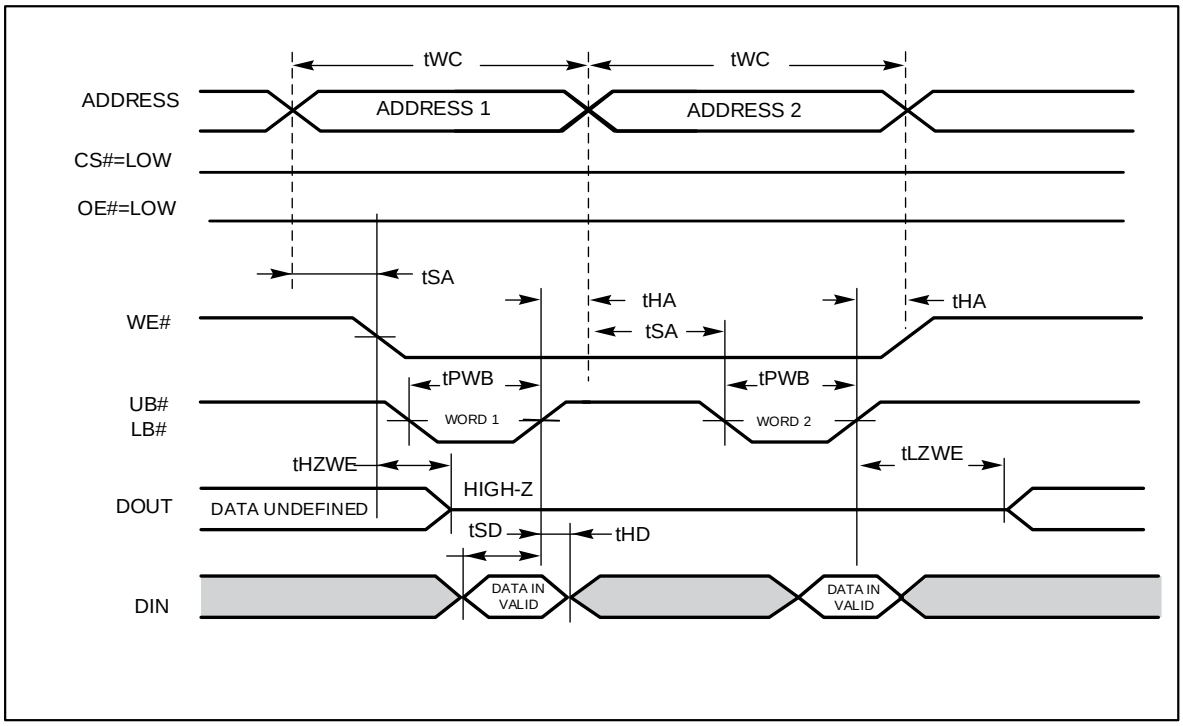
Notes:
1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if OE# goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 3(WE# CONTROLLED: OE# & CS# ARE LOW DURING WRITE CYCLE)



Note:
1. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

WRITE CYCLE NO. 4 (UB# & LB# Controlled)



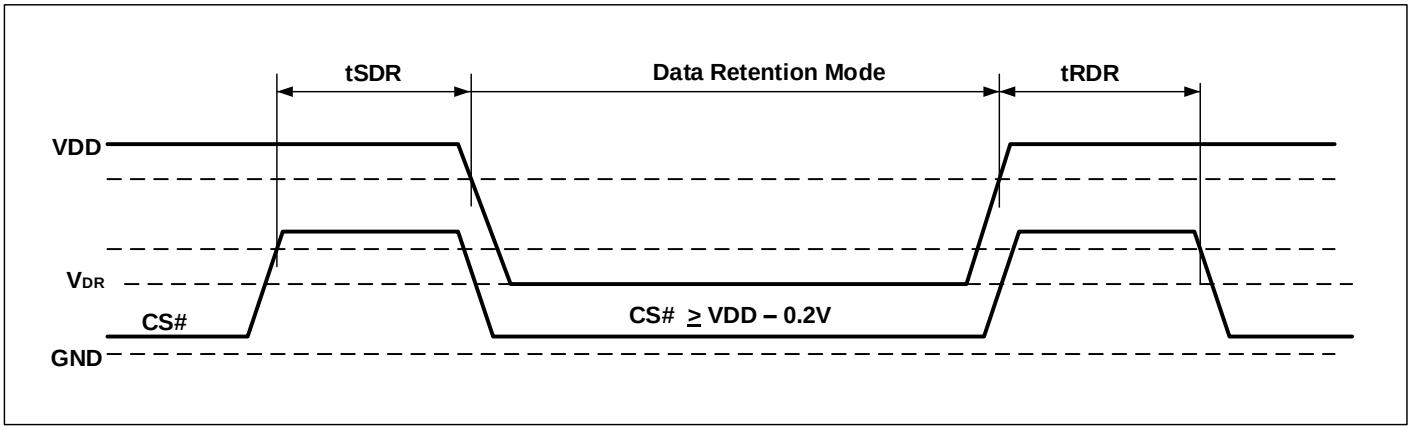
Notes:
1. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.
2. Due to the restriction of note1, OE# is recommended to be HIGH during write period.
3. Note WE# stays LOW in this example. If WE# toggles, tPWE and tHZWE must be considered.

DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition		Min	Typ (1)	Max	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0	-	-	V
I_{DR}	Data Retention Current	V_{DD}= V_{DR}(min), CS# ≥ V_{DD} – 0.2V or (LB# and UB#) ≥ V_{DD} - 0.2V, VIN ≤ 0.2V or VIN ≥ V_{DD} - 0.2V	25°C	-	5.0	8	uA
			85°C	-	-	16	
			125°C	-	-	30	
t_{SDR} (2)	Data Retention Setup Time	See Data Retention Waveform		-	-	-	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		tRC			ns

Notes:
1. Typical value indicates the value for the center of distribution at V_{DD} = V_{DR} (min.), and not 100% tested.
2. VDD power down slope must be longer than 100 us/volt when enter into Data Retention Mode.

DATA RETENTION WAVEFORM (CS# CONTROLLED)



ORDERING INFORMATION

IS62C25616EL

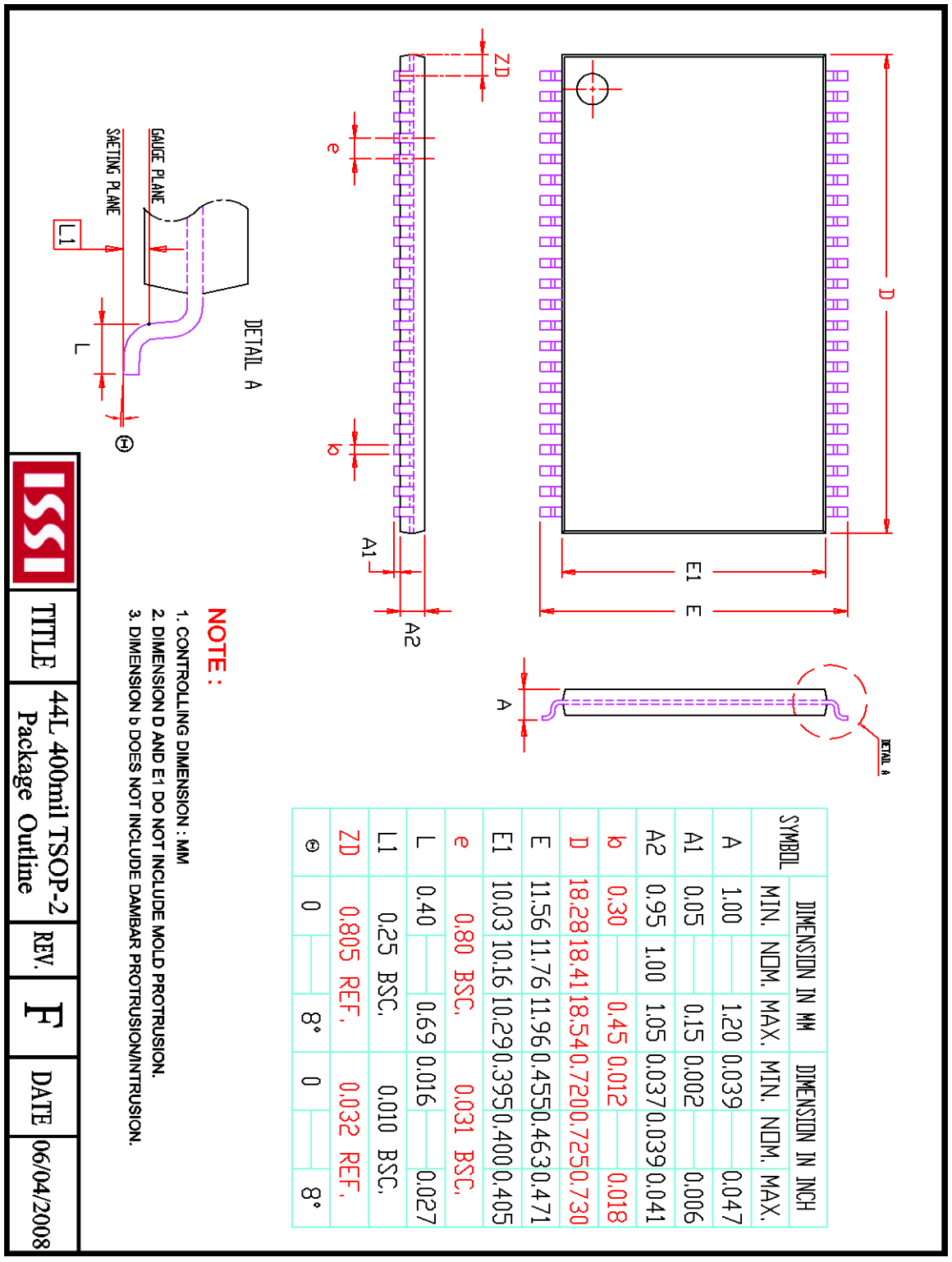
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62C25616EL-45TLI	44-pin TSP-II, Lead-free

Automotive Range (A3): –40°C to +125°C

Speed (ns)	Order Part No.	Package
55	IS65C25616EL-55CTLA3	44-pin TSOP-II, Lead-free, Copper Lead-frame

PACKAGE INFORMATION



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.45	0.012		0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e		0.80 BSC.			0.031 BSC.	
L	0.40		0.69	0.016		0.027
L1		0.25 BSC.			0.010 BSC.	
ZD		0.805 REF.			0.032 REF.	
θ	0		8°	0		8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

TITLE	44L 400mil TSOP-2 Package Outline	REV.	F	DATE 06/04/2008