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February 2008

74LVT245, 74LVTH245 Low Voltage Octal Bidirectional Transceiver with 3-STATE Inputs/Outputs

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH245), also available without bushold feature (74LVT245)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink, -32mA/+64mA
- Latch-up performance exceeds 500mA
- ESD performance:
 - Human-body model > 2000V
 - Machine model > 200V
 - Charged-device model > 100^r

General Description

The LVT245 and LVTH245 cordinates of non-inverting bidirectional buffers with ASI TE out uts and are intended for bus-orient applications, he Transmit/Receive (T/R) input determines the auton of claraflow through the bidirectional anscendent. Transmit (active-HIGH) enable data on arts to B ports; Receive (active-Livial V) tables at a from B ports to A ports. The Output Enable in the HIGH, disables both A and B ports of them in a HIGH. Z condition.

The section external pull-up resistors to hold unused input.

These transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V en ironment. The LVT245 and LVTH245 are fabricaled with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

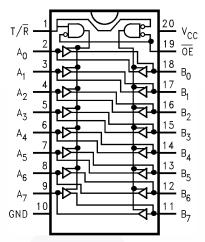
Orderin Inform ion

der I mber	Package Number	Package Description
74L róWM	M20L	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVT245SJ	iM2uD	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74L'(T245MSA	MS 4∠0	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
741.VT245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LVTH245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVTH245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVTH245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LVTH245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

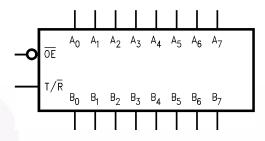
Connection Diagram

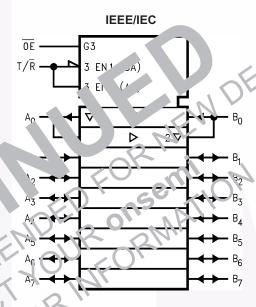


Pin Description

Pin Names	Description	
ŌĒ	Output Enable Input	
T/R	Transmit/Receive Input	
A ₀ -A ₇	Side A Inputs or 3-STATE Out	
B ₀ –B ₇	Side B Inputs or 3-ST/- 'tpu	

Logic Symbols





Truth Table

Inp	uts	
ŌĒ	T/R	Outputs
L	L	Bus B Data to Bus A
L	Н	Bus A Data to Bus B
Н	Х	HIGH-Z State

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V _{CC}	Supply Voltage	-0.5V to +4.6V
V _I	DC Input Voltage	–0.5V to +7.0V
Vo	DC Output Voltage	
	Output in 3-STATE	–0.5V to +7.0V
	Output in HIGH or LOW State ⁽¹⁾	-0.5V to +7.0V
I _{IK}	DC Input Diode Current, V _I < GND	_50mA
I _{OK}	DC Output Diode Current, V _O < GND	-50mA
Io	DC Output Current, V _O > V _{CC}	
	Output at HIGH State	64mA
	Output at LOW State	128mA
I _{CC}	DC Supply Current per Supply Pin	±64mA
I _{GND}	DC Ground Current per Ground Pin	±128mA
T _{STG}	Storage Temperature	-65° C tc →150° C

Note:

1. In Absolute Maximum Rating must be of a red.

Recommended Operation Corditions

The Recommended Ope one conditions are pecified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend excess git on or consigning to assolute maximum ratings.

Symb	Parariever	Min	Max	Units
	Signal oltage	2.7	3.6	V
VI	nput Voltage	0	5.5	V
IOH	HIGH Level Output Current		-32	mA
JL	LOV/-Leve! Output Current		64	mA
T _A	Free-Air Cperating 1 mperature	-40	85	°C
Δ+/ ΔV	Input Edge Rate, $V_{IN} = 0.8V-2.0V$, $V_{CC} = 3.0V$	0	10	ns/V

DC Electrical Characteristics

Symbol Parameter V _{CC} (V) Conditions Min. Max. Units					T _A = -40°C	C to +85°C	
Vi _H Input HIGH Voltage 2.7–3.6 V _O ≤ 0.1V or 2.0 V V _{II} Input LOW Voltage 2.7–3.6 V _O ≥ V _{CC} − 0.1V 0.8 V V _{OH} Output HIGH Voltage 2.7–3.6 I _{OH} = −100µA V _{CC} − 0.2 V I _{OH} = −32mA 2.4 3.0 I _{OH} = −32mA 2.0 V V _{OL} Output LOW Voltage 2.7 I _{OL} = 100µA 0.2 V I _{OL} = 24mA 5 3.0 I _{OL} = 32mA 0.5 0.5 I _{OL} = 32mA 0.5 0.5 0.5 0.5 0.5 I _{ICOD} = 24mA 0.5 0.5 0.5 0.5 0.5 0.5 I _I = 64mA 0.5 <td< th=""><th>Symbol</th><th>Parameter</th><th>V_{CC} (V)</th><th>Conditions</th><th>Min.</th><th>Max.</th><th>Units</th></td<>	Symbol	Parameter	V _{CC} (V)	Conditions	Min.	Max.	Units
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	V _{IK}	Input Clamp Diode Voltage	2.7	I _I = -18mA		-1.2	V
Voh	V _{IH}	Input HIGH Voltage	2.7–3.6	$V_O \le 0.1V$ or	2.0		V
2.7	V _{IL}	Input LOW Voltage	2.7–3.6	$V_O \ge V_{CC} - 0.1V$		0.8	
3.0 I _{OH} = -3zmA 2.0	V _{OH}	Output HIGH Voltage	2.7–3.6	$I_{OH} = -100 \mu A$	V _{CC} - 0.2		V
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			2.7	$I_{OH} = -8mA$	2.4		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			3.0	I _{OH} = -32mA	2.0		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	V _{OL}	Output LOW Voltage	2.7	$I_{OL} = 100 \mu A$		0.2	V
I _{OL} = 32mA 0.5 I _{OL} = 64mA 0.55 I _{OL} = 2 nV -75 I _{OL} = 3 nV -75 I _{OL} = 1 nV 1 nV I _{OL} =				I _{OL} = 24mA		5	
I _{I(HOLD)} (2) Bushold Input Minimum Drive 3.0 V _I = 0.8V D _I = 2 °V -75 D _I D _I			3.0	I _{OL} = 16mA			/S
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$				I _{OL} = 32mA		0.5	
I _{I(OD)} (2) Bushold Input Over-Drive, Current to Change State (3) 500 μA				I _{OL} = 64mA		0.55	
I _{I(OD)} (2) Bushold Input Over-Drive, Current to Change State 3.0 (2) 500 μA	I _{I(HOLD)} ⁽²⁾	Bushold Input Minimum Drive	3.0	V _I = 0.8V	.0		μΑ
Current to Change State (4) -500				V _I = 2 °V	-75		
$ \begin{array}{ c c c c c } \hline Current to Change State & (4) & -500 \\ \hline & I_1 & Input Current & 5.6 & V_1 = 5.7 & 10 & \mu A \\ \hline & Control Pins & 3.6 & = 0V \text{ or } V_{CC} & \pm 1 & 10 & \mu A \\ \hline & Data Pins & V_1 = 0V & -5 & 10 & \mu A \\ \hline & V_1 = 0V & -5 & 1 & 100 & \mu A \\ \hline & I_{DIF} & Power Off Leakane C & ent & 0 & 0V \leq V_{V} \text{ or } V_{O} \leq 5.5V & \pm 100 & \mu A \\ \hline & I_{PU/PD} & Power Up/D & vn, 3-STA. & 10 & nt & 0-1.5V & V_0 = 0.5V \text{ to } V_{CC} & \pm 100 & \mu A \\ \hline & I_{OZL} & 3 & \text{IATE Outp. } & \text{age Current} & 2.6 & V_0 = 0.5V & -5 & \mu A \\ \hline & I_{OZL}^{(2)} & 3-5 & \text{or } E \text{ O} & \text{but Leakage Current} & 3.6 & V_0 = 0.5V & -5 & \mu A \\ \hline & I_{OZL}^{(2)} & 3-5 & \text{or } E \text{ O} & \text{but Leakage Current} & 3.6 & V_0 = 3.6V & 5 & \mu A \\ \hline & I_{OZH}^{(2)} & 3-5 & \text{ATE Output Leakage Current} & 3.6 & V_0 = 3.6V & 5 & \mu A \\ \hline & I_{CCH} & Fover Supply Current & 3.6 & \text{Outputs HIGH} & 0.19 & \text{mA} \\ \hline & I_{CCH} & Fover Supply Current & 3.6 & \text{Outputs LOW} & 5 & \text{mA} \\ \hline & I_{CC2} & Power Supply Current & 3.6 & \text{Outputs Disabled} & 0.19 & \text{mA} \\ \hline & I_{CC2} & Power Supply Current & 3.6 & \text{Outputs Disabled} & 0.19 & \text{mA} \\ \hline & AI_{CC} & Increase in Power Supply Current & 3.6 & \text{One Input at } V_{CC} - 0.6V_{O} & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.19 & \text{mA} \\ \hline & Outputs Disabled & 0.19 & \text{mA} \\ \hline & Outputs Disabled & 0.19 & \text{mA} \\ \hline & Outputs Disabled & 0.19 & \text{mA} \\ \hline & Outputs Disabled & 0.19 & \text{mA} \\ \hline & Outputs Disabled & 0.19 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & \text{mA} \\ \hline & Outputs Disabled & 0.2 & $	I _{I(OD)} ⁽²⁾	Bushold Input Over-Drive,	3.0		500		μΑ
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		Current to Change State		(4)	-500		7
$\begin{array}{ c c c c c c }\hline Data Pins & V_1 = CV & -5 \\\hline V_1 = V_{CC} & 1 \\\hline \\ I_{DU/PD} & Power Off Leakage Curent & 0 & CV \leq V_1 \text{ or } V_{CC} \leq 5.5V & \pm 100 & \mu A \\\hline \\ I_{PU/PD} & Power Up/D & vn, 3-STA. & Curent & 0-1.5V & V_0 = 0.5V \text{ to } V_{CC} \\\hline \\ I_{OZL} & 3 & \text{IATE Outp. To age Current} & 2.6 & V_0 = 0.5V & -5 & \mu A \\\hline \\ I_{OZL} & 3-2 & C & \text{O but Leakage Current} & 3.6 & V_0 = 0.5V & -5 & \mu A \\\hline \\ I_{OZL} & 3-2 & C & \text{O but Leakage Current} & 3.6 & V_0 = 3.0V & -5 & \mu A \\\hline \\ I_{OZH} & 3-2 & \text{ATE Output Leakage Current} & 3.6 & V_0 = 3.6V & 5 & \mu A \\\hline \\ I_{OZH} & 3-2 & \text{ATE Output Leakage Current} & 3.6 & V_0 = 3.6V & 5 & \mu A \\\hline \\ I_{CH} & 3-2 & \text{Output Leakage Current} & 3.6 & \text{Outputs HIGH} & 0.19 & mA \\\hline \\ I_{CCH} & Fover Supply Current & 3.6 & \text{Outputs LOW} & 5 & mA \\\hline \\ I_{CCZ} & Power Supply Current & 3.6 & \text{Outputs Disabled} & 0.19 & mA \\\hline \\ I_{CCZ} & Power Supply Current & 3.6 & \text{Outputs Disabled} & 0.19 & mA \\\hline \\ I_{CCZ} & Power Supply Current & 3.6 & \text{One Input at } V_{CC} - 0.6V_{CC} & 0.2 & mA \\\hline \\ D_{CCCZ} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & Increase in Power Supply Current & 0.2 & mA \\\hline \\ D_{CCC} & D_{CCC} & D_{CCC} & D_{CCC} & D_{C$	I _I	Input Current	J.6	V _I = 5 /	250	10	μA
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		Control Pins	3.6	= 0V or V _{CC}	0, 1	±1	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		Data Pins		$V_1 = CV$	01/4	- 5	
$\begin{array}{ c c c c c c }\hline I_{PU/PD} & Power Up/D \ vn, 3-STA. \ Coront & U-15V \ V_O=0.5V \ to V_{CC} \\ \hline I_{OZL} & 3 \ \text{IATE Outp. 's age Current} & 2.6 \ V_O=0.5V \\ \hline I_{OZL}^{(2)} & 3-51 = 0 \ \text{out Leakage Current} & 3.6 \ V_O=0.0V \\ \hline I_{OZL}^{(2)} & 3-51 = 0 \ \text{out Leakage Current} & 3.6 \ V_O=3.0V \\ \hline I_{OZL}^{(2)} & 3-51 = 0 \ \text{output Leakage Current} & 3.6 \ V_O=3.0V \\ \hline I_{OZH}^{(2)} & 3-51 = 0 \ \text{output Leakage Current} & 3.6 \ V_O=3.6V \\ \hline I_{OZH}^{(2)} & 3-51 = 0 \ \text{output Leakage Current} & 3.6 \ V_O=3.6V \\ \hline I_{CCH} & Fover Supply Current & 3.6 \ Outputs HIGH \\ \hline I_{CCH} & Fover Supply Current & 3.6 \ Outputs LOW \\ \hline I_{CCC} & Power Supply Current & 3.6 \ Outputs Disabled \\ \hline I_{CCC} & Power Supply Current & 3.6 \ Outputs Disabled \\ \hline \Delta I_{CC} & Increase in Power Supply Current^{(5)} & 3.6 \ One Input at V_{CC} - 0.6V, Other Inputs at V_{CC} or \\ \hline \end{array}$				¥, ≠Vcc	.0	1	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	I _{OFF}	Power Off Leakage C ent	0	$0V \le V_i$ or $V_0 \le 5.5V$		±100	μA
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	I _{PU/PD}	Power Up/D vn, 3-STA. ^nt	0-1.5V	$V_{()} = 0.5 \text{V to } V_{CC}$		±100	μΑ
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$							
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	I _{OZL}	3 ATE Out 1 age Current		$V_0 = 0.5$ V		– 5	μA
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	I _{OZL} ⁽²⁾	3-5 □ O put Leakage Current	3.6	$V_D = 0.0V$		– 5	μΑ
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	JL.	ST. Jutput Leakinge Current	3.6	$V_0 = 3.0V$		5	μΑ
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	'2ZH ⁽²⁾	3- ATE Output Leakage Current	3.6	$V_0 = 3.6V$		5	μΑ
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		3-STATE Output Leakage Current	3.6	$V_{CC} < V_O \le 5.5V$		10	μΑ
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	ICCH	Folver Supply Current	3.6	Outputs HIGH	A	0.19	mA
Power Supply Current 3.6 $V_{CC} \le V_O \le 5.5V$, Outputs Disabled 0.19 mA ΔI_{CC} Increase in Power Supply Current ⁽⁵⁾ 3.6 One Input at $V_{CC} = 0.6V$, Other Inputs at V_{CC} or	Icci	Power Supply Current	3.6	Outputs LOW		5	mA
Outputs Disabled $\Delta I_{CC} \text{Increase in Power Supply Current}^{(5)} 3.6 \text{One Input at V}_{CC} - 0.6 \text{V}, \\ \text{Other Inputs at V}_{CC} \text{ or} 0.2 \text{mA}$	Iccz	Power Supply Current	3.6	Outputs Disabled		0.19	mA
Outputs Disabled ΔI_{CC} Increase in Power Supply Current ⁽⁵⁾ 3.6 One Input at $V_{CC} - 0.6V$, Other Inputs at V_{CC} or	CCZ+	Power Supply Current	3.6			0.19	mA
Other Inputs at V _{CC} or				Outputs Disabled			
	Δl _{CC}	Increase in Power Supply Current ⁽⁵⁾	3.6			0.2	mA

Notes

- 2. Applies to Bushold versions only (LVTH245).
- 3. An external driver must source at least the specified current to switch from LOW-to-HIGH.
- 4. An external driver must sink at least the specified current to switch from HIGH-to-LOW.
- 5. This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics⁽⁶⁾

		V _{CC}	Conditions	٦	$\Gamma_{A}=25^{\circ}$		
Symbol	Parameter	(V)	$C_L = 50 \text{ pF, } R_L = 500\Omega$	Min.	Тур.	Max.	Units
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	(7)		0.8		V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	(7)		-0.8		V

Notes:

- 6. Characterized in SOIC package. Guaranteed parameter, but not tested.
- 7. Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

		$T_A = -4^{\circ}C$ $C_L = 50 \text{ p.}$	t 3°C, R _L 50′ 2	N.	0
		$V_{CC} = 2 \ 3V - 3.3V$	V _{CC} =	2.79	
Symbol	Parameter	K M.	Milh.	Max.	Units
t _{PLH}	Propagation Delay	1.2 3.6	1.2	4.0	ns
t _{PHL}		2 3.5	1.2	4.0)\
t _{PZH}	Output Enable Time	1.5 5.5	1.3	7.1	ns
t _{PZL}		1.7 5.7	17	6.7	
t _{PHZ}	Output Disable	2.0 5.)	20	6.5	ns
t _{PLZ}		2.0 5.0	2.0	5.1	
t _{OSHL} , t _{OSLH}	Output Cipul 'rew(8)	1.0		1.0	ns

Note:

8. Skew is defined as the isolar value of the difference between the actual propagation delay for any two separation. The specification applies to any outputs switching in the same direction, either H. H-to-LOW occur) or LO V-to-HIGH (t. sc. u.).

C. aci ince⁽⁹⁾

Symbol	Farameter	Conditions	Typical	Units
Chr	Input Capacitance	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}	4	pF
COUT	Output Cape citance	$V_{CC} = 3.0V$, $V_{O} = 0V$ or V_{CC}	8	pF

Vote:

9. Capacitance is measured at frequency f = 1MHz, per MIL-STD-883, Method 3012.

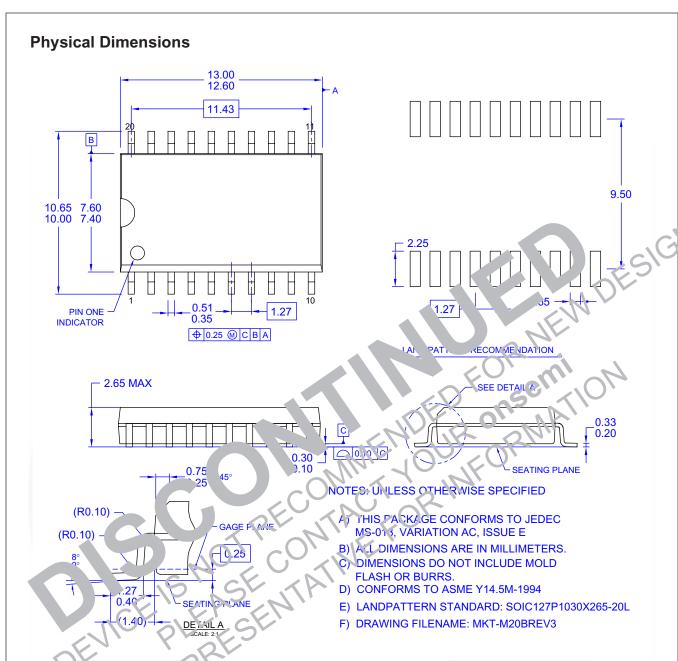


Figure 1. 20-Level Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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Physical Dimensions (Continued) 12.6±0.10 0.40 TYP -A-20 11 12 11 5.01 TYP 5.3±0.10 9.27 TYP 7.8 -B-3.9 △ 0.2 C B A ALL LEAD TIPS 10 PIN #1 IDENT. J.6 TYP 1.27 ALL LEAD TIPS △ 0.1 C 2.1 MAX. -C-0.15 - 0.250.35-0.51 1.27 TYP 7° TYP ARE IN MILLIMETER GAGE PLANE 0°-8° TYP CONFORMS TO LIAU EDG-7320 REGISTRATION ESTABLISHED IN DECEMBER, 1998. D.Y.L.NSIONS ARE EXCLUSIVE OF TURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. 0.60 ± 0.15 SEATING PLANE 1.25 -DETAIL A

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Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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M20DREVC

Physical Dimensions (Continued) 0.68 TYP В 9.12 5.58 5.3±0.30 7.8 10 3.9 △ 0.2 C A B PIN #1 IDENT. RECOMMENDATIONS △ 0.10 C ALL LEAD TIPS 1.75±0 2.0 MAX. 0.65 TYP 0.15M L GAGE PLANE NOTES 0.25 NFORMS TO JEDIC REGISTRATION ARIATION AC, LATE 1/94. DIMENSIONS ARE IN MILLINIZIERS. 0.75±0.2 DIMENSIONS ARE FACLUSIVE CF DURRS, MOLD FLASH, AND THE BAR EXTRUSIONS SEATING PLANE (1.25) CIMENSIONS AND TOLERAILC'S PER ASME Y14.5M - 1994. DETAIL A

Figure 3. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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SA20REVE

Physical Dimensions (Continued) 5.5±0.1 -A--0.20 وحا 4.16 6,4 4.4±0.1 -B-3,2 0.2 C B A 0.65 ALL LEAD PIN #1 IDENT. O.1 C -0.90 1.2 -C-0.09-0.20 0.05 0.65 -12.00° GAGE PLANE 0.25 SEATING PLANE CONFORMS TO JEDEC RESISTRATION MIL-133 REF NOTE 6, DATE 7/33. VARIATION AC, -0.6±0.1 R0.09min D'MENSIONS ARE IN MILLIMETERS. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS

MTC20REVD1

D. DIMENSIONS AND TO ERANCES PER ANSI Y14.5M, 1982.

Figure 4. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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DETAIL A





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