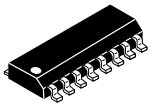
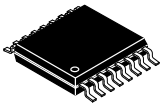
Dual J-K Flip-Flops with Preset and Clear

74VHC112



SOIC−16, 150 mils
CASE 751BG



TSSOP 16
CASE 948AH

General Description

The VHC112 is an advanced high speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high−speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

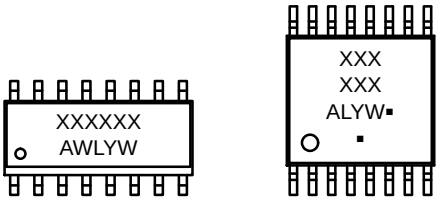
The VHC112 contains two independent, high−speed JK flip−flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to transition time. The J and K inputs can change when the clock is in either state without affecting the flip−flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. The LOW signal on PR or CLR prevents clocking and forces Q and $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on PR and CLR force both Q and $\overline{Q}$ HIGH.

An input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: f_{MAX} = 200 MHz (Typ.) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 2 μA (Max.) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is Provided on All Inputs
- Pin and Function Compatible with 74HC112
- These are Pb−Free Devices

MARKING DIAGRAM



SOIC−16 TSSOP 16

XXXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

Connection Diagram

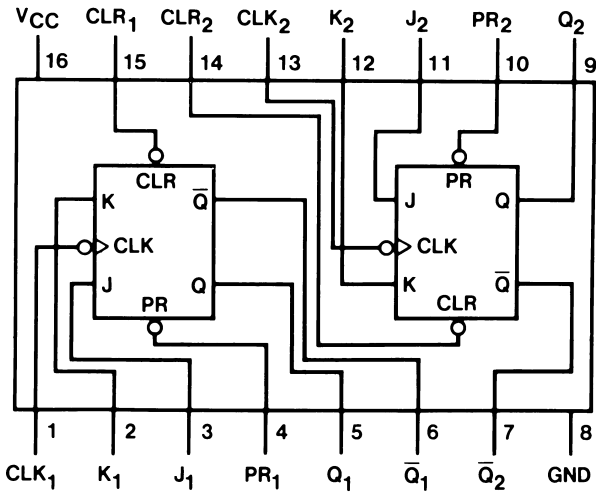


Figure 1. Connection Diagram

TRUTH TABLE

Input					Outputs	
PR	CLR	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	↘	h	h	$\overline{Q}_0$	Q_0
H	H	↘	l	h	L	H
H	H	↘	h	l	H	L
H	H	↘	l	l	Q_0	$\overline{Q}_0$

H (h) = HIGH Voltage Level
L (l) = LOW Voltage Level
X = Immaterial
↘ = HIGH−to−LOW Clock Transition
Q_0 ($\overline{Q}_0$) = Before HIGH−to−LOW Transition of Clock
Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH−to−LOW clock transition.

PIN DESCRIPTION

Pin Names	Description
J_1, J_2, K_1, K_2	Data Inputs
CLK_1, CLK_2	Clock Pulse Inputs (Active Falling Edge)
CLR_1, CLR_2	Direct Clear Inputs (Active LOW)
PR_1, PR_2	Direct Preset Inputs (Active LOW)
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs

Logic Diagram (One Half Shown)

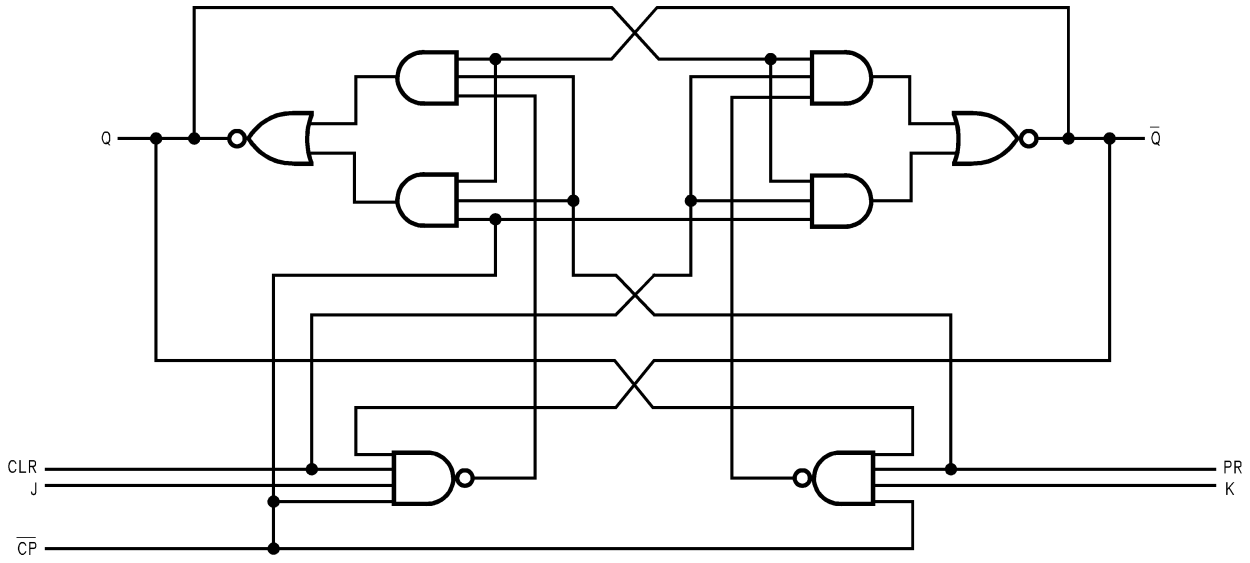


Figure 2. Logic Diagram (One Half Shown)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} + 0.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{IK}	Input Clamp Current		−20	mA
I_{OK}	Output Clamp Current		±20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC−16	126	°C/W
		TSSOP 16	159	
P_D	Power Dissipation in Still Air at 25°C	SOIC−16	995	mW
		TSSOP 16	787	
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.112 in	
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model	2000	V
		Charged Device Model	N/A	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage (Note 4)		0	5.5	V
V_{OUT}	DC Output Voltage (Note 4)		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 3.0 V to 3.6 V	0	100	ns/V
		V_{CC} = 4.5 V to 5.5 V	0	20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
					Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage			2.0	1.50	−	−	1.50	−	V
				3.0–5.5	0.7 x V_{CC}	−	−	0.7 x V_{CC}	−	
V_{IL}	LOW Level Input Voltage			2.0	−	−	0.50	−	0.50	V
				3.0–5.5	−	−	0.3 x V_{CC}	−	0.3 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –50 μA	2.0	1.9	2.0	−	1.9	−	V
				3.0	2.9	3.0	−	2.9	−	
				4.5	4.4	4.5	−	4.4	−	
			I_{OH} = –4 mA	3.0	2.58	−	−	2.48	−	
			I_{OH} = –8 mA	4.5	3.94	−	−	3.80	−	
V_{OL}	LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	−	0.0	0.1	−	0.1	V
				3.0	−	0.0	0.1	−	0.1	
				4.5	−	0.0	0.1	−	0.1	
			I_{OL} = 4 mA	3.0	−	−	0.36	−	0.44	
			I_{OL} = 8 mA	4.5	−	−	0.36	−	0.44	
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND		0–5.5	−	−	±0.1	−	±1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND		5.5	−	−	2.0	−	20.0	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	C_L = 15 pF	3.3 ±0.3	110	150	−	100	−	MHz
		C_L = 50 pF		90	120	−	80	−	
		C_L = 15 pF	5.0 ±0.5	150	200	−	135	−	MHz
		C_L = 50 pF		120	185	−	110	−	
t_{PLH}, t_{PHL}	Propagation Delay Time (CP to Q_n or $\overline{Q}_n$)	C_L = 15 pF	3.3 ±0.3	−	8.5	11.0	1.0	13.4	ns
		C_L = 50 pF		−	10.0	15.0	1.0	16.5	
		C_L = 15 pF	5.0 ±0.5	−	5.1	7.3	1.0	8.8	ns
		C_L = 50 pF		−	6.3	10.5	1.0	12.0	
t_{PLH}, t_{PHL}	Propagation Delay Time (PR or CLR to Q_n or $\overline{Q}_n$)	C_L = 15 pF	3.3 ±0.3	−	6.7	10.2	1.0	11.7	ns
		C_L = 50 pF		−	9.7	13.5	1.0	15.0	
		C_L = 15 pF	5.0 ±0.5	−	4.6	6.7	1.0	8.0	ns
		C_L = 50 pF		−	6.4	9.5	1.0	11.0	
C_{IN}	Input Capacitance	V_{CC} = Open		−	4	10	−	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)		−	18	−	−	−	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation:
I_{CC} (opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4$ (per F/F), and the total C_{PD} when n pcs of the Flip−Flop operate can be calculated by the following equation:
C_{PD} (total) = 30 + 14 · n

AC ELECTRICAL REQUIREMENTS

Symbol	Parameter	V_{CC} (V) (Note 6)	T_A = 25°C	T_A = −40°C to +85°C	Unit
			Typ	Guaranteed Minimum	
t_W	Minimum Pulse Width (CP or CLR or PR)	3.3	−	5.0	5.0	ns
		5.0	−	5.0	5.0	
t_S	Minimum Setup Time (J_n or K_n to CP_n)	3.3	−	5.0	5.0	ns
		5.0	−	4.0	4.0	
t_H	Minimum Hold Time (J_n or K_n to CP_n)	3.3	−	1.0	1.0	ns
		5.0	−	1.0	1.0	
t_{REC}	Minimum Recovery Time (CLR or PR to CP)	3.3	−	6.0	6.0	ns
		5.0	−	5.0	5.0	

6. V_{CC} is 3.3 ±0.3 V or 5.0 ±0.5 V.

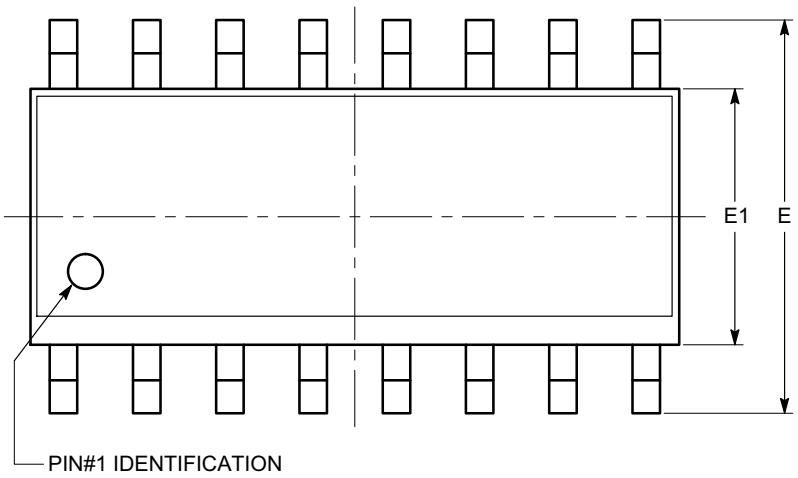
ORDERING INFORMATION

Device	Marking	Package	Shipping†
74VHC112MX	VHC112	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
74VHC112MTCX	VHC 112	TSSOP−16 (Pb−Free, Halide Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

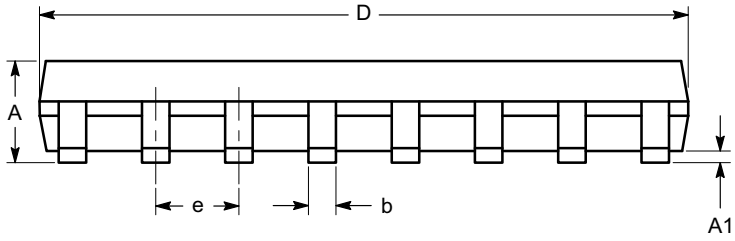
SOIC−16, 150 mils
CASE 751BG−01
ISSUE O

DATE 19 DEC 2008

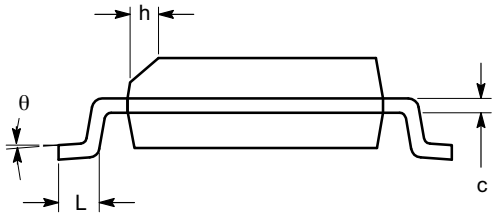


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

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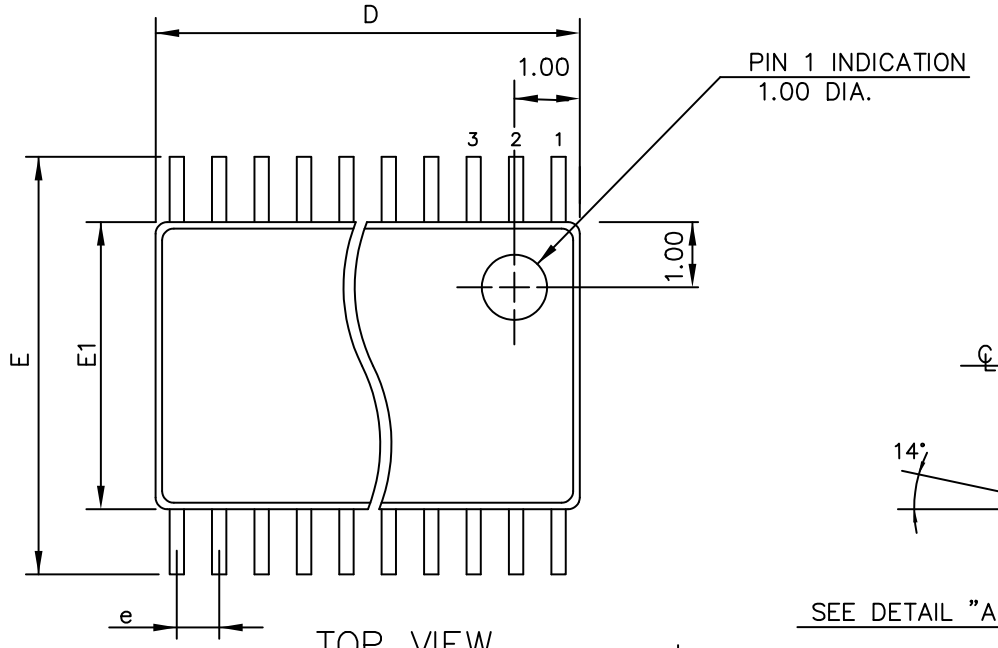
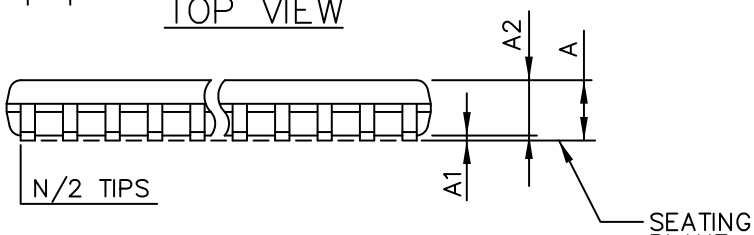
TSSOP 16
CASE 948AH–01
ISSUE O

DATE 19 SEP 2008



TOP VIEW

END VIEW



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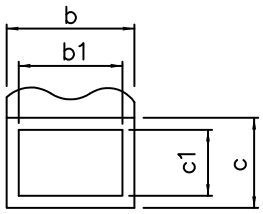
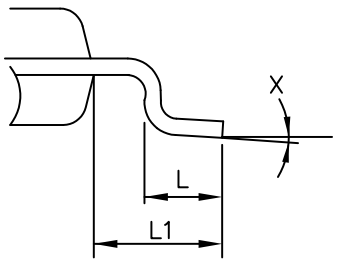


SECTION "B–B"

THIS TABLE FOR 0.65mm PITCH

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	D	N
	MIN.	NOM.	MAX.			
A	——	——	1.10	AA/AAT	3.00 BSC	8
A_1	0.05	——	0.15	AB–1/ABT	5.00 BSC	14
A_2	0.85	0.90	0.95	AB/ABT	5.00 BSC	16
b	0.19	–	0.30	AD/ADT	7.80 BSC	24
b1	0.19	0.22	0.25			
c	0.09	–	0.20			
c1	0.09	0.127	0.16			
D	SEE VARIATIONS					
E1	4.30	4.40	4.50			
e	0.65 BSC					
E	6.40 BSC					
L	0.50	0.60	0.70			
L1	1.00 REF					
N	SEE VARIATIONS					
X	0°	——	8°			



DETAIL 'A'

ALL DIMENSIONS IN MILLIMETERS

MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D PER SIDE

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