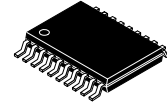


# Octal Buffer/Line Driver with 3-STATE Outputs

## 74VHC240



TSSOP20, 4.4x6.5  
CASE 948AQ

### General Description

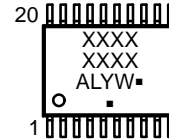
The VHC240 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHC240 is an inverting 3-STATE buffer having two active-LOW output enables. This device is designed to drive buslines or buffer memory address registers.

An input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

### Features

- High Speed:  $t_{PD} = 3.6 \text{ ns (Typ)}$  at  $T_A = 25^\circ\text{C}$
- Low Power Dissipation:  $I_{CC} = 4 \mu\text{A (Max)}$  @  $T_A = 25^\circ\text{C}$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min)
- Power Down Protection is Provided on All Inputs
- Low Noise:  $V_{OLP} = 0.9 \text{ V (Max)}$
- Pin and Function Compatible with 74HC240
- This is a Pb-Free Device

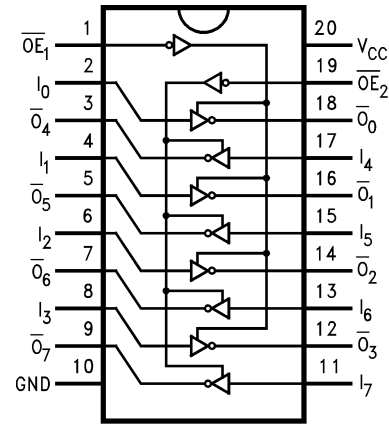
### MARKING DIAGRAM



- XXXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

### CONNECTION DIAGRAM



### PIN DESCRIPTIONS

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
$I_0-I_7$	Inputs
$\overline{O}_0-\overline{O}_7$	Outputs 3-STATE Outputs

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

# 74VHC240

## Logic Symbol

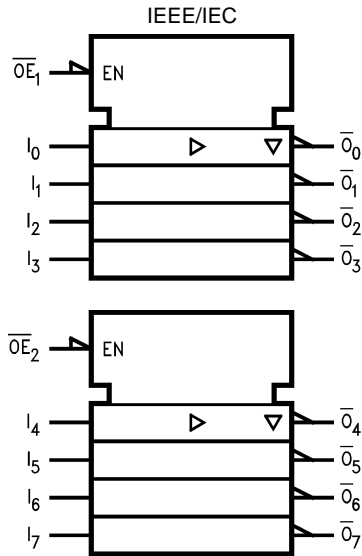


Figure 1. Logic Symbol

## TRUTH TABLES

Inputs		Outputs
$\overline{OE}_1$	$I_n$	(Pins 12, 14, 16, 18)
L	H	H
L	L	L
H	X	Z

Inputs		Outputs
$\overline{OE}_1$	$I_n$	(Pins 3, 5, 7, 9)
L	H	H
L	L	L
H	X	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
$V_{CC}$	DC Supply Voltage		-0.5 to +6.5	V
$V_{IN}$	DC Input Voltage		-0.5 to +6.5	V
$V_{OUT}$	DC Output Voltage		-0.5 to $V_{CC} + 0.5$	V
$I_{IN}$	DC Input Current, per Pin		$\pm 20$	mA
$I_{OUT}$	DC Output Current, per Pin		$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins		$\pm 75$	mA
$I_{IK}$	Input Clamp Current		-20	mA
$I_{OK}$	Output Clamp Current		$\pm 20$	mA
$T_{STG}$	Storage Temperature Range		-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
$T_J$	Junction Temperature under Bias		+150	°C
$\theta_{JA}$	Thermal Resistance (Note 2)		150	°C/W
$P_D$	Power Dissipation in Still Air at 25°C		833	mW
MSL	Moisture Sensitivity		Level 1	
$F_R$	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.240 in	
$V_{ESD}$	ESD Withstand Voltage (Note 3)	Human Body Model	2000	V
		Charged Device Model	N/A	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

# 74VHC240

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage	2.0	5.5	V	
$V_{IN}$	DC Input Voltage (Note 4)	0	5.5	V	
$V_{OUT}$	DC Output Voltage (Note 4)	0	$V_{CC}$	V	
$T_A$	Operating Temperature	-40	+85	°C	
$t_r, t_f$	Input Rise or Fall Rate	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	0	100	ns/V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	0	20	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to }+85^\circ\text{C}$		Unit	
				Min	Typ	Max	Min	Max		
$V_{IH}$	HIGH Level Input Voltage		2.0	1.50	-	-	1.50	-	V	
			3.0-5.5	$0.7 \times V_{CC}$	-	-	$0.7 \times V_{CC}$	-		
$V_{IL}$	LOW Level Input Voltage		2.0	-	-	0.50	-	0.50	V	
			3.0-5.5	-	-	$0.3 \times V_{CC}$	-	$0.3 \times V_{CC}$		
$V_{OH}$	HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\ \mu\text{A}$	2.0	1.9	2.0	-	1.9	-	V
				3.0	2.9	3.0	-	2.9	-	
				4.5	4.4	4.5	-	4.4	-	
			$I_{OH} = -4\ \text{mA}$	3.0	2.58	-	-	2.48	-	
4.5	3.94	-		-	3.80	-				
$V_{OL}$	LOW Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\ \mu\text{A}$	2.0	-	0.0	0.1	-	0.1	V
				3.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
			$I_{OL} = 4\ \text{mA}$	3.0	-	-	0.36	-	0.44	
				4.5	-	-	0.36	-	0.44	
$I_{OZ}$	3-STATE Output Off-State Current	$V_{IN} = V_{IH}$ or $V_{IL}$ ; $V_{OUT} = V_{CC}$ or GND	5.5	-	-	$\pm 0.25$	-	$\pm 2.5$	$\mu\text{A}$	
$I_{IN}$	Input Leakage Current	$V_{IN} = 5.5\ \text{V}$ or GND	0-5.5	-	-	$\pm 0.1$	-	$\pm 1.0$	$\mu\text{A}$	
$I_{CC}$	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5	-	-	4.0	-	40.0	$\mu\text{A}$	

## NOISE CHARACTERISTICS

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$		Unit
				Typ	Limits	
$V_{OLP}$ (Note 5)	Quiet Output Maximum Dynamic $V_{OL}$	$C_L = 50\ \text{pF}$	5.0	0.6	0.9	V
$V_{OLV}$ (Note 5)	Quiet Output Minimum Dynamic $V_{OL}$	$C_L = 50\ \text{pF}$	5.0	-0.6	-0.9	V
$V_{IHD}$ (Note 5)	Minimum HIGH Level Dynamic Input Voltage	$C_L = 50\ \text{pF}$	5.0	-	3.5	V
$V_{ILD}$ (Note 5)	Maximum LOW Level Dynamic Input Voltage	$C_L = 50\ \text{pF}$	5.0	-	1.5	V

5. Parameter guaranteed by design.

# 74VHC240

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Unit	
				Min	Typ	Max	Min	Max		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time		C <sub>L</sub> = 15 pF	3.3 ±0.3	-	5.3	7.5	1.0	9.0	ns
			C <sub>L</sub> = 50 pF		-	7.8	11.0	1.0	12.5	
			C <sub>L</sub> = 15 pF	5.0 ±0.5	-	3.6	5.5	1.0	6.5	
			C <sub>L</sub> = 50 pF		-	5.1	7.5	1.0	8.5	
t <sub>PZL</sub> , t <sub>PZH</sub>	3-STATE Output Enable Time	R <sub>L</sub> = 1 kΩ	C <sub>L</sub> = 15 pF	3.3 ±0.3	-	6.6	10.6	1.0	12.5	ns
			C <sub>L</sub> = 50 pF		-	9.1	14.1	1.0	16.0	
			C <sub>L</sub> = 15 pF	5.0 ±0.5	-	4.7	7.3	1.0	8.5	
			C <sub>L</sub> = 50 pF		-	6.2	9.3	1.0	10.5	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	3-STATE Output Disable Time	R <sub>L</sub> = 1 kΩ	C <sub>L</sub> = 50 pF	3.3 ±0.3	-	10.3	14.0	1.0	16.0	ns
			C <sub>L</sub> = 50 pF	5.0 ±0.5	6.7	-	9.2	1.0	10.5	
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew	(Note 6)	C <sub>L</sub> = 50 pF	3.3 ±0.3	-	-	1.5	-	1.5	ns
			C <sub>L</sub> = 50 pF	5.0 ±0.5	-	-	1.0	-	1.0	
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open			-	4	10	-	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 5.0 V			-	6	-	-	-	pF
C <sub>PD</sub>	Power Dissipation Capacitance	(Note 7)			-	17	-	-	-	pF

6. Parameter guaranteed by design.  $t_{OSLH} - |t_{PLHmax} - t_{PLHmin}|$ ;  $t_{OSHL} - |t_{PHLmax} - t_{PHLmin}|$

7. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC} (opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$  (per bit).

## ORDERING INFORMATION

Device	Marking	Package	Shipping†
74VHC240MTCX	VHC 240	TSSOP20 (Pb-Free)	2500 Units / Tape & Reel

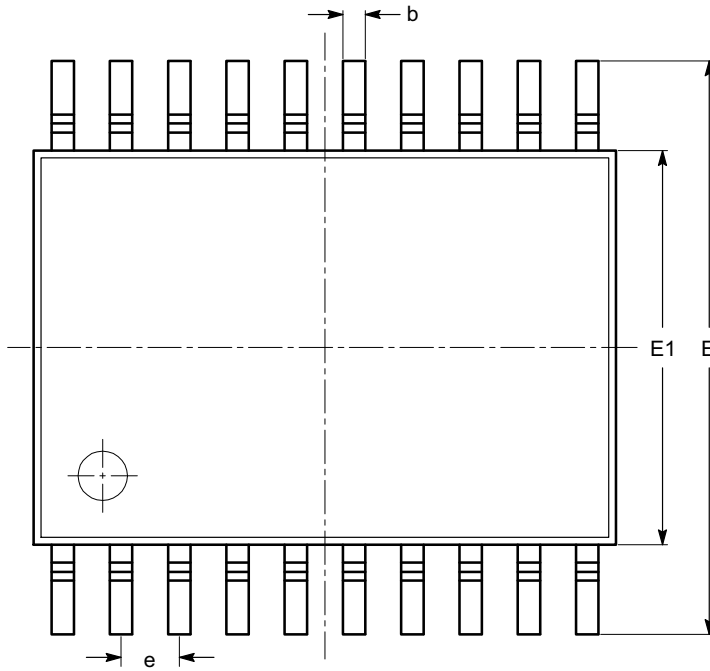
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**



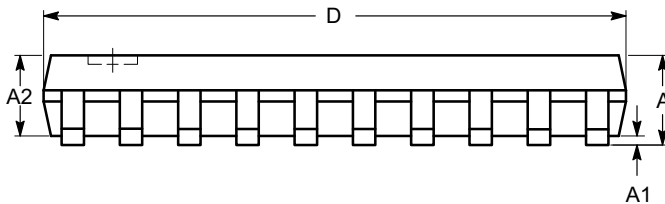
**TSSOP20, 4.4x6.5**  
**CASE 948AQ**  
**ISSUE A**

DATE 19 MAR 2009

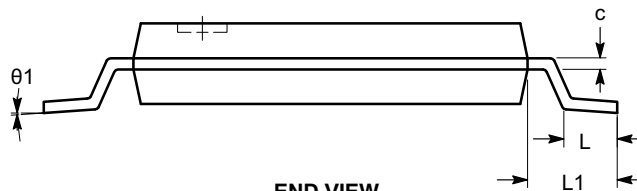


SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°		8°

**TOP VIEW**



**SIDE VIEW**



**END VIEW**

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

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