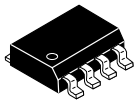
# 30 V PMOS-NMOS Bridge Driver

# FAN3278/D



SOIC8
CASE 751EB

## Description

The FAN3278 dual 1.5 A gate driver is optimized to drive a high−side P−channel MOSFET and a low−side N−channel MOSFET in motor control applications operating from a voltage rail up to 27 V. Internal circuitry limits the voltage applied to the gates of the external MOSFETs to 13 V maximum. The driver has TTL input thresholds and provides buffer and level translation from logic inputs. Internal circuitry prevents the output switching devices from operating if the $V_{DD}$ supply voltage is below the IC operation level. Internal 100 kΩ resistors bias the non−inverting output LOW and the inverting output to $V_{DD}$ to keep the external MOSFETs off during startup intervals when logic control signals may not be present.

The FAN3278 driver incorporates MOSFET devices for the final output stage, providing high current throughout the MOSFET turn−on / turn−off transition to minimize switching loss. The internal gate−drive regulators provide optimum gate−drive voltage when operating from a rail of 8 V to 27 V. The FAN3278 can be driven from a voltage rail of less than 8 V; however, its gate drive current is reduced.

The FAN3278 has two independent ENABLE pins that default to ON if not connected. If the ENABLE pin for non−inverting channel A is pulled LOW, OUTA is forced LOW. If the ENABLE pin for inverting channel B is pulled LOW, OUTB is forced HIGH. If an input is left unconnected, internal resistors bias the inputs such that the external MOSFETs are OFF.

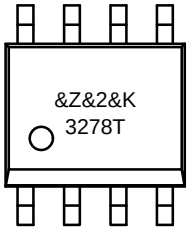
## Features

- 8 V to 27 V Optimum Operating Range
- Drives High−Side PMOS and Low−Side NMOS in Motor Control or Buck Step−Down Applications
- Output Drive−Voltage Magnitude Limited: <13 V for $V_{DD}$ up to 30 V
- Biases Each Load Device OFF with a 100 kΩ Resistor when $V_{DD}$ Below Operating Level
- Low−Voltage TTL Input Thresholds
- Peak Gate Drives at 12 V: +1.5 A Sink, −1.0 A Source
- Internal Resistors Hold Driver Off When No Inputs Present
- 8−Lead SOIC Package
- Rated from –40°C to +125°C Ambient
- This Device is Pb−Free, Halide Free and is RoHS Compliant

## Applications

- Motor Control with PMOS / NMOS Half−Bridge Configuration
- Buck Converters with High−Side PMOS Device; 100% Duty Cycle Operation Possible
- Logic−Controlled Load Circuits with High−Side PMOS Switch

## MARKING DIAGRAM




&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
3278T = Device Code

## ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

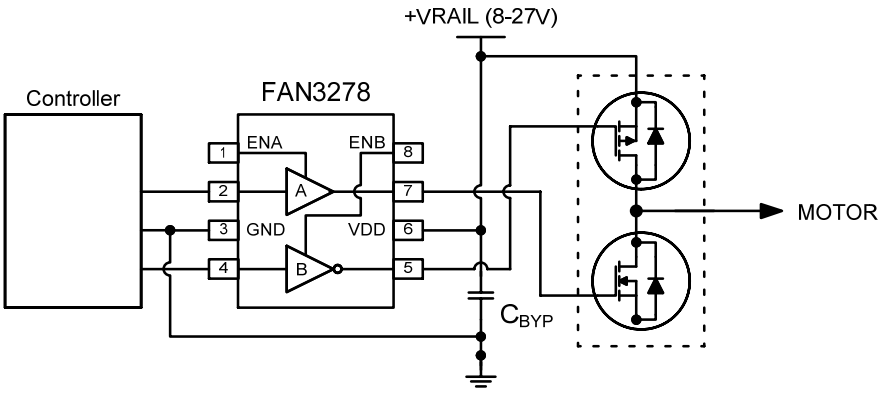



**Figure 1. Typical Application**

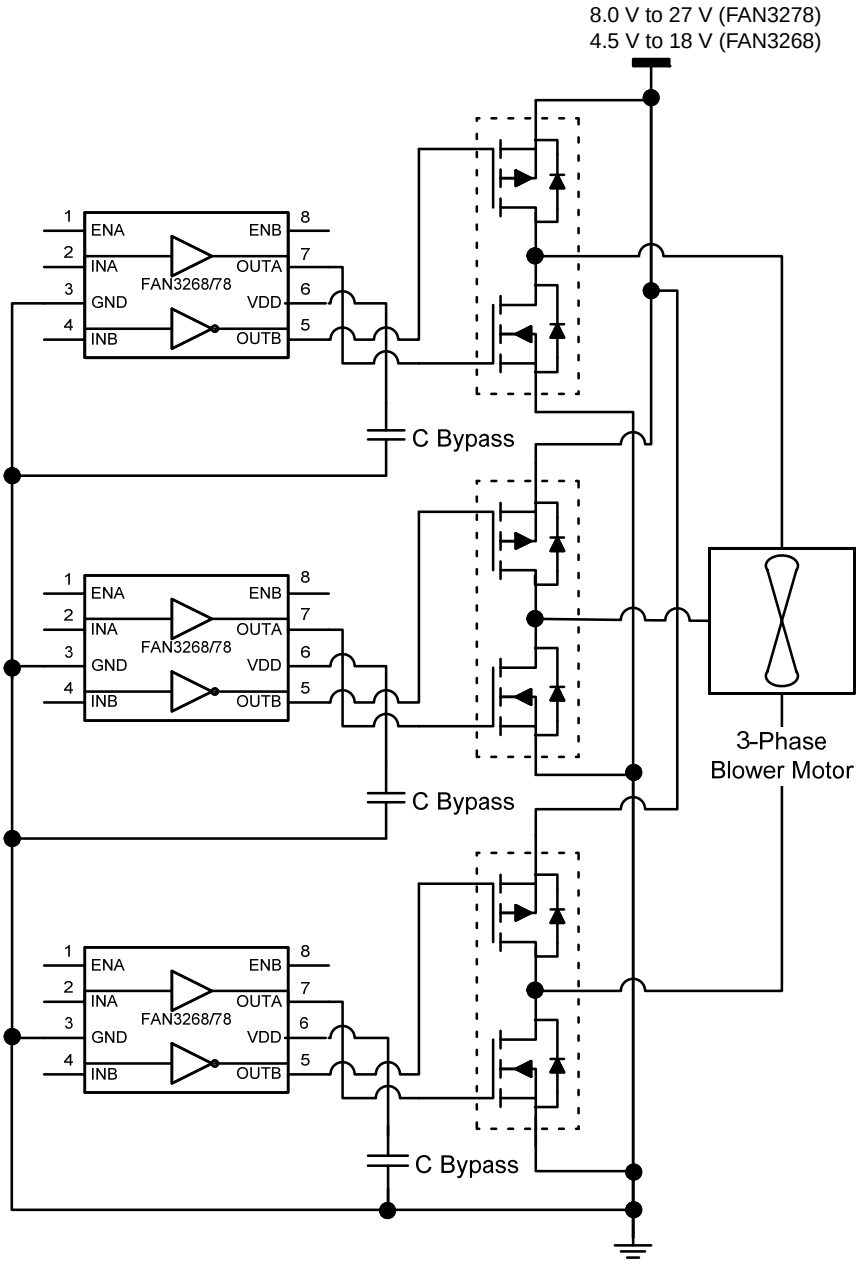



**Figure 2. Typical 3−Phase Blower Motor Drive Application**

## PIN CONFIGURATION

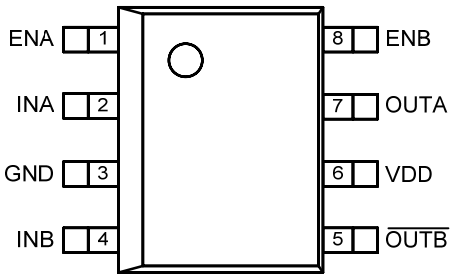



**Figure 3. Pin Configuration (Top View)**

### THERMAL CHARACTERISTICS (Note 1)

| Package | $\Theta_{JL}$ (Note 2) | $\Theta_{JT}$ (Note 3) | $\Theta_{JA}$ (Note 4) | $\Psi_{JB}$ (Note 5) | $\Psi_{JT}$ (Note 6) | Unit |
|---|---|---|---|---|---|---|
| 8−Pin Small−Outline Integrated Circuit (SOIC) | 40 | 31 | 89 | 43 | 3 | °C/W |

1. Estimates derived from thermal simulation; actual values depend on the application.
2. Theta_JL ($\Theta_{JL}$): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
3. Theta_JT ($\Theta_{JT}$): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top−side heatsink.
4. Theta_JA ($\Theta_{JA}$): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heatsink, as specified in JEDEC standards JESD51−2, JESD51−5, and JESD51−7, as appropriate.
5. Psi_JB ($\Psi_{JB}$): Thermal characterization parameter providing correlation between semiconductor junction temperature and an application circuit board reference point for the thermal environment defined in Note 4. For the SOIC−8 package, the board reference is defined as the PCB copper adjacent to pin 6.
6. Psi_JT ($\Psi_{JT}$): Thermal characterization parameter providing correlation between the semiconductor junction temperature and the center of the top of the package for the thermal environment defined in Note 4.

### PIN DEFINITIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | ENA | *Enable Input for Channel A.* Pull pin LOW to inhibit driver A. ENA has TTL thresholds. |
| 8 | ENB | *Enable Input for Channel B.* Pull pin LOW to inhibit driver B. ENB has TTL thresholds. |
| 3 | GND | *Ground.* Common ground reference for input and output circuits. |
| 2 | INA | *Input to Channel A.* |
| 4 | INB | *Input to Channel B.* |
| 7 | OUTA | *Gate Drive Output A:* Held LOW unless required input is present and $V_{DD}$ is above the internal voltage threshold where the IC is functional. |
| 5 | $\overline{\text{OUTB}}$ | *Gate Drive Output B* (inverted from the input). Held HIGH unless the required input is present and $V_{DD}$ is above the internal voltage threshold where the IC is functional. |
| 6 | VDD | *Supply Voltage.* Provides power to the IC. |

### OUTPUT LOGIC

| FAN3278 (Channel A) | | |
|---|---|---|
| **ENA** | **INA** | **OUTA** |
| 0 | 0 (Note 7) | 0 |
| 0 | 1 | 0 |
| 1 (Note 7) | 0 (Note 7) | 0 |
| 1 (Note 7) | 1 | 1 |

| FAN3278 (Channel B) | | |
|---|---|---|
| **ENB** | **INB** | **OUTB** |
| 0 | 0 (Note 7) | 1 |
| 0 | 1 | 1 |
| 1 (Note 7) | 0 (Note 7) | 1 |
| 1 (Note 7) | 1 | 0 |

7. Default input signal if no external connection is made.

## BLOCK DIAGRAM

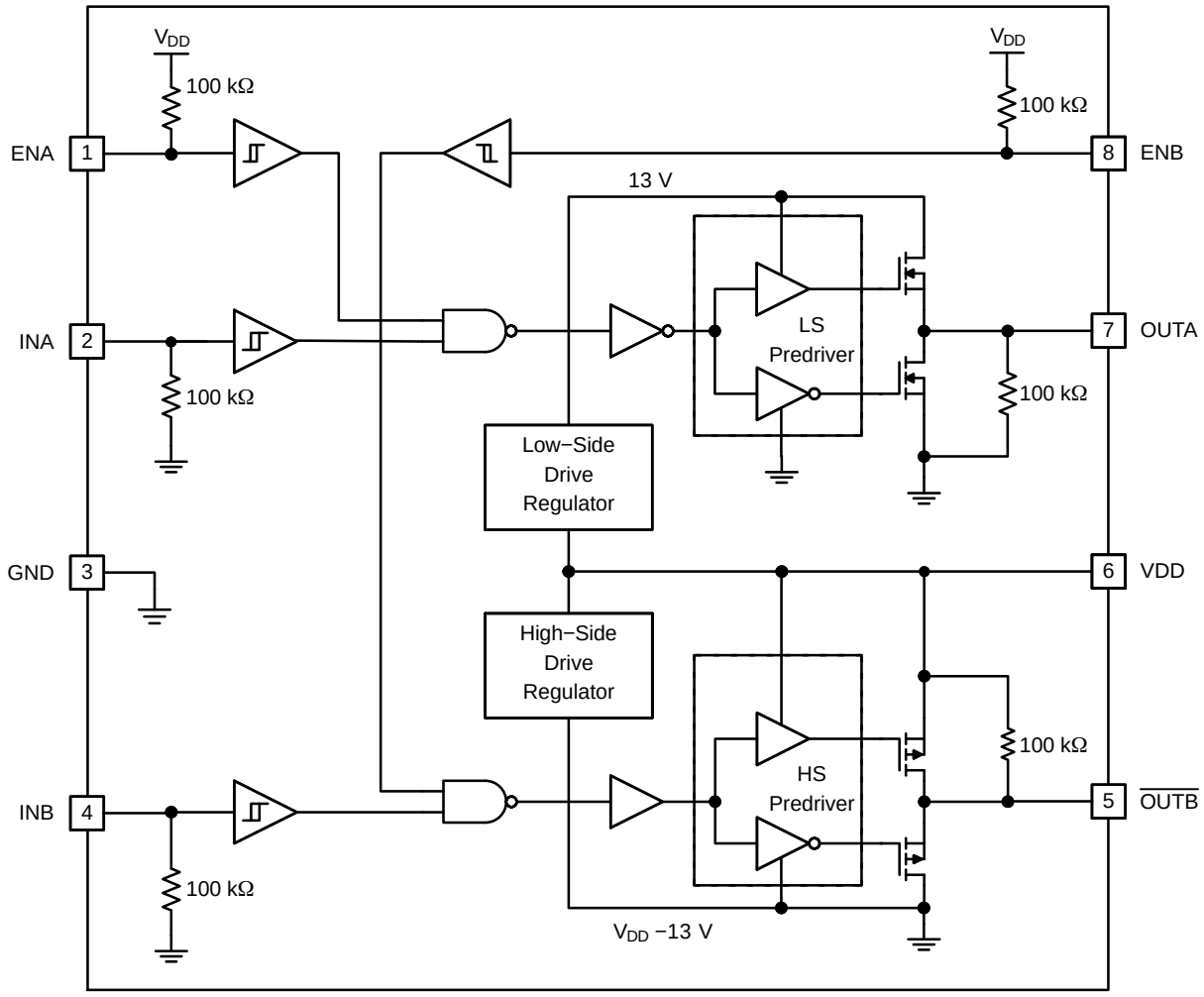



**Figure 4. Block Diagram**

### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | VDD to PGND | −0.3 | 30.0 | V |
| $V_{EN}$ | ENA, ENB to GND | GND − 0.3 | $V_{DD}$ + 0.3 | V |
| $V_{IN}$ | INA, INB to GND | GND − 0.3 | $V_{DD}$ + 0.3 | V |
| $V_{OUT}$ | OUTA, OUTB to GND | GND − 0.3 | $V_{DD}$ + 0.3 | V |
| $T_L$ | Lead Soldering Temperature (10 Seconds) | − | +260 | °C |
| $T_J$ | Junction Temperature | −55 | +150 | °C |
| $T_{STG}$ | Storage Temperature | −65 | +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage Range | 8 | 27 | V |
| $V_{EN}$ | Enable Voltage (ENA, ENB) | 0 | $V_{DD}$ | V |
| $V_{IN}$ | Input Voltage (INA, INB) | 0 | $V_{DD}$ | V |
| TA | Operating Ambient Temperature | −40 | +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted, $V_{DD}$ = 12 V and $T_J$ = −40°C to +125°C. Currents are defined as positive into the device ($I_{sink}$) and negative out of the device ($I_{source}$).)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $V_{DD}$ | Optimum Operating Range (Note 8) | | 8 | – | 27 | V |
| $I_{DD}$ | Supply Current Inputs / EN Not Connected | | – | 1.3 | 2.0 | mA |
| $V_{ON}$ | Turn−On Voltage (Note 9) | INA = ENA = $V_{DD}$, INB = ENB = 0 V | – | 3.8 | – | V |
| $V_{HYS}$ | Turn−On / Turn−Off Hysteresis (Note 9) | INA = ENA = $V_{DD}$, INB = ENB = 0 V | – | 10 | – | mV |
| **INPUT** (Note 9) | | | | | | |
| $V_{IL}$ | INx Logic Low Threshold | | 0.8 | 1.1 | – | V |
| $V_{IH}$ | INx Logic High Threshold | | – | 1.80 | 2.25 | V |
| $V_{HYS}$ | Logic Hysteresis Voltage | | 0.4 | 0.7 | 1.0 | V |
| **ENABLE** | | | | | | |
| $V_{ENL}$ | Enable Logic Low Threshold | EN from 5 V to 0 V | 0.8 | 1.2 | – | V |
| $V_{ENH}$ | Enable Logic High Threshold | EN from 0 V to 5 V | – | 1.60 | 2.25 | V |
| $V_{HYS}$ | Logic Hysteresis Voltage (Note 10) | | – | 0.7 | – | V |
| $R_{PU}$ | Enable Pull−Up Resistance | | – | 100 | – | kΩ |
| $t_{D1}$ | Propagation A Delay, EN Rising (Note 11) | 0 − 5 $V_{IN}$, 1 V/ns Slew Rate | – | 44 | 70 | ns |
| $t_{D2}$ | Propagation A Delay, EN Falling (Note 11) | 0 − 5 $V_{IN}$, 1 V/ns Slew Rate | – | 33 | 60 | ns |
| $t_{D2}$ | Propagation B Delay, EN Rising (Note 11) | 0 − 5 $V_{IN}$, 1 V/ns Slew Rate | – | 39 | 70 | ns |
| $t_{D1}$ | Propagation B Delay, EN Falling (Note 11) | 0 − 5 $V_{IN}$, 1 V/ns Slew Rate | – | 29 | 60 | ns |
| **OUTPUT** | | | | | | |
| $I_{PK\_OFF}$ | OUT Current, Peak, Turn−Off (Note 10) | $C_{LOAD}$ = 0.1 μF, f = 1 kHz | – | 1.5 | – | A |
| $I_{PK\_ON}$ | OUT Current, Peak, Turn−On (Note 10) | $C_{LOAD}$ = 0.1 μF, f = 1 kHz | – | −1.0 | – | A |
| $I_{OFF}$ | OUT Current, Mid−Voltage, Turn−Off (Note 10) | OUT at $V_{DD}$, $C_{LOAD}$ = 0.1 μF, f = 1 kHz | – | 1.0 | – | A |
| $I_{ON}$ | OUT Current, Mid−Voltage, Turn−On (Note 10) | OUT at $V_{DD}$/2, $C_{LOAD}$ = 0.1 μF, f = 1 kHz | – | −0.5 | – | A |
| $V_{OUTA}$ | OUTA Drive Voltage | $V_{DD}$ = 27 V, INA = “HI” | – | 11 | 13 | V |
| $V_{OUTB}$ | OUTB Drive Voltage, $V_{DD}$ − $V_{OUTB}$ | $V_{DD}$ = 27 V, INA = “HI” | – | 11 | 13 | V |
| $V_{OUTA}$ | OUTA Drive Voltage | $V_{DD}$ = 10 V, INB = “HI” | 6.5 | 7.0 | – | V |
| $V_{OUTB}$ | OUTB Drive Voltage, $V_{DD}$ − $V_{OUTB}$ | $V_{DD}$ = 10 V, INB = “HI” | 6.5 | 7.0 | – | V |
| $R_{O\_A\_SINK}$ | OUTA Sink Impedance (Turn−Off) (Note 10) | $V_{DD}$ = 6 V, $C_{LOAD}$ = 0.1 μF | – | 4.2 | – | Ω |
| $R_{O\_A\_SRC}$ | OUTA Source Impedance (Turn−On) (Note 10) | $V_{DD}$ = 6 V, $C_{LOAD}$ = 0.1 μF | – | 10.3 | – | Ω |
| $R_{O\_B\_SINK}$ | OUTB Sink Impedance (Turn−On) (Note 10) | $V_{DD}$ = 6 V, $C_{LOAD}$ = 0.1 μF | – | 6.8 | – | Ω |
| $R_{O\_B\_SRC}$ | OUTB Source Impedance (Turn−Off) (Note 10) | $V_{DD}$ = 6 V, $C_{LOAD}$ = 0.1 μF | – | 13.7 | – | Ω |

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted, $V_{DD}$ = 12 V and $T_J$ = −40°C to +125°C. Currents are defined as positive into the device ($I_{sink}$) and negative out of the device ($I_{source}$).) (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | |
| $t_{ON,N}$ | Output A Rise Time (Note 11) | $C_{LOAD}$ = 1000 pF to GND | − | 17 | 30 | ns |
| $t_{OFF,N}$ | Output A Fall Time (Note 11) | $C_{LOAD}$ = 1000 pF to GND | − | 8 | 15 | ns |
| $t_{ON,P}$ | Output B Fall Time (Note 11) | $C_{LOAD}$ = 1000 pF to $V_{DD}$ | − | 21 | 30 | ns |
| $t_{OFF,P}$ | Output B Rise Time (Note 11) | $C_{LOAD}$ = 1000 pF to $V_{DD}$ | − | 8 | 15 | ns |
| $t_{D1}$ | Output Propagation Delay On (Note 11) | 0 − 5 $V_{IN}$, 1 V/ns Slew Rate | − | 45 | 70 | ns |
| $t_{D2}$ | Output Propagation Delay Off (Note 11) | 0 − 5 $V_{IN}$, 1 V/ns Slew Rate | − | 35 | 60 | ns |
| $I_{RVS}$ | Output Reverse Current Withstand (Note 10) | | − | 500 | − | mA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. The internal gate−drive regulators provide optimum gate−drive voltage when operating from a rail of 8 V to 27 V. The FAN3278 can be driven from a voltage rail of less than 8 V; however, with reduced gate drive current.
9. EN inputs have near−TTL thresholds *(refer to the ENABLE section)*.
10. Not tested in production.
11. See the Timing Diagrams of Figure 5 and Figure 6.

## TIMING DIAGRAMS

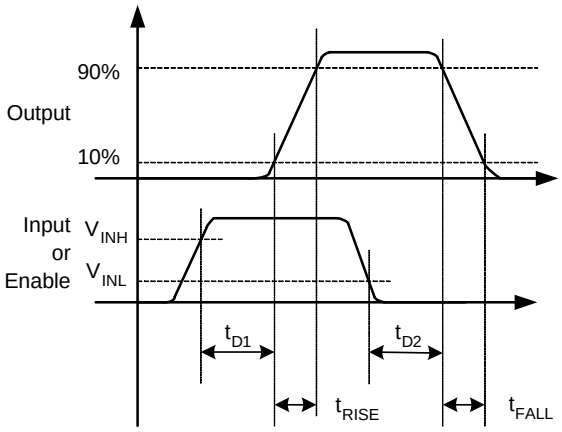



**Figure 5. Non−Inverting**

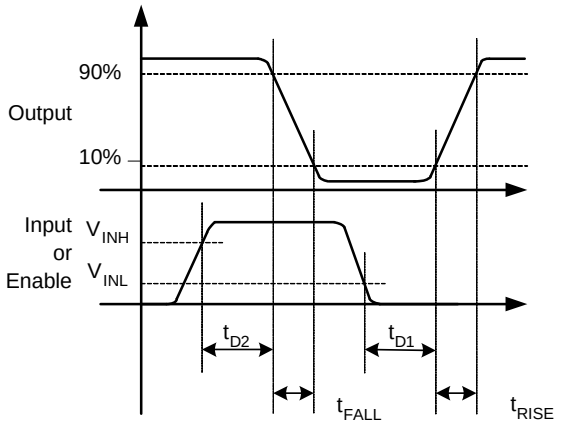



**Figure 6. Inverting**

## TYPICAL PERFORMANCE CHARACTERISTICS

(Typical characteristics are provided at $T_A$ = 25°C and $V_{DD}$ = 12 V unless otherwise noted.)

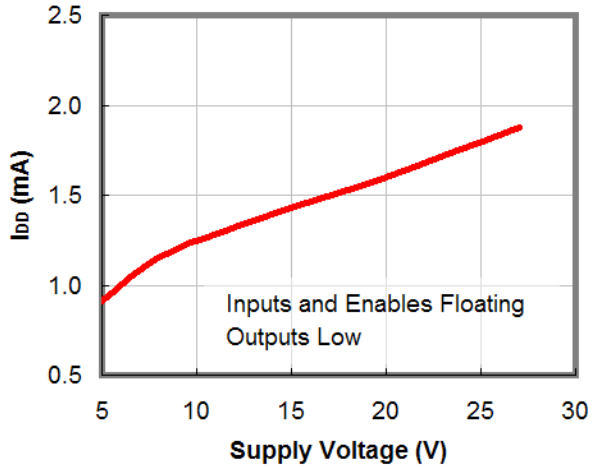



**Figure 7. $I_{DD}$ (Static) vs. Supply Voltage (Note 12)**

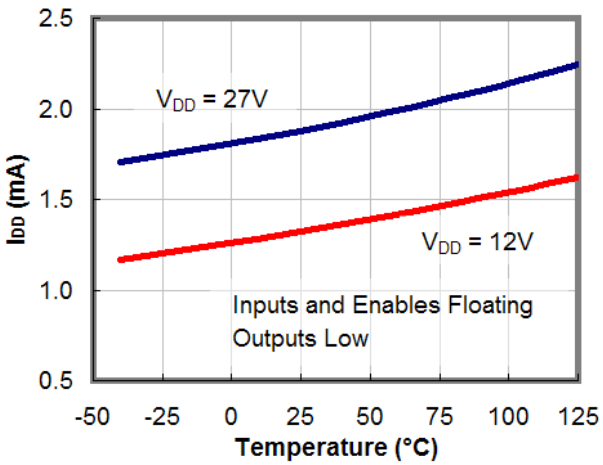



**Figure 8. $I_{DD}$ (Static) vs. Temperature (Note 12)**

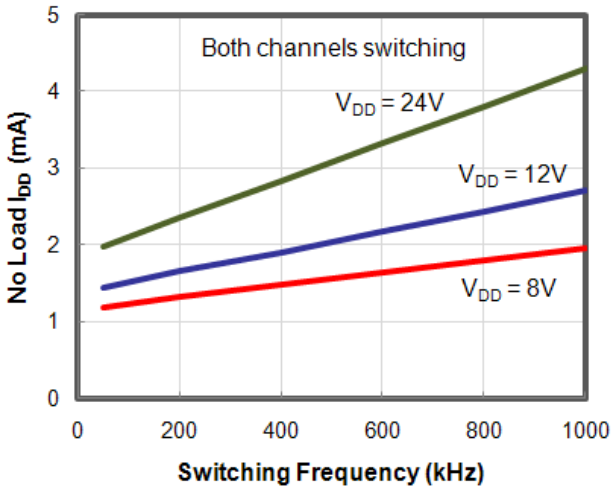



**Figure 9. $I_{DD}$ (No Load) vs. Frequency**

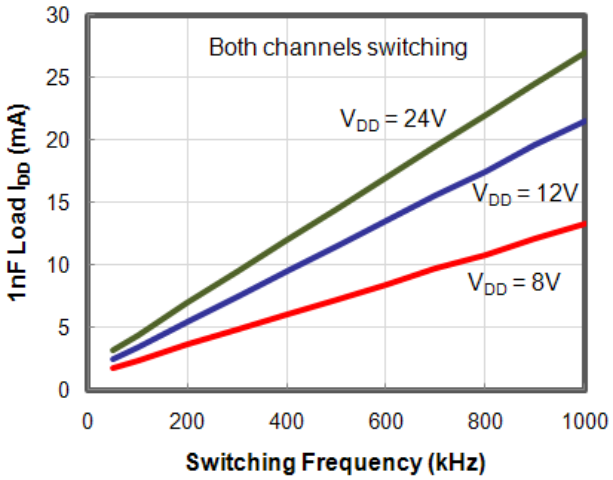



**Figure 10. $I_{DD}$ (1 nF Load) vs. Frequency**

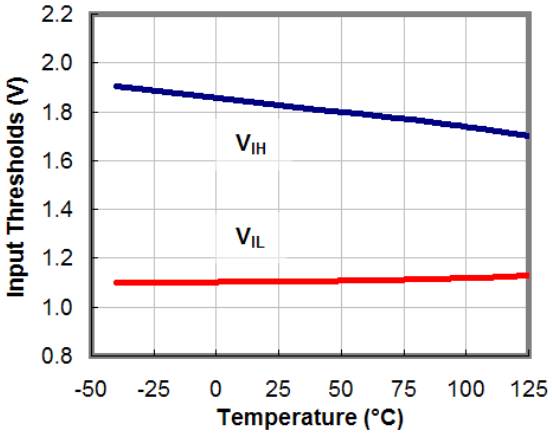



**Figure 11. Input Thresholds vs. Temperature**

## TYPICAL PERFORMANCE CHARACTERISTICS

(Typical characteristics are provided at $T_A$ = 25°C and $V_{DD}$ = 12 V unless otherwise noted.)

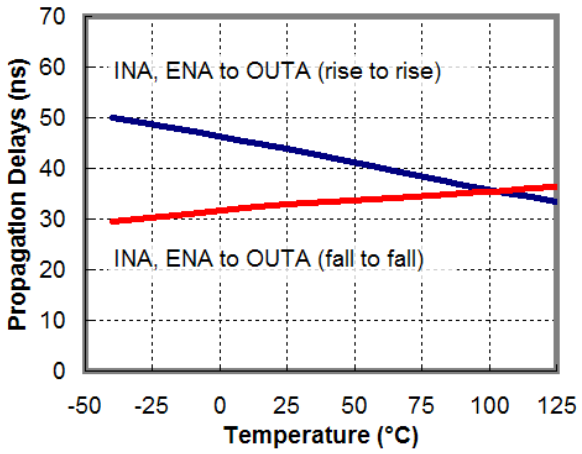



**Figure 12. Propagation Delays vs. Temperature**

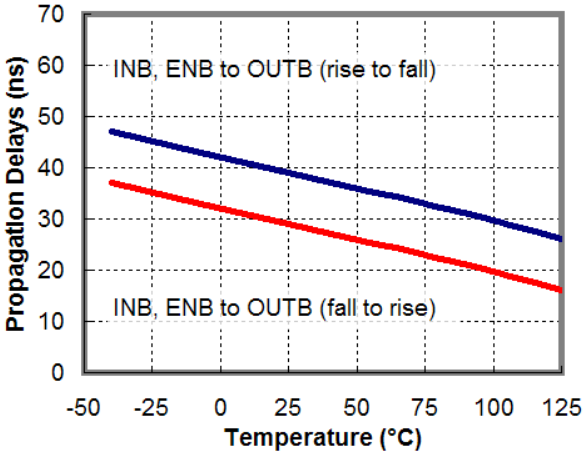



**Figure 13. Propagation Delays vs. Temperature**

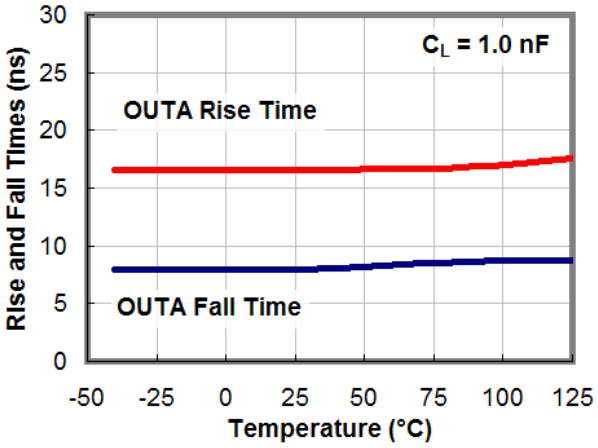



**Figure 14. Rise and Fall Times vs. Temperature**

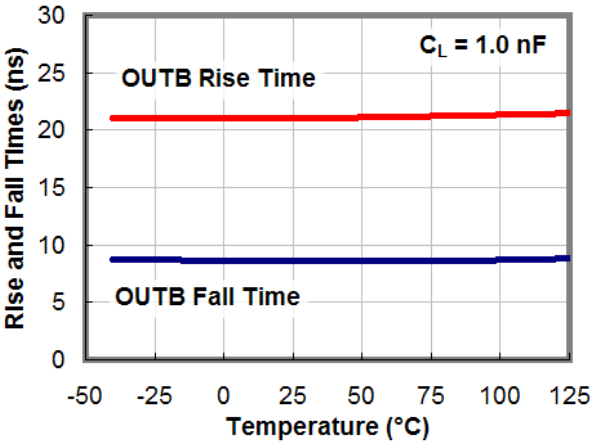



**Figure 15. Rise and Fall Times vs. Temperature**

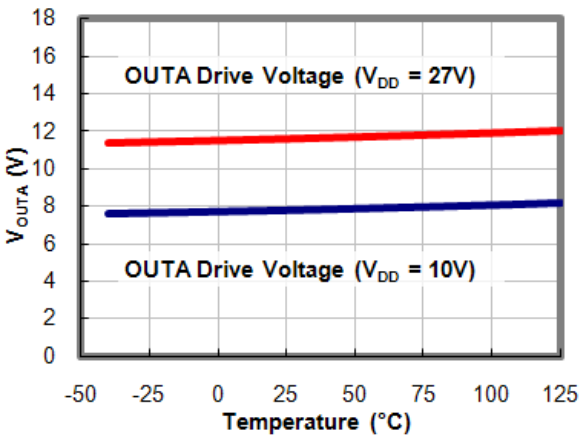



**Figure 16. Gate Drive Voltage vs. Temperature**

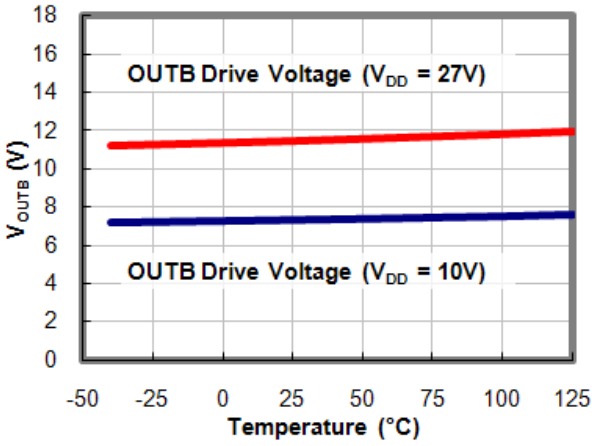



**Figure 17. Gate Drive Voltage vs. Temperature**

NOTE:

12. For any inverting inputs pulled LOW, non−inverting inputs pulled HIGH, or outputs driven HIGH; static $I_{DD}$ increases by the current flowing through the corresponding pull−up/down resistor, shown in Figure 4.

## APPLICATIONS INFORMATION

### Input Thresholds

The FAN3278 driver has TTL input thresholds and provides buffer and level translation functions from logic inputs. The input thresholds meet industry−standard TTL−logic thresholds, independent of the $V_{DD}$ voltage, and there is a hysteresis voltage of approximately 0.4 V. These levels permit the inputs to be driven from a range of input logic signal levels for which a voltage over 2 V is considered logic HIGH. The driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6 V/μs or faster, so a rise time from 0 to 3.3 V should be 550 ns or less. With reduced slew rate, circuit noise could cause the driver input voltage to exceed the hysteresis voltage and retrigger the driver input inadvertently.

### Static Supply Current

In the IDD (static) typical performance characteristics (*see Figure 7 and Figure 8*), the curve is produced with all inputs / enables floating (OUTA is LOW, OUTB is HIGH) and indicates the lowest static IDD current for the tested configuration. For other states, additional current flows through the 100 kΩ resistors on the inputs and outputs, shown in the block diagram (*see Figure 4*). In these cases, the static $I_{DD}$ current is the value obtained from the curves plus this additional current.

### Gate Drive Regulator

FAN3278 incorporates internal regulators to regulate the gate drive voltage. The output pin slew rate is determined by this gate drive voltage and the load on the output. It is not user adjustable, but a series resistor can be added if a slower rise or fall time is needed at the MOSFET gate.

### Startup Operation

The FAN3278 startup logic is optimized to drive a ground−referenced N−channel MOSFET with channel A and a $V_{DD}$−referenced P−channel MOSFET with channel B.

The optimum operating voltage of the FAN3278 is 8 V to 27 V. It has an internal “watchdog” circuit that provides a loose UVLO turn−on voltage ($V_{ON}$) of approximately 3.8 V with a small hysteresis of about 10 mV. However, it is recommended that $V_{DD}$ is greater than 4.75 V in all application circuits.

When the $V_{DD}$ supply voltage is below the level needed to operate the internal circuitry, the outputs are biased to hold the external MOSFETs in OFF state. Internal 100 kΩ resistors bias the non−inverting output LOW and the inverting output to $V_{DD}$ to keep the external MOSFETs off during startup intervals when input control signals may not be present.

Figure 18 shows startup waveforms for non−inverting channel A. At power−up, the driver output for channel A remains LOW until $V_{DD}$ reaches the voltage where the device starts operating, then OUTA operates in−phase with INA.

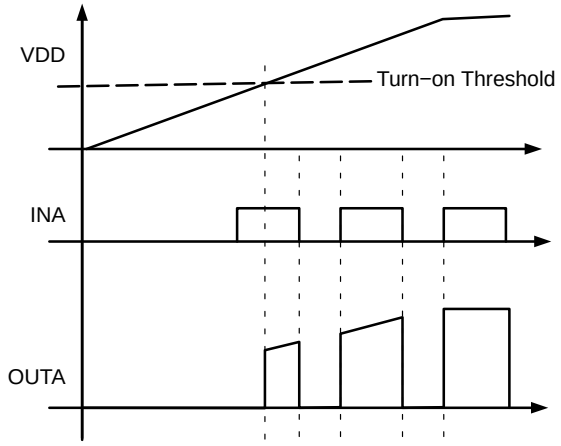



**Figure 18. Non−Inverting Startup Waveforms**

Figure 19 illustrates startup waveforms for inverting channel B. At power−up, the driver output for channel B is tied to $V_{DD}$ through an internal 100 kΩ resistor until $V_{DD}$ reaches the voltage where the device starts operating, then OUTB operates out of phase with INB.

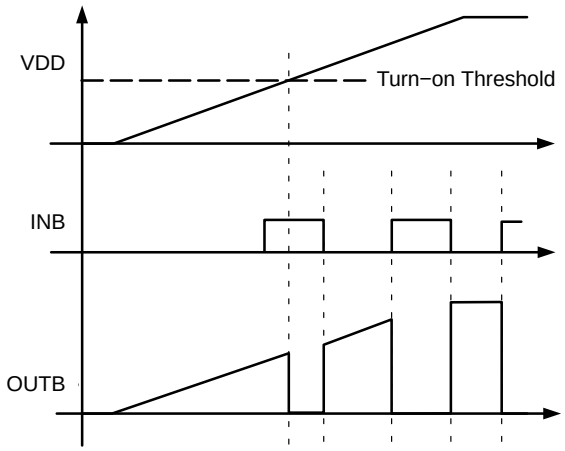



**Figure 19. Inverting Startup Waveforms**

It is possible, during startup, before $V_{DD}$ has reached approximately 4.5 V, that the output pulse width may take a few switching cycles to reach the full duty−cycle of the input pulse. This is due to internal propagation delays affecting the operation with higher switching frequency (e.g. >100 kHz) and slow $V_{DD}$ ramp−up (e.g. <20 V/ms). For this reason, it is recommended that $V_{DD}$ should be greater than 4.75 V before any INA or INB signals are present.

For high−frequency applications (several hundred kHz up to 1 MHz), where the above recommendation of $V_{DD}$ > 4.75 V is not possible, the use of ENABLES to actively hold the outputs LOW until $V_{DD}$ > 4.75 V assures the driver output pulse width follows the input from 4.75 V up to 28 V.

### $V_{DD}$ Bypass Capacitor Guidelines

To enable this IC to turn a device on quickly, a local high−frequency bypass capacitor, $C_{BYP}$, with low ESR and ESL should be connected between the VDD and GND pins with minimal trace length. This capacitor is in addition to bulk electrolytic capacitance of 10 μF to 47 μF commonly found on driver and controller bias circuits.

A typical criterion for choosing the value of $C_{BYP}$ is to keep the ripple voltage on the $V_{DD}$ supply to ≤5%. This is often achieved with a value ≥20 times the equivalent load capacitance $C_{EQV}$, defined as $Q_{GATE}/V_{DD}$. Ceramic capacitors of 0.1 μF to 1 μF or larger are common choices, as are dielectrics, such as X5R and X7R, with stable temperature characteristics and high pulse current capability.

If circuit noise affects normal operation, the value of $C_{BYP}$ may be increased to 50−100 times the $C_{EQV}$ or $C_{BYP}$ may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1−10 nF, mounted closest to the VDD and GND pins to carry the higher−frequency components of the current pulses. The bypass capacitor must provide the pulsed current from both of the driver channels and, if the drivers are switching simultaneously, the combined peak current sourced from the $C_{BYP}$ can be twice as large as when a single channel is switching.

### Layout and Connection Guidelines

The FAN3278 gate driver incorporates fast−reacting input circuits, short propagation delays, and powerful output stages capable of delivering current peaks over 1.5 A to facilitate fast voltage transition times. The following layout and connection guidelines are strongly recommended:

- Keep high−current output and power ground paths separate from logic and enable input signals and signal ground paths. This is especially critical when dealing with TTL−level logic thresholds at driver inputs and enable pins.
- Keep the driver as close to the load as possible to minimize the length of high−current traces. This reduces the series inductance to improve high− speed switching, while minimizing the loop area that can couple EMI to the driver inputs and surrounding circuitry.
- If the inputs to a channel are not externally connected, the internal 100 kΩ resistors indicated on block diagrams command a low output on channel A and a high output on channel B. In noisy environments, it may be necessary to tie inputs of an unused channel to VDD or GND using short traces to prevent noise from causing spurious output switching.
- Many high−speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output mis− triggering. These effects can be obvious if the circuit is tested in breadboard or non−optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.
- The turn−on and turn−off current paths should be minimized, as discussed above.

### Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of two components, $P_{GATE}$ and $P_{DYNAMIC}$:

$$P_{TOTAL} = P_{GATE} + P_{DYNAMIC} \quad \text{(eq. 1)}$$

Gate Driving Loss: The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET with a specified gate−source voltage, $V_{GS}$, with gate charge, $Q_G$, at switching frequency, $f_{SW}$, is determined by:

$$P_{GATE} = Q_G \cdot V_{GS} \cdot f_{SW} \quad \text{(eq. 2)}$$

This needs to be calculated for each P−channel and N−channel MOSFET where the $Q_G$ is likely to be different.

Dynamic Pre−drive / Shoot−through Current: Power loss resulting from internal current consumption under dynamic operating conditions, including pin pull−up / pull−down resistors, can be obtained using the "$I_{DD}$ (No− Load) vs. Frequency" graphs in Figure 9 to determine the current $I_{DYNAMIC}$ drawn from $V_{DD}$ under actual operating conditions.

$$P_{DYNAMIC} = I_{DYNAMIC} \cdot V_{DD} \quad \text{(eq. 3)}$$

Once the power dissipated in the driver is determined, the driver junction rise with respect to circuit board can be evaluated using the following thermal equation, assuming $\psi_{JB}$ was determined for a similar thermal design (heat sinking and air flow):

$$T_J = P_{TOTAL} \cdot \psi_{JB} + T_B \quad \text{(eq. 4)}$$

where:

$T_J$ = driver junction temperature

$\psi_{JB}$ = (psi) thermal characterization parameter relating temperature rise to total power dissipation

$T_B$ = board temperature in location defined in Note 1 under Thermal Resistance table.

As an example of a power dissipation calculation, consider an application driving two MOSFETs (one P−channel and one N−channel, both with a gate charge of 60 nC each) with $V_{GS} = V_{DD} = 12$ V. At a switching frequency of 200 kHz, the total power dissipation is:

$$P_{GATE} = 60\ \text{nC} \cdot 12\ \text{V} \cdot 200\ \text{kHz} \cdot 2 = 0.288\ \text{W} \quad \text{(eq. 5)}$$

$$P_{DYNAMIC} = 1.65\ \text{mA} \cdot 12\ \text{V} = 0.020\ \text{W} \quad \text{(eq. 6)}$$

$$P_{TOTAL} = 0.308\ \text{W} \quad \text{(eq. 7)}$$

The SOIC−8 package has a junction−to−board thermal characterization parameter of $\psi_{JB}$ = 43°C/W. In a system application, the localized temperature around the device is a function of the layout and construction of the PCB along with airflow across the surfaces. To ensure reliable operation, the maximum junction temperature of the device must not exceed the absolute maximum rating of 150°C; with 80% derating, $T_J$ would be limited to 120°C. Rearranging Equation 4 determines the board temperature required to maintain the junction temperature below 120°C:

$$T_B = T_J - P_{TOTAL} \cdot \psi_{JB} \quad \text{(eq. 8)}$$

$$T_B = 120°C - 0.308\ W \cdot 43°C/W = 107°C \quad \text{(eq. 9)}$$

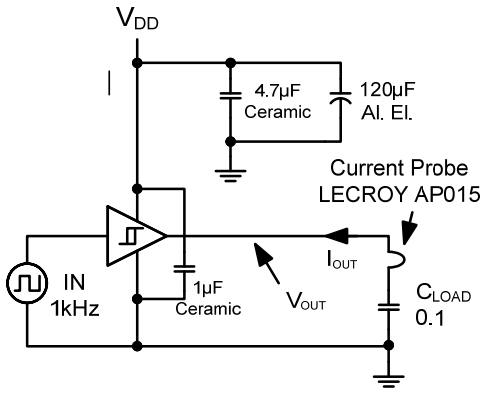



**Figure 20. Quasi−Static $I_{OUT}$ / $V_{OUT}$ Test Circuit**

## DIFFERENCES BETWEEN FAN3278 AND FAN3268

FAN3278 and FAN3268 are pin−compatible to each other and are designed to drive one P−Channel and one N−channel MOSFET in applications such as battery−powered compact fan / pump DC motor drives. However, there are key differences, highlighted in Table 1.

**Table 1. DIFFERENCES BETWEEN FAN3278 AND FAN3268**

| | FAN3278 | FAN3268 |
|---|---|---|
| **Supply Voltage** | 27 V Operating Maximum<br>30 V Absolute Maximum | 18 V Operating Maximum<br>20 V Absolute Maximum |
| **Gate Drive Regulator** | Yes, since the maximum operating $V_{DD}$ can be as high as 27 V, the gate voltage to the external MOSFETs is limited to about 13 V. | No gate drive regulator is needed. The gate drive voltage is $V_{DD}$ and the FAN3268 switches rail−to−rail. |
| **Minimum Operating Voltage** | The optimum operating range is 8 V to 27 V. After the IC turns on at about 3.8 V, the output tracks $V_{DD}$ up to the regulated voltage rail of about 11~13 V. Below 8 V of $V_{DD}$, the FAN3278 operates, but (a) slower and (b) with limited gate drive voltage until it reaches around 8 V. | 4.1 V is the UVLO turn−off voltage which is the minimum operating voltage. |
| **Startup** | The IC starts operating approximately at 3.8 V which acts as a loose UVLO threshold. It incorporates a “smart startup” feature where the outputs are held OFF before the IC starts operating. | Has the tight UVLO threshold of 4.5V on / 4.1V off. Incorporates “smart startup” (outputs held OFF before IC is fully operational at the UVLO threshold). |
| **Output Gate Drive Architecture** | Standard MOS−based output structure with gate drive clamp. | Compound MillerDrive™ architecture in the final output stage to provide a more efficient gate drive current during the Miller plateau stage of the turn− on/turn−off switching transition. |
| **OUTB Gate Drive Current Strength** | Optimized for P−channel: The turn−OFF (1.5 A) is stronger than turn−ON (1.0 A). | P−channel turn−ON (2.4 A) is stronger than turn−OFF (1.6 A). |

**Table 2. RELATED PRODUCTS**

| Part Number | Type | Gate Drive (Note 13) (Sink / Src) | Input Threshold | Logic | Package |
|---|---|---|---|---|---|
| FAN3111C | Single 1 A | +1.1 A / −0.9 A | CMOS | Single Channel of Dual−Input/Single−Output | SOT23−5, MLP6 |
| FAN3111E | Single 1 A | +1.1 A / −0.9 A | External (Note 14) | Single Non−Inverting Channel with External Reference | SOT23−5, MLP6 |
| FAN3100C | Single 2 A | +2.5 A / −1.8 A | CMOS | Single Channel of Two−Input/One−Output | SOT23−5, MLP6 |
| FAN3100T | Single 2 A | +2.5 A / −1.8 A | TTL | Single Channel of Two−Input/One−Output | SOT23−5, MLP6 |
| FAN3226C | Dual 2 A | +2.4 A / −1.6 A | CMOS | Dual Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3226T | Dual 2 A | +2.4 A / −1.6 A | TTL | Dual Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3227C | Dual 2 A | +2.4 A / −1.6 A | CMOS | Dual Non−Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3227T | Dual 2 A | +2.4 A / −1.6 A | TTL | Dual Non−Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3228C | Dual 2 A | +2.4 A / −1.6 A | CMOS | Dual Channels of Two−Input/One−Output, Pin Config.1 | SOIC8, MLP8 |
| FAN3228T | Dual 2 A | +2.4 A / −1.6 A | TTL | Dual Channels of Two−Input/One−Output, Pin Config.1 | SOIC8, MLP8 |
| FAN3229C | Dual 2 A | +2.4 A / −1.6 A | CMOS | Dual Channels of Two−Input/One−Output, Pin Config.2 | SOIC8, MLP8 |
| FAN3229T | Dual 2 A | +2.4 A / −1.6 A | TTL | Dual Channels of Two−Input/One−Output, Pin Config.2 | SOIC8, MLP8 |
| FAN3268T | Dual 2 A | +2.4 A / −1.6 A | TTL | Non−Inverting Channel (NMOS) and Inverting Channel (PMOS) + Dual Enables | SOIC8 |
| FAN3278T | Dual 2 A | +1.4 A / −1.0 A | TTL | 30 V Non−Inverting (NMOS) and Inverting (PMOS) + Dual Enable | SOIC8 |
| FAN3223C | Dual 4 A | +4.3 A / −2.8 A | CMOS | Dual Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3223T | Dual 4 A | +4.3 A / −2.8 A | TTL | Dual Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3224C | Dual 4 A | +4.3 A / −2.8 A | CMOS | Dual Non−Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3224T | Dual 4 A | +4.3 A / −2.8 A | TTL | Dual Non−Inverting Channels + Dual Enable | SOIC8, MLP8 |
| FAN3225C | Dual 4 A | +4.3 A / −2.8 A | CMOS | Dual Channels of Two−Input/One−Output | SOIC8, MLP8 |
| FAN3225T | Dual 4 A | +4.3 A / −2.8 A | TTL | Dual Channels of Two−Input/One−Output | SOIC8, MLP8 |
| FAN3121C | Single 9 A | +9.7 A / −7.1 A | CMOS | Single Inverting Channel + Enable | SOIC8, MLP8 |
| FAN3121T | Single 9 A | +9.7 A / −7.1 A | TTL | Single Inverting Channel + Enable | SOIC8, MLP8 |
| FAN3122T | Single 9 A | +9.7 A / −7.1 A | CMOS | Single Non−Inverting Channel + Enable | SOIC8, MLP8 |
| FAN3122C | Single 9 A | +9.7 A / −7.1 A | TTL | Single Non−Inverting Channel + Enable | SOIC8, MLP8 |

13. Typical currents with OUT at 6 V and $V_{DD}$ = 12 V.
14. Thresholds proportional to an externally supplied reference voltage.

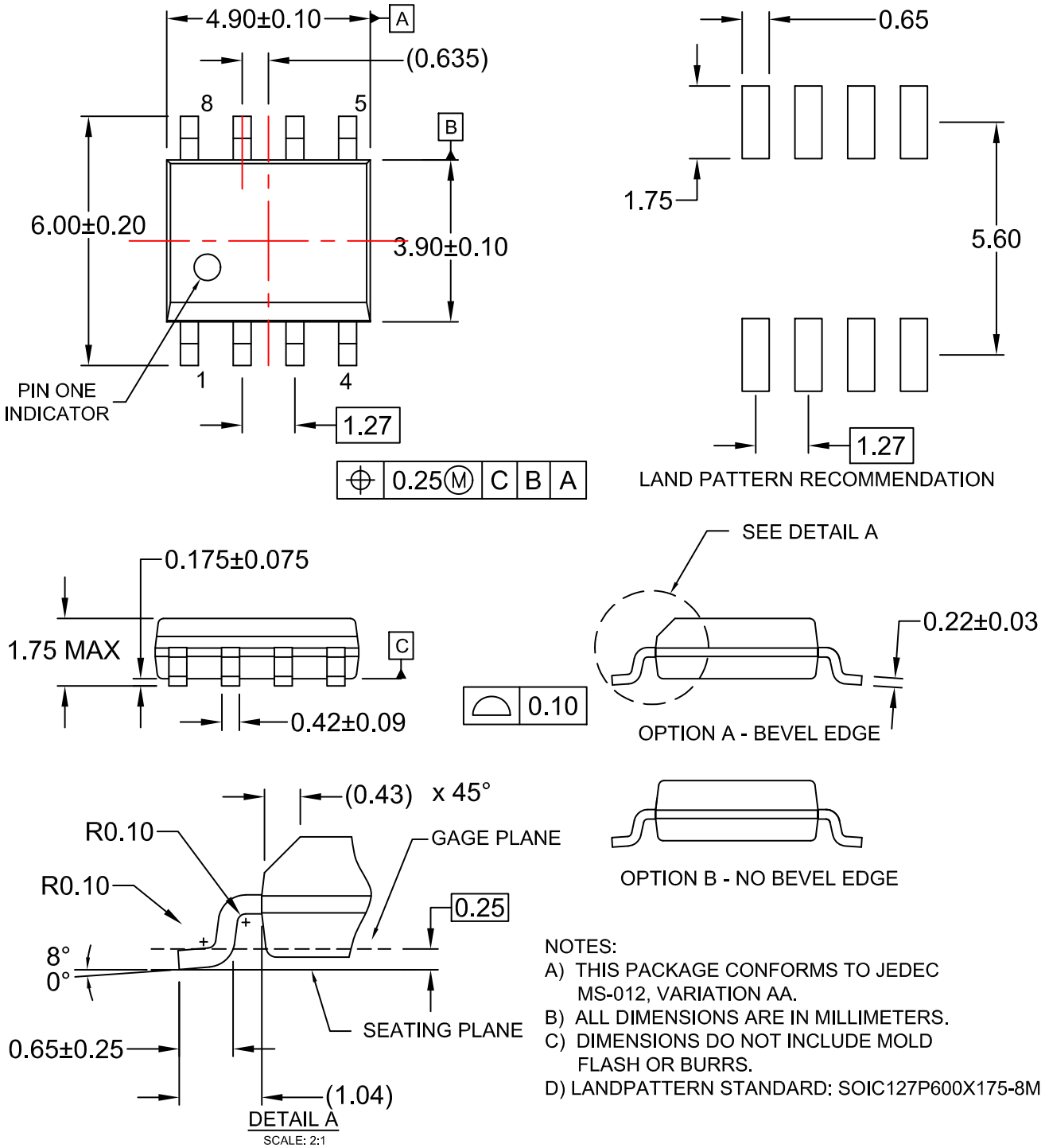
## ORDERING INFORMATION

| Part Number | Logic | Input Threshold | Package Type | Shipping† |
|---|---|---|---|---|
| FAN3278TMX | Non−Inverting Channel and Inverting Channel with Dual Enable | TTL | SOIC8 (Pb−Free, Halide Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**SOIC8**
CASE 751EB
ISSUE A

DATE 24 AUG 2017




NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

| | | |
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