

# Fixed-Output Synchronous TinyBoost<sup>®</sup> Regulator

## FAN48615



WLCSP9  
CASE 567QW

### Description

The FAN48615 is a low-power PWM only boost regulator designed to provide a minimum voltage-regulated rail from a standard single-cell Li-Ion battery and advanced battery chemistries. Even below the minimum system battery voltage, the device maintains the output voltage regulation for an output load current of 1000 mA. The combination of built-in power transistors, synchronous rectification, and low supply current suit the FAN48615 for battery-powered applications.

The FAN48615 is available in a 9-bump, 0.4 mm pitch, (1.215 x 1.215 mm) Wafer-Level Chip-Scale Package (WLCSP).

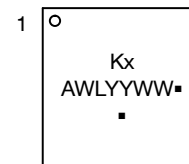
### Features

- Input Voltage Range: 2.7 V to 5.5 V
- Output Voltage: 5.25 V and 5.4 V
- 1000 mA Max. Load Capability
- PWM Only
- Up to 97% Efficient
- Forced Pass-Through Operation via EN Pin
- Internal Synchronous Rectification
- True Load Disconnect
- Short-Circuit Protection
- Three External Components: 2016 (Metric) 0.47  $\mu$ H Inductor, 0402 Input and 0603 Output Capacitors
- This is a Pb-Free Device

### Applications

- Class-D Audio Amplifier
- Boost for Low-Voltage Li-Ion Batteries
- Smart Phones, Tablets, Portable Devices
- RF Applications
- NFC Applications

### MARKING DIAGRAM



- KY / KZ = Specific Device Code
- F = Fab Indicator
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

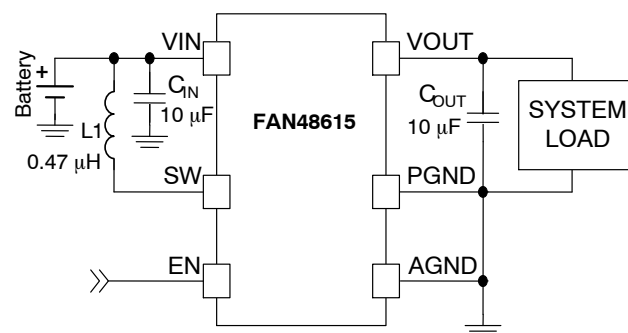


Figure 1. Typical Application

### ORDERING INFORMATION

Part Number	V <sub>OUT</sub>	Operating Temperature	Package	Packing	Device Marking
FAN48615UC08X	5.25 V	-40°C to 85°C	9-Bump, 0.4 mm Pitch, WLCSP Package	3000 / Tape & Reel	KY
FAN48615UC11X	5.40 V				KZ

# FAN48615

## Block Diagram

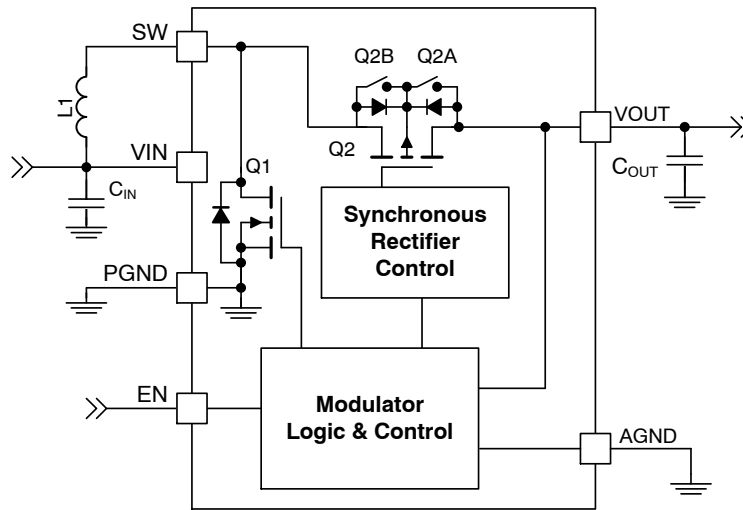


Figure 2. IC Block Diagram

Table 1. RECOMMENDED COMPONENTS

Component	Description	Vendor	Parameter	Typical Value	Unit
L1	20%, 5.3 A, 2016, 1.0 mm Height	DFE201610E-R47M TOKO	Inductance	470	nH
			DCR (Series R)	26	mΩ
C <sub>IN</sub>	20%, 6.3 V, X5R, 0402 (1005)	C1005X5R0J106M050BC TDK	Capacitance	10	μF
C <sub>OUT</sub>	20%, 10 V, X5R, 0603 (1608)	C1608X5R1A106K080AC TDK	Capacitance	10	μF

# FAN48615

## Pin Configuration

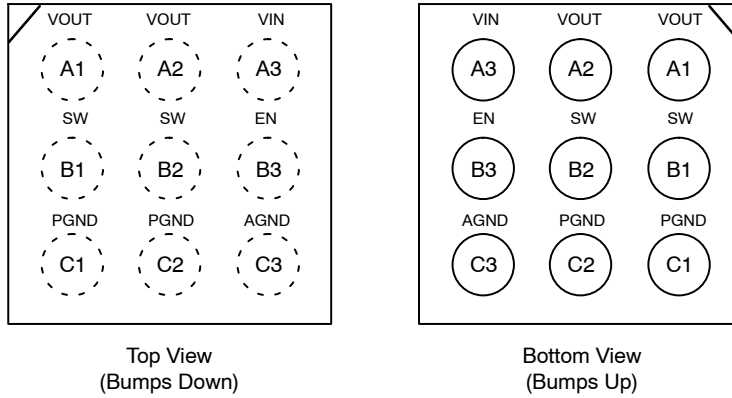


Figure 3. Pin Assignment

## Pin Definitions

Table 2. PIN DEFINITIONS

Pin #	Name	Description
A1	VOUT	<b>Output Voltage.</b> This pin is the output voltage terminal; connect directly to C <sub>OUT</sub> .
A2		
A3	VIN	<b>Input Voltage.</b> Connect to Li-Ion battery input power source and C <sub>IN</sub> .
B1	SW	<b>Switching Node.</b> Connect to inductor.
B2		
B3	EN	<b>Enable.</b> When this pin is HIGH, the circuit is enabled. After part is engaged, pin forces part into Forced-Pass-Through Mode when EN pin is pulled LOW.
C1	PGND	<b>Power Ground.</b> This is the power return for the IC. C <sub>OUT</sub> capacitor should be returned with the shortest path possible to these pins.
C2		
C3	AGND	<b>Analog Ground.</b> This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin – connect to PGND at a single point.

**Table 3. ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter		Min	Max	Unit
V <sub>IN</sub>	Voltage on VIN Pin		-0.3	6.0	V
V <sub>OUT</sub>	Voltage on VOUT Pin		-0.3	6.0	V
V <sub>SW</sub>	SW Node	DC	-0.3	6.0	V
		Transient: 10 ns, 3 MHz	-1.0	8.0	
V <sub>CC</sub>	Voltage on Other Pins		-0.3	6.0 <sup>(1)</sup>	V
ESD	Electrostatic Discharge Protection Level	Human Body Model, ANSI/ESDA/ JEDEC JS-001-2012	2.0		kV
		Charged Device Model, JESD22-C101	1.0		
T <sub>J</sub>	Junction Temperature		-40	150	°C
T <sub>STG</sub>	Storage Temperature		-65	150	°C
T <sub>L</sub>	Lead Soldering Temperature, 10 Seconds			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Lesser of 6.0 V or V<sub>IN</sub> + 0.3 V.

**Table 4. RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>IN</sub>	Supply Voltage for Boost & Auto Pass Through Operation <sup>(2)</sup>	2.7	5.5	V
I <sub>OUT</sub>	Maximum Output Current	1000		mA
T <sub>A</sub>	Ambient Temperature	-40	85	°C
T <sub>J</sub>	Junction Temperature	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. When V<sub>IN</sub> nears V<sub>OUT</sub> the part will automatically go into pass through mode, depending on load current.

**Table 5. THERMAL PROPERTIES**

Symbol	Parameter	Typical	Unit
θ <sub>JA</sub>	Junction-to-Ambient Thermal Resistance	50	°C/W

NOTE: Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards with vias in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature, T<sub>J(max)</sub>, at a given ambient temperature, T<sub>A</sub>.

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**Table 6. ELECTRICAL CHARACTERISTICS**

Recommended operating conditions, unless otherwise noted, circuit per Figure 1,  $V_{OUT} = 5.40\text{ V}$ . Typical, minimum and maximum values are given at  $V_{IN} = 3.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $-40^\circ\text{C}$  and  $+85^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Power Supply</b>						
$I_Q$	$V_{IN}$ Quiescent Current	$I_{OUT} = 0\text{ mA}$ , $EN = 1.8\text{ V}$ , No Switching		95		$\mu\text{A}$
		Forced Pass-Through $EN = 0\text{ V}$ , $V_{OUT} = V_{IN}$		3.5		
$V_{UVLO}$	Under-Voltage Lockout	$V_{IN}$ Rising		2.20		V
$V_{UVLO\_HYS}$	Under-Voltage Lockout Hysteresis			150		mV
<b>Inputs</b>						
$V_{IH}$	Enable HIGH Voltage		1.05			V
$V_{IL}$	Enable LOW Voltage				0.4	V
<b>Outputs</b>						
$V_{REG}$	Output Voltage Accuracy DC <sup>(3)</sup>	$2.7\text{ V} \leq V_{IN} \leq 4.5\text{ V}$	-2		+2	%
<b>Timing</b>						
$f_{SW}$	Switching Frequency	$I_{OUT} = 300\text{ mA}$	1.8	2.3	2.8	MHz
$t_{SS}^{(4)}$	EN HIGH to 95% of Regulation	$I_{OUT} = 150\text{ mA}$		440		$\mu\text{s}$
$t_{RST}^{(4)}$	FAULT Restart Timer			20		ms
<b>Power Stage</b>						
$R_{DS(ON)N}$	N-Channel Boost Switch $R_{DS(ON)}$			63		$\text{m}\Omega$
$R_{DS(ON)P}$	P-Channel Sync. Rectifier $R_{DS(ON)}$			52		$\text{m}\Omega$

3. DC  $I_{LOAD}$  from 0 to 1 A.  $V_{OUT}$  measured from mid-point of output voltage ripple. Effective capacitance of  $C_{OUT} \geq 2.2\ \mu\text{F}$ .

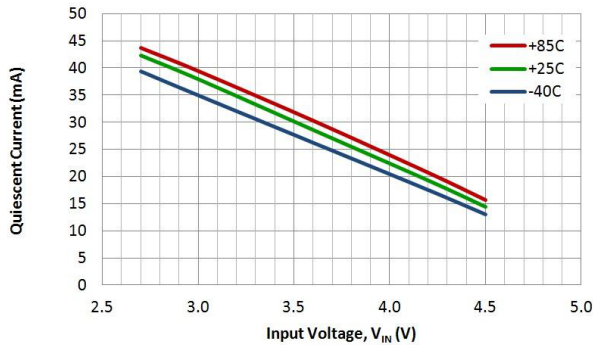
4. Guaranteed by design and characterization; not tested in production.

**Typical Performance Characteristics**

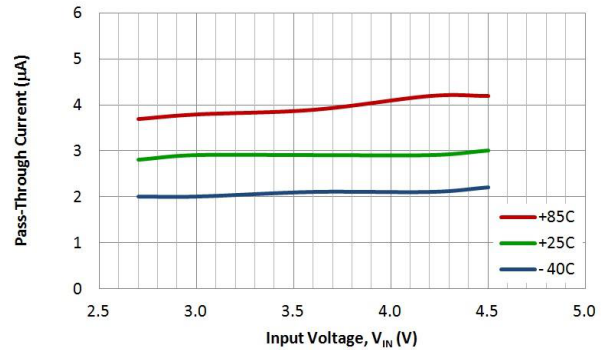
Unless otherwise specified;  $V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 5.40\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , and circuit according to Figure 1.

Components:  $C_{IN} = 10\ \mu\text{F}$  (0402, X5R, 6.3 V, C1005X5R0J106M050BC),  $C_{OUT} = 10\ \mu\text{F}$  (0603, X5R,

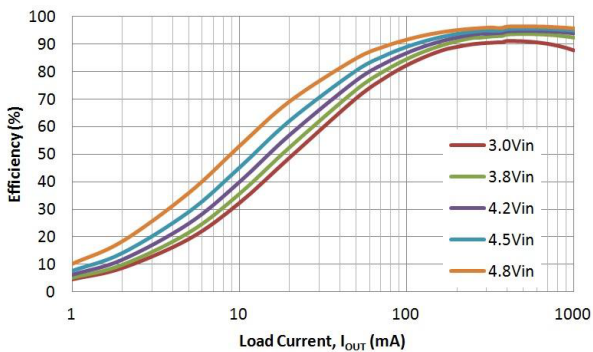
10 V, C1608X5R1A106K080AC),  $L1 = 470\text{ nH}$  (2016, 26 m $\Omega$ , DFE201610E-R47M ).



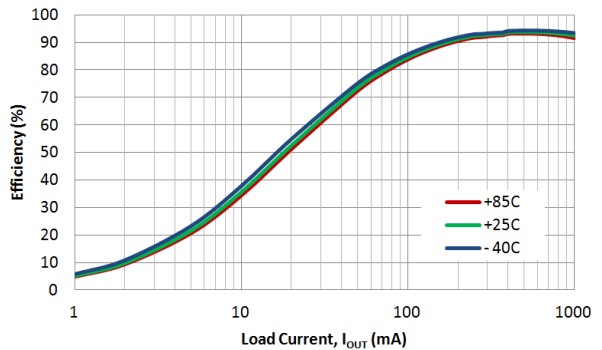
**Figure 4. Quiescent Current (Switching) vs. Input Voltage and Temperature**



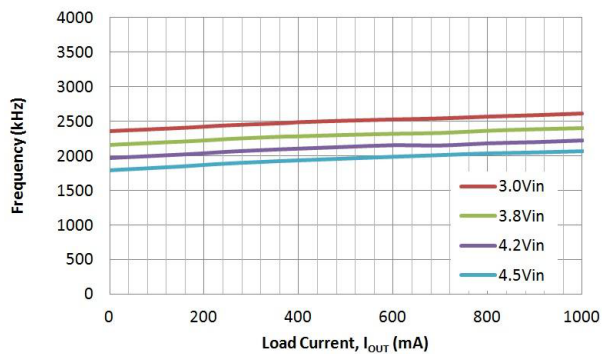
**Figure 5. Pass-Through Current vs. Input Voltage and Temperature**



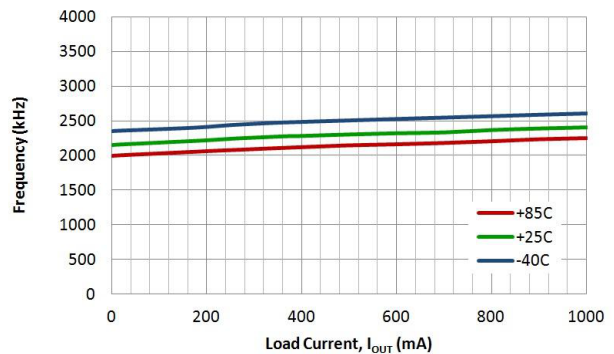
**Figure 6. Efficiency vs. Load Current and Input Voltage**



**Figure 7. Efficiency vs. Load Current and Temperature**



**Figure 8. Switching Frequency vs. Load Current and Input Voltage**



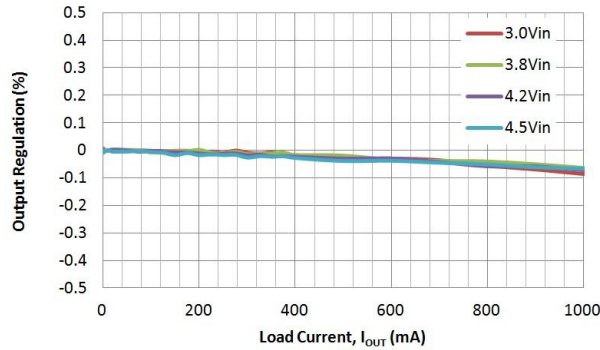
**Figure 9. Switching Frequency vs. Load Current and Temperature**

**Typical Performance Characteristics**

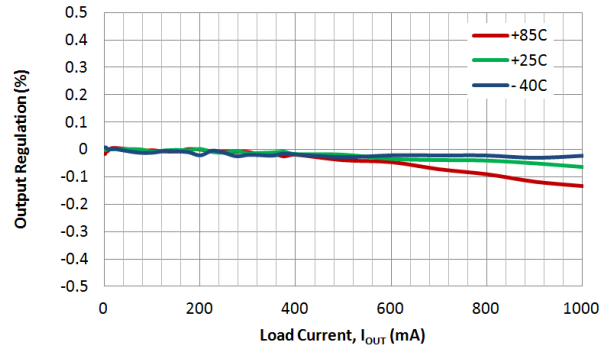
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Components:  $C_{IN} = 10\ \mu\text{F}$  (0402, X5R, 6.3 V, C1005X5R0J106M050BC),  $C_{OUT} = 10\ \mu\text{F}$  (0603, X5R,

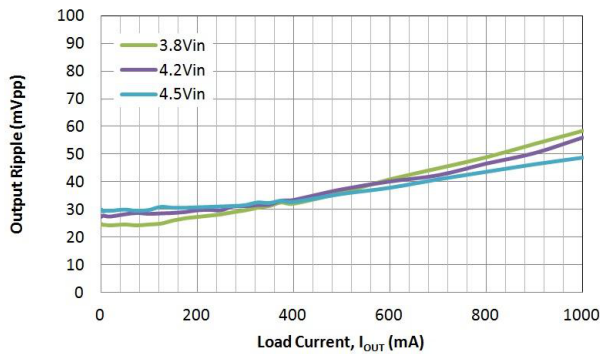
10 V, C1608X5R1A106K080AC),  $L1 = 470\text{ nH}$  (2016, 26 m $\Omega$ , DFE201610E-R47M ).



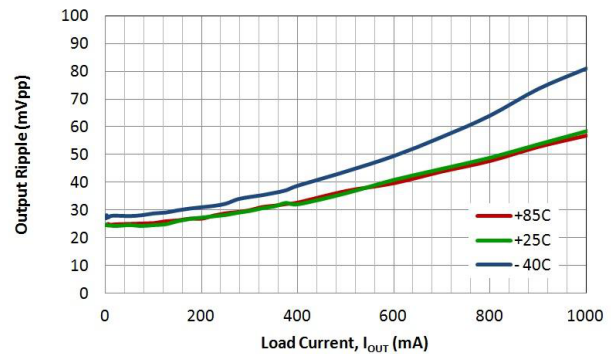
**Figure 10. Output Regulation vs. Load Current and Input Voltage**



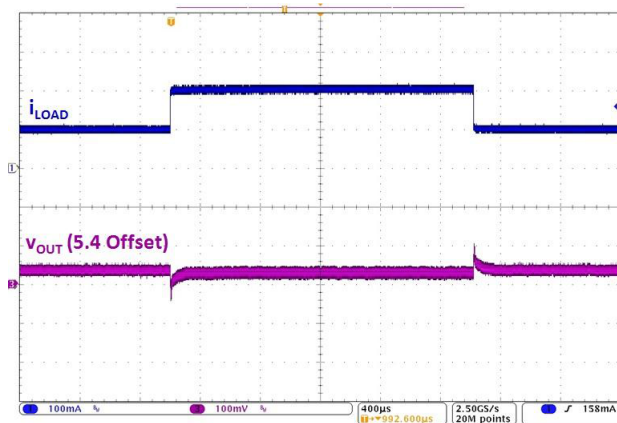
**Figure 11. Output Regulation vs. Load Current and Temperature**



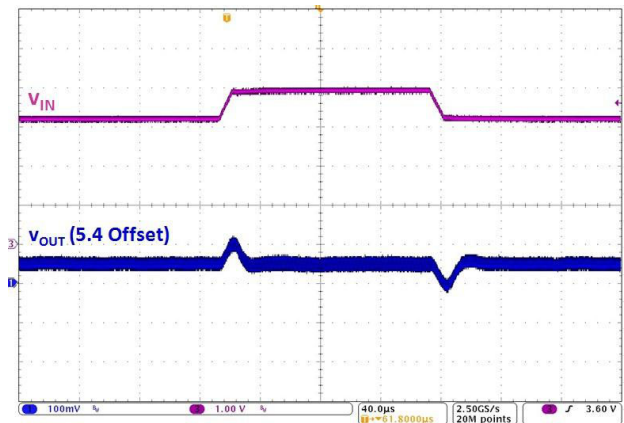
**Figure 12. Output Ripple vs. Load Current and Input Voltage**



**Figure 13. Output Ripple vs. Load Current and Temperature**



**Figure 14. Load Transient, 3.6  $V_{IN}$ , 100  $\leftrightarrow$  200 mA, 1  $\mu\text{s}$  Edge**



**Figure 15. Line Transient, 50 mA, 3.2 V  $\leftrightarrow$  3.9 V, 10  $\mu\text{s}$  Edge**

# FAN48615

## Typical Performance Characteristics

Unless otherwise specified;  $V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 5.40\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , and circuit according to Figure 1.

Components:  $C_{IN} = 10\ \mu\text{F}$  (0402, X5R, 6.3 V, C1005X5R0J106M050BC),  $C_{OUT} = 10\ \mu\text{F}$  (0603, X5R,

10 V, C1608X5R1A106K080AC),  $L1 = 470\ \text{nH}$  (2016, 26  $\text{m}\Omega$ , DFE201610E-R47M ).

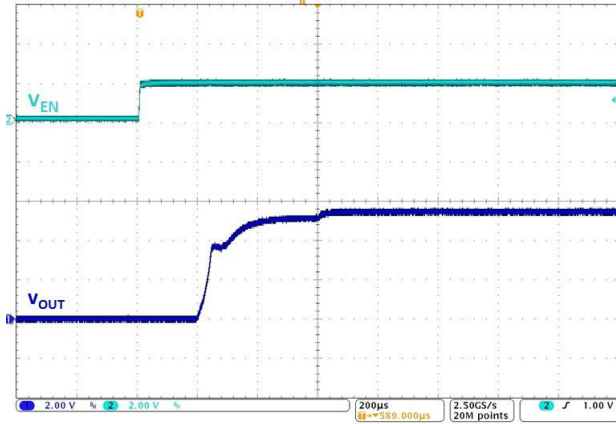


Figure 16. Startup, 150 mA Load

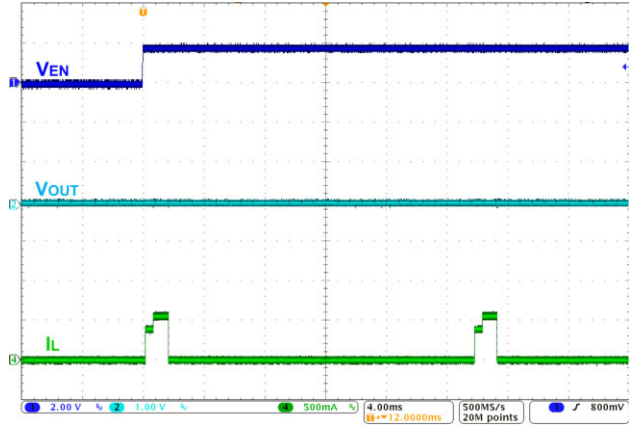


Figure 17. Fault Restart



**CIRCUIT DESCRIPTION**

FAN48615 is a synchronous PWM Only boost regulator. The regulator’s Pass-Through Mode automatically activates when VIN is above the boost regulator’s set point.

**Table 7. OPERATING MODES**

Mode	Description	Invoked When:
LIN	Linear Startup	$V_{IN} > V_{OUT}$
SS	Boost Soft-Start	$V_{IN} < V_{OUT} < V_{OUT(TARGET)}$
BST	Boost Operating Mode	$V_{OUT} = V_{OUT(TARGET)}$
PT	Pass-Through Mode	$V_{IN} > V_{OUT(TARGET)}$ or when EN is pulled LOW after initial startup

**Boost Mode Regulation**

The FAN48615 uses a current-mode modulator to achieve excellent transient response.

**Table 8. BOOST STARTUP SEQUENCE**

Start Mode	Entry	Exit	End Mode	Timeout (μs)
LIN1	$V_{IN} > V_{UVLO}$ , EN = 1	$V_{OUT} > V_{IN} - 300\text{ mV}$ Timeout	SS LIN2	512
LIN2	LIN1 Exit	$V_{OUT} > V_{IN} - 300\text{ mV}$ Timeout	SS FAULT	1024
SS	LIN1 or LIN2 Exit	$V_{OUT} = V_{OUT(TARGET)}$ Overload Timeout	BST FAULT	64

**LIN Mode**

When EN is HIGH and  $V_{IN} > V_{UVLO}$ , the regulator first attempts to bring  $V_{OUT}$  within 300 mV of  $V_{IN}$  by using the internal fixed-current source from VIN (Q2). The current is limited to the LIN1 set point.

If  $V_{OUT}$  reaches  $V_{IN}-300\text{ mV}$  during LIN1 Mode, the SS Mode is initiated. Otherwise, LIN1 times out after 512 μs and LIN2 Mode is entered.

In LIN2 Mode, the current source is incremented. If  $V_{OUT}$  fails to reach  $V_{IN}-300\text{ mV}$  after 1024 μs, a fault condition is declared and the device waits 20 ms to attempt an automatic restart.

**Soft-Start (SS) Mode**

Upon the successful completion of LIN Mode ( $V_{OUT} \geq V_{IN}-300\text{ mV}$ ), the regulator begins switching with boost pulses current limited to 50% of nominal level.

During SS Mode, if  $V_{OUT}$  fails to reach regulation during the SS ramp sequence for more than 64 μs, a fault is declared. If large  $C_{OUT}$  is used, the reference is automatically stepped slower to avoid excessive input current draw.

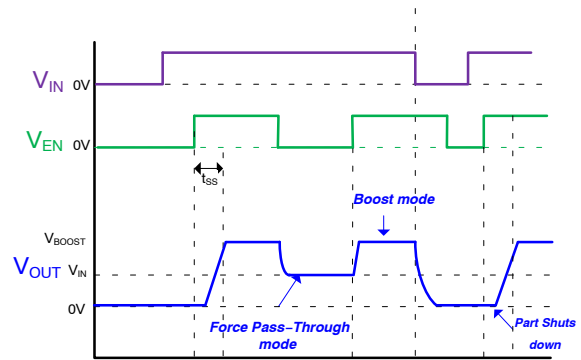
**Boost (BST) Mode**

This is a normal operating mode of the regulator.

**Pass-Through Mode**

The device allows the user to force the device in Forced Pass-Through Mode through the EN pin. If the EN pin is pulled HIGH, the device starts operating in Boost Mode. Once the EN pin is pulled LOW, the device is forced into Pass-Through Mode. To disable the device, the input supply voltage must be removed. The device cannot startup in Forced Pass-Through Mode (see Figure 18). During startup, keep the EN pulled HIGH for at least 350 μs before pulling it LOW in order to make sure that the device enters Pass-Through Mode reliably.

In normal operation, the device automatically transitions from Boost Mode to Pass-Through Mode if VIN goes above the target  $V_{OUT}$ . In Pass-Through Mode, the device fully enhances Q2 to provide a very low impedance path from VIN to VOUT. Entry to the Pass-Through Mode is triggered by condition where  $V_{IN} > V_{OUT}$  and no switching has occurred during the past 5 μs. To soften the entry into Pass-Through Mode, Q2 is driven as a linear current source for the first 5 μs. Pass-Through Mode exit is triggered when  $V_{OUT}$  reaches the target  $V_{OUT}$  voltage. During Automatic Pass-Through Mode, the device is short-circuit protected by a voltage comparator tracking the voltage drop from  $V_{IN}$  to  $V_{OUT}$ ; if the drop exceeds 300 mV, a fault is declared.



**Figure 18. Pass-Through Profile**

**Current Limit Protection**

The FAN48615 has valley current limit protection in case of overload situations. The valley current limit will prevent high current from causing damage to the IC and the inductor. The current limit is halved during soft-start.

When starting into a fault condition, the input current will be limited by LIN1 and LIN2 current threshold.

**Fault State**

The regulator enters Fault State under any of the following conditions:

- $V_{OUT}$  fails to achieve the voltage required to advance from LIN Mode to SS Mode.
- $V_{OUT}$  fails to achieve the voltage required to advance from SS Mode to BST Mode.

- Boost current limit triggers for 2 ms during BST Mode.
- $V_{IN} - V_{OUT} > 300 \text{ mV}$ ; this fault can occur only after successful completion of the soft-start sequence.
- $V_{IN} < V_{UVLO}$

Once a fault is triggered, the regulator stops switching and presents a high-impedance path between VIN and VOUT. After waiting 20 ms, an automatic restart is attempted.

**Over-Temperature**

The regulator shuts down if the die temperature exceeds 150°C and restarts when the IC cools by ~20°C.

**Layout Recommendation**

The layout recommendations below highlight various top-copper pours by using different colors.

To minimize spikes at VOUT, COUT must be placed as close as possible to PGND and VOUT, as shown in Figure 19.

For best thermal performance, maximize the pour area for all planes other than SW. The ground pour, especially, should fill all available PCB surface area and be tied to internal layers with a cluster of thermal vias.

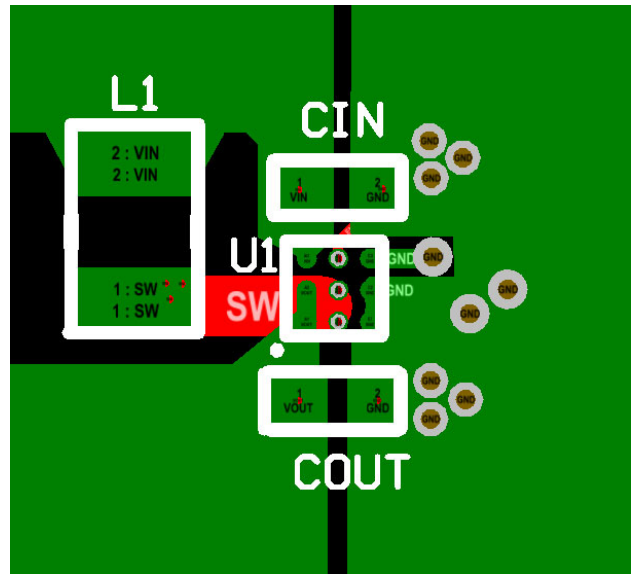


Figure 19. Recommended Layout

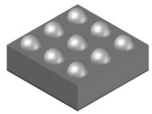
**Table 9. PRODUCT-SPECIFIC PACKAGE DIMENSIONS**

The following information applies to the WLCSP package dimensions on the next page.

Product	D (mm)	E (mm)	X (mm)	Y (mm)
FAN48615UC08X	1.215 ± 0.030	1.215 ± 0.030	0.2075	0.2075

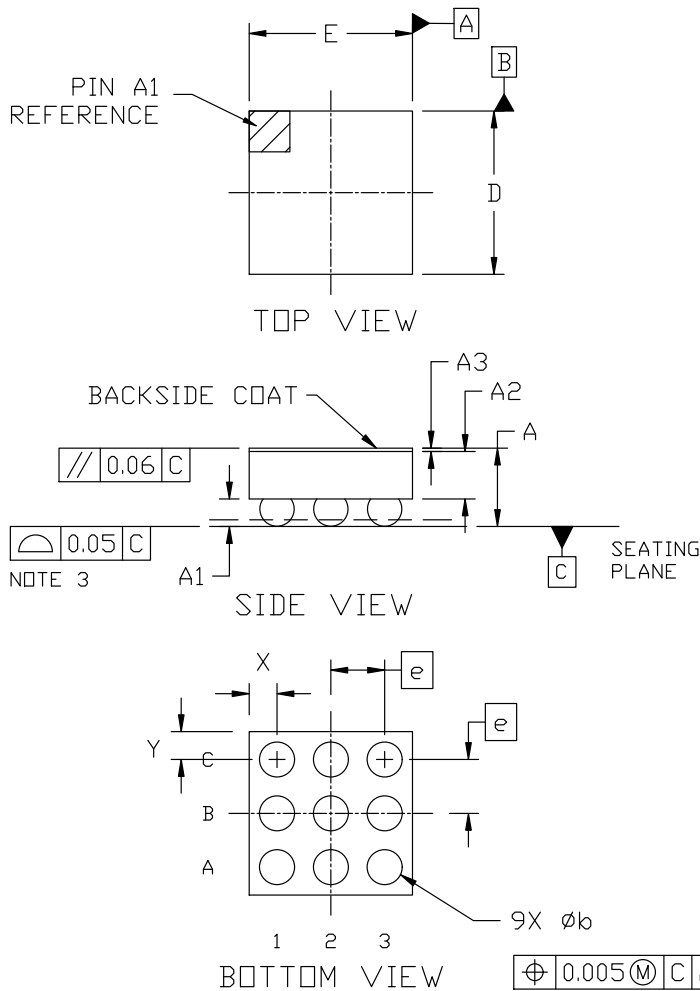
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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**WLCSP9 1.215x1.215x0.581**  
CASE 567QW  
ISSUE B

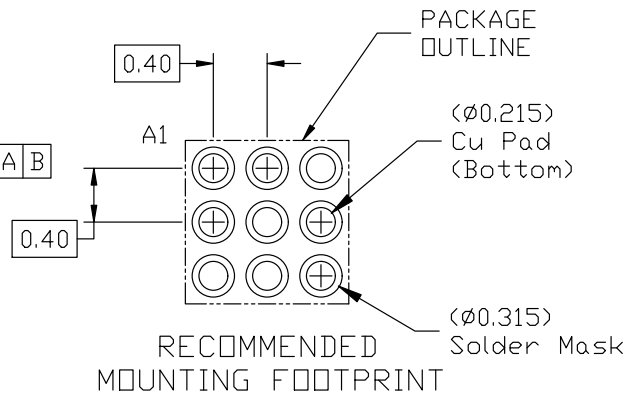
DATE 24 FEB 2023



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION  $b$  IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.

DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.542	0.581	0.620
A1	0.183	0.203	0.223
A2	0.335	0.353	0.371
A3	0.022	0.025	0.027
$b$	0.24	0.26	0.28
D	1.185	1.215	1.245
E	1.185	1.215	1.245
$e$	0.400 BSC		
X	0.208 REF		
Y	0.208 REF		



\* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON13355G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>WLCSP9 1.215x1.215x0.581</b>	<b>PAGE 1 OF 1</b>

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