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# FAN7361, FAN7362 High-Side Gate Driver

## Features

- Floating Channel Designed for Bootstrap Operation to +600V
- Typically 250mA/500mA Sourcing/Sinking Current Driving Capability
- Common-Mode dv/dt Noise Canceling Circuit
- $V_{CC}$  &  $V_{BS}$  Supply Range from 10V to 20V
- UVLO Function for  $V_{BS}$
- Output In-phase with Input Signal
- 8-SOP

## Applications

- PDP Scan Driver
- Motor Control
- SMPS
- Electronic Ballast

## Description

The FAN7361/FAN7362, a monolithic high-side gate drive IC, can drive MOSFETs and IGBTs that operate up to +600V. Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level shifting circuit offers high-side gate driver operation up to  $V_{GS}=9.8V$  typ. for  $V_{BS}=15V$ .

The UVLO circuit prevents malfunction when  $V_{BS}$  is lower than the specified threshold voltage. Output drivers typically source/sink 250mA/500mA, respectively, which is suitable for fluorescent lamp ballast, PDP scan driver, motor control and so on.

8-SOP



## Ordering Information

Part Number	Package	Operating Temperature Range	Eco Status	Packing Method
FAN7361M <sup>(1)</sup>	8-SOP	-40°C ~ 125°C	RoHS	Tube
FAN7361MX <sup>(1)</sup>				Tape & Reel
FAN7362M <sup>(1)</sup>				Tube
FAN7362MX <sup>(1)</sup>				Tape & Reel

### Note:

1. These devices passed wave soldering test by JESD22A-111.



For Fairchild's definition of Eco Status, please visit: [http://www.fairchildsemi.com/company/green/rohs\\_green.html](http://www.fairchildsemi.com/company/green/rohs_green.html).

Typical Application Circuit

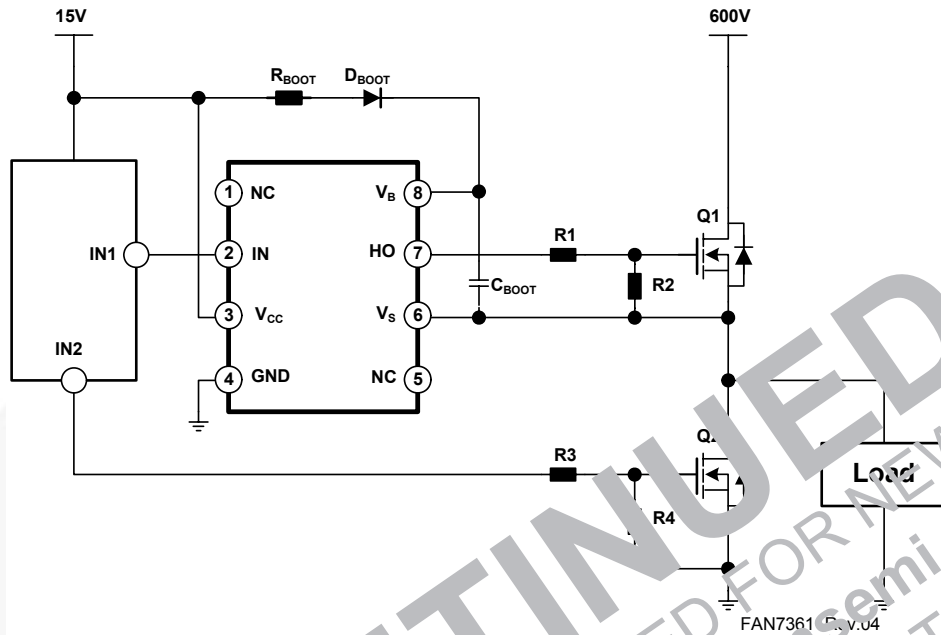
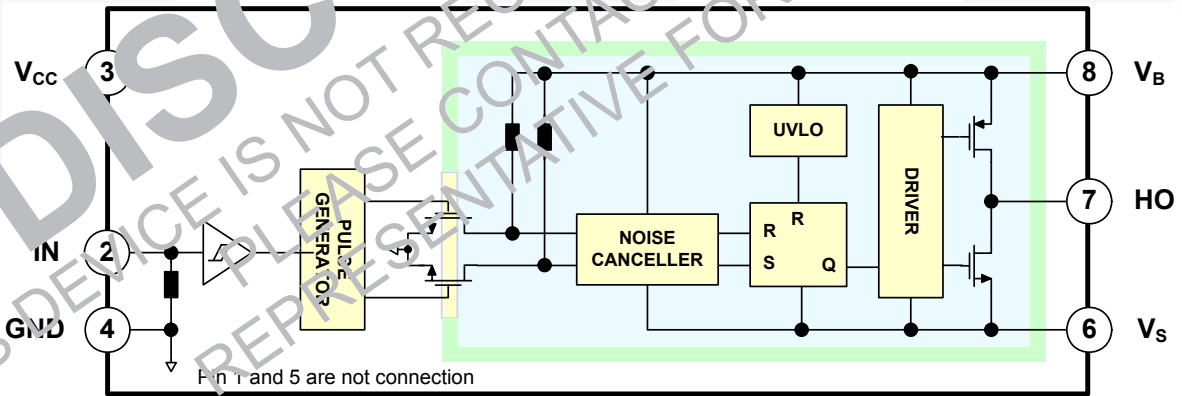


Figure 1. Typical Application Circuit

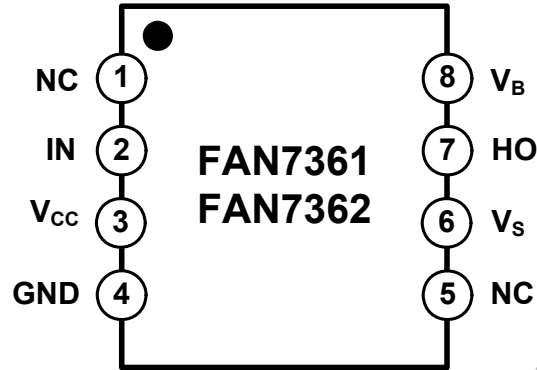
Internal Block Diagram



FAN7361 Rev.04

Figure 2. Functional Block Diagram

### Pin Assignments



FAN7361 Rev.04

Figure 3. Pin Configuration (Top View)

### Pin Definitions

Pin	Name	Function/ Description
1	NC	No Connection
2	IN	Logic Input / High-Side Gate Driver Output
3	V <sub>CC</sub>	Supply Voltage
4	GND	Logic Ground
5	NC	No Connection
6	V <sub>S</sub>	High-Voltage Floating Supply Return
7	HO	High-Side Driver Output
8	V <sub>B</sub>	High-Side Floating Supply

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A=25^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Characteristics	Min.	Max.	Unit
$V_S$	High-Side Offset Voltage	$V_B-25$	$V_B+0.3$	V
$V_B$	High-Side Floating Supply Voltage	-0.3	625	
$V_{HO}$	High-Side Floating Output Voltage	$V_S-0.3$	$V_B+0.3$	
$V_{CC}$	Logic Fixed Supply Voltage	-0.3	25	
$V_{IN}$	Logic Input Voltage	-0.3	$V_{CC}+0.3$	
$dV_S/dt$	Allowable Offset Voltage Slew Rate		$\pm 10$	V/ns
$P_D^{(2)(3)(4)}$	Power Dissipation		0.625	W
$\theta_{JA}$	Thermal Resistance, Junction-to-Ambient		200	$^{\circ}\text{C}/\text{W}$
$T_J$	Junction Temperature		150	$^{\circ}\text{C}$
$T_S$	Storage Temperature		+150	$^{\circ}\text{C}$
$T_A$	Ambient Temperature	-40	+125	$^{\circ}\text{C}$

### Notes:

- Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 class epoxy material).
- Refer to the following standards:
  - JESD51-2: Integral circuits thermal test method environmental conditions - Natural convection
  - JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
- Do not exceed  $P_D$  under any circumstances.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_B$	High-Side Floating Supply Voltage	$V_S+10$	$V_S+20$	V
$V_S$	High-Side Floating Supply Offset Voltage	$6-V_{CC}$	600	
$V_{HO}$	High-Side Output Voltage	$V_S$	$V_B$	
$V_{IN}$	Logic Input Voltage	GND	$V_{CC}$	
$V_{CC}$	Logic Supply Voltage	10	20	

## Electrical Characteristics

$V_{BIAS}(V_{CC}, V_{BS})=15.0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified. The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to GND. The  $V_O$  and  $I_O$  parameters are referenced to  $V_S$  and are applicable to the respective output HO.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit	
$V_{BSUV+}$	$V_{BS}$ Supply Under-Voltage Positive Going Threshold	$V_{BS}=\text{Sweep}$	FAN7361	8.2	9.2	10.2	V
			FAN7362	7.6	8.6	9.6	
$V_{BSUV-}$	$V_{BS}$ Supply Under-Voltage Negative Going Threshold	$V_{BS}=\text{Sweep}$	FAN7361	7.4	8.6	9.2	
			FAN7362	7.2	8.2	9.2	
$V_{BSHYS}$	$V_{BS}$ Supply Under-Current Lockout Hysteresis	$V_{BS}=\text{Sweep}$	FAN7361		0.5		
			FAN7362		0.4		
$I_{LK}$	Offset Supply Leakage Current	$V_B=V_S=600V$			10		
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	$V_{IN}=0V$ or $5V$		50	80	$\mu A$	
$I_{QCC}$	Quiescent $V_{CC}$ Supply Current	$V_{IN}=0V$			75		
$I_{PBS}$	Operating $V_{BS}$ Supply Current	$C_L=1nF$ , $f=10kHz$		420	550		
$V_{IH}$	Logic "1" Input Voltage		FAN7361	2.6			V
			FAN7362	2.3			
$V_{IL}$	Logic "0" Input Voltage		FAN7361			1.0	
			FAN7362			0.8	
$V_{OH}$	High Level Output Voltage, $V_B-V_{HO}$	No load			0.1		
$V_{OL}$	Low Level Output Voltage, $V_{HC}$	No load			0.1		
$I_{IN+}$	Logic "1" Input Bias Current	$V_{IN}=5V$		50	90	$\mu A$	
$I_{IN-}$	Logic "0" Input Bias Current	$V_{IN}=0V$		1.0	2.0		
$I_{O+}$	Output High Short Circuit Pulse Current	$V_{HO}=0V$ , $V_{IN}=5V$ , $PW \leq 10\mu s$	200	250		mA	
$I_{O-}$	Output Low Short Circuit Pulse Current	$V_{HO}=15V$ , $V_{IN}=0V$ , $PW \leq 10\mu s$	400	500			
$V_S$	Allowable Negative $V_S$ Pin Voltage for IN Signal Propagation to HO			-9.8	-7.0	V	

## Dynamic Electrical Characteristics

$V_{BIAS}(V_{CC}, V_{BS})=15.0V$ ,  $V_S=GND$ ,  $C_L=1000pF$  and  $T_A = 25^\circ C$ , unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
$t_{on}$	Turn-on Propagation Delay	$V_S=0V$		120	200	ns
$t_{off}$	Turn-off Propagation Delay <sup>(5)</sup>	$V_S=0V$ or $600V$		90	180	
$t_r$	Turn-on Rise Time			70	160	
$t_f$	Turn-off Fall Time			30	100	

### Note:

5. This parameter guaranteed by design.

Typical Characteristics

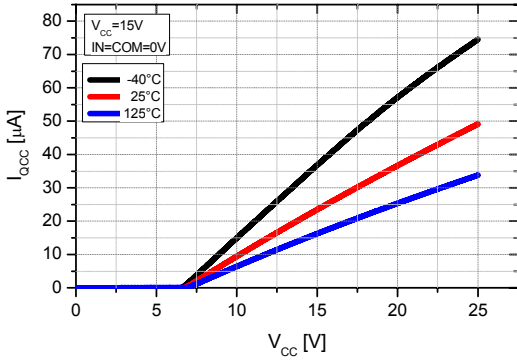


Figure 4.  $I_{QCC}$  vs. Supply Voltage

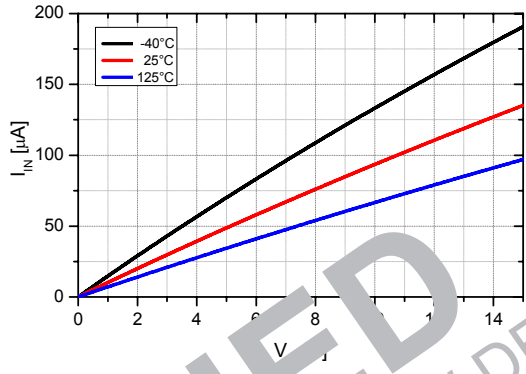


Figure 5. Output Base Current vs. Input Voltage

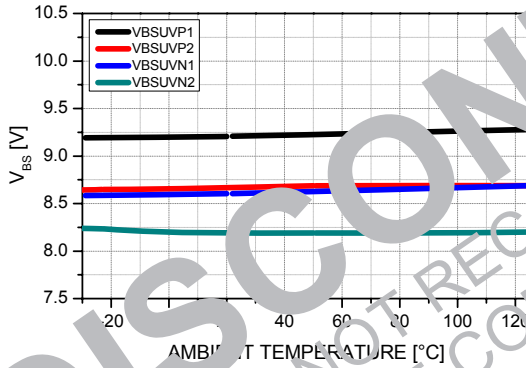


Figure 6.  $V_{GS}$  (V<sub>LO</sub>) vs. Temp.

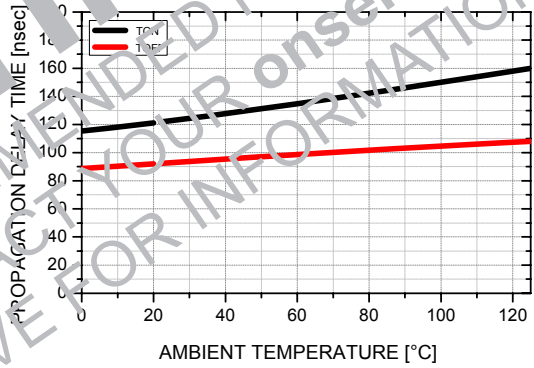


Figure 7. Turn On/Off Propagation Time vs. Temp.

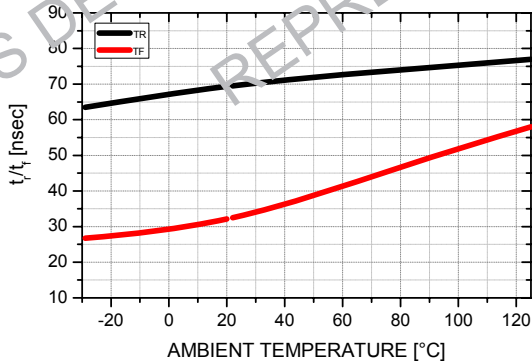


Figure 8. Rising/Falling Time vs. Temp.

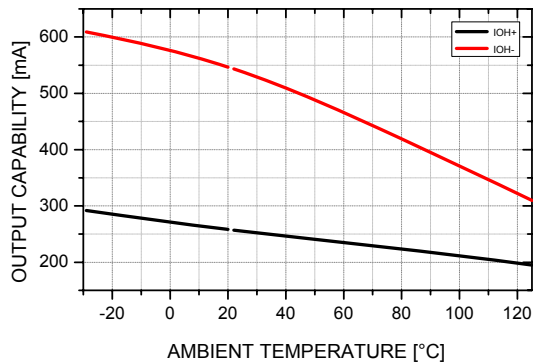


Figure 9. Output Sinking/Sourcing Current vs. Temp.



### Switching Time Definition

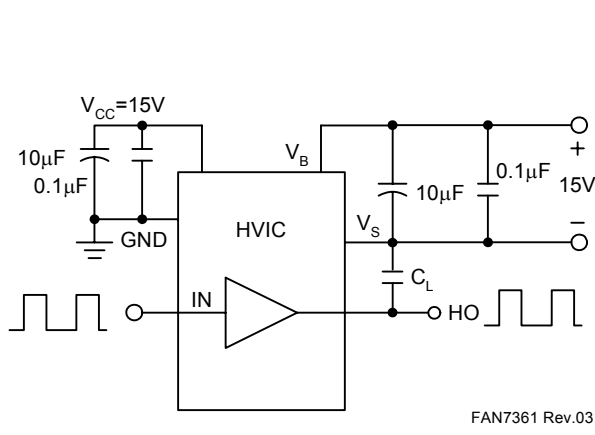


Figure 10. Switching Time Test Circuit

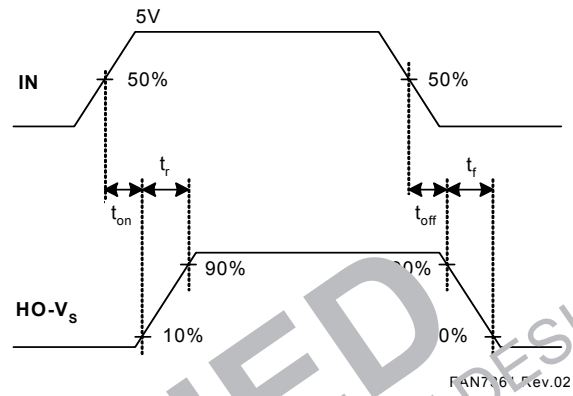


Figure 11. Input Output Timing Diagram

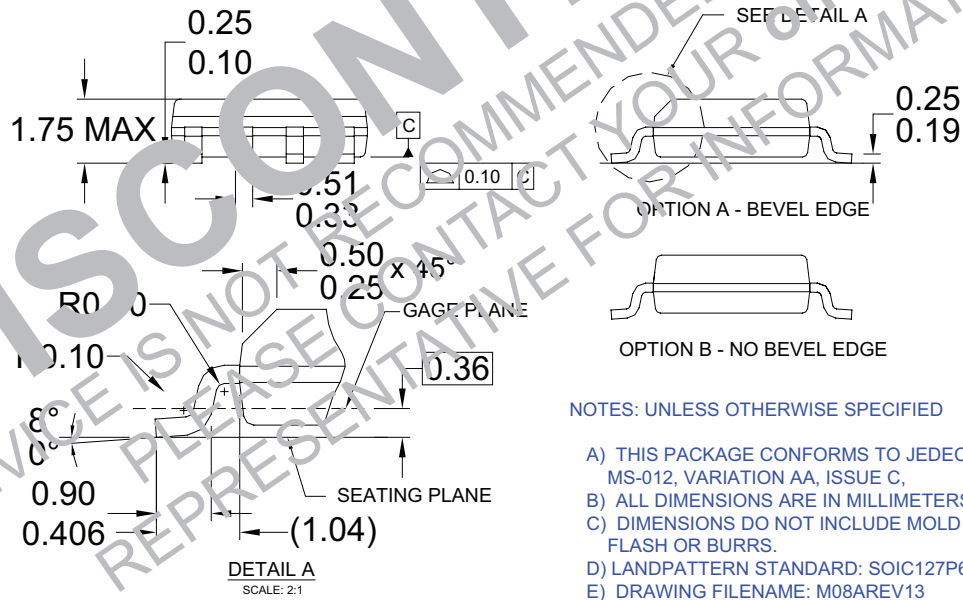
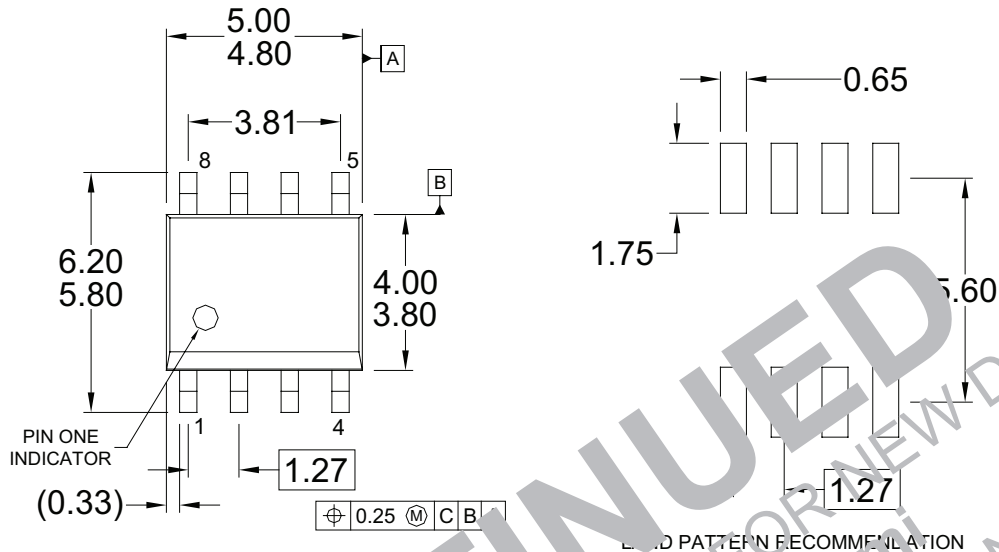
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- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
- E) DRAWING FILENAME: M08AREV13

Figure 12. 8-Lead Small Outline Package (SOP)

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