

MOSFET – Single, P-Channel, Logic Level, POWERTRENCH®

FDC658P

General Description

This P-Channel Logic Level MOSFET is produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance. These devices are well suited for notebook computer applications: load switching and power management, battery charging circuits, and DC/DC conversion.

Features

- -4 A, -30 V
 - ◆ $R_{DS(ON)} = 0.050 \Omega @ V_{GS} = -10 \text{ V}$
 - ◆ $R_{DS(ON)} = 0.075 \Omega @ V_{GS} = -4.5 \text{ V}$
- Low Gate Charge (8 nC Typical)
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- SUPERSOT™ -6 Package: Small Footprint (72% Smaller than Standard SO-8); Low Profile (1 mm Thick)
- This is a Pb-Free Device

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage – Continuous	± 20	V
I_D	Drain Current – Continuous (Note 1a) – Pulsed	-4	A
		-20	
P_D	Maximum Power Dissipation (Note 1a) (Note 1b)	1.6	W
		0.8	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

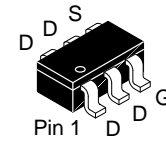
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Case (Note 1)	30	$^\circ\text{C}/\text{W}$

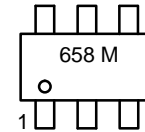
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
 - $78^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz Cu on FR-4 board.
 - $156^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz Cu on FR-4 board.

V_{DSS}	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
-30 V	$0.05 \Omega @ -10 \text{ V}$	-4 A
	$0.075 \Omega @ -4.5 \text{ V}$	



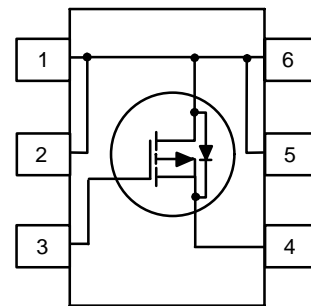
TSOT23 6-Lead
(SUPERSOT-6)
CASE 419BL

MARKING DIAGRAM



658 = Specific Device Code
M = Date Code

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
FDC658P	TSOT23-6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FDC658P

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = -250 μA	-30	-	-	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	I _D = -250 μA, Referenced to 25°C	-	-22	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24 V, V _{GS} = 0 V	-	-	-1	μA
		V _{DS} = -24 V, V _{GS} = 0 V, T _J = 55°C	-	-	-10	μA
I _{GSSF}	Gate – Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V	-	-	100	nA
I _{GSSR}	Gate – Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V	-	-	-100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250 μA	-1	-1.7	-3	V
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Temp. Coefficient	I _D = -250 μA, Referenced to 25°C	-	4.1	-	mV/°C
R _{DS(ON)}	Static Drain–Source On–Resistance	V _{GS} = -10 V, I _D = -4.0 A	-	0.041	0.05	Ω
		V _{GS} = -10 V, I _D = -4.0 A, T _J = 125°C	-	0.058	0.08	
		V _{GS} = -4.5 V, I _D = -3.4 A	-	0.06	0.075	
I _{D(on)}	On–State Drain Current	V _{GS} = -10 V, V _{DS} = -5 V	-20	-	-	A
g _{FS}	Forward Transconductance	V _{DS} = -5 V, I _D = -4 A	-	9	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -15 V, V _{GS} = 0 V, f = 1.0 MHz	-	750	-	pF
C _{oss}	Output Capacitance		-	220	-	pF
C _{rss}	Reverse Transfer Capacitance		-	100	-	pF

SWITCHING CHARACTERISTICS (Note 2)

t _{D(on)}	Turn – On Delay Time	V _{DD} = -15 V, I _D = -1 A, V _{GS} = -10 V, R _{GEN} = 6 Ω	-	12	22	ns
t _r	Turn – On Rise Time		-	14	25	ns
t _{D(off)}	Turn – Off Delay Time		-	24	38	ns
t _f	Turn – Off Fall Time		-	16	27	ns
Q _g	Total Gate Charge	V _{DS} = -15 V, I _D = -4.0 A, V _{GS} = -5 V	-	8	12	nC
Q _{gs}	Gate–Source Charge		-	1.8	-	nC
Q _{gd}	Gate–Drain Charge		-	3	-	nC

DRAIN–SOURCE DIODE CHARACTERISTICS

I _S	Continuous Source Diode Current	-	-	-1.3	A	
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -1.3 A (Note 2)	-	-0.76	-1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

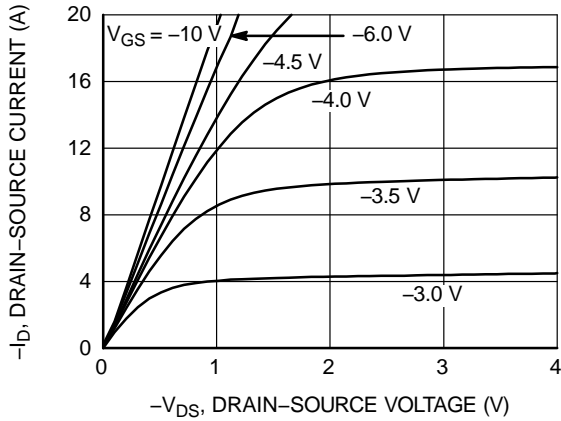


Figure 1. On-Region Characteristics

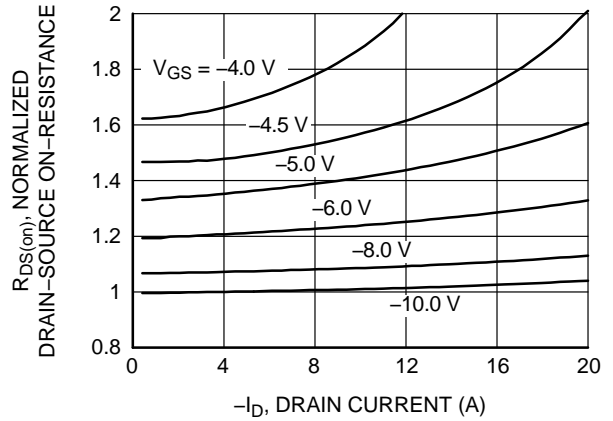


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

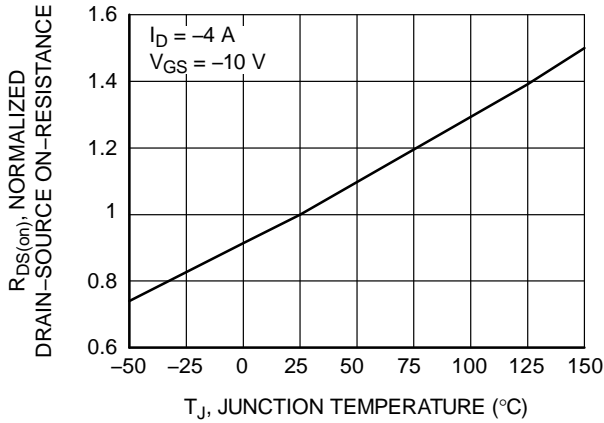


Figure 3. On-Resistance Variation with Temperature

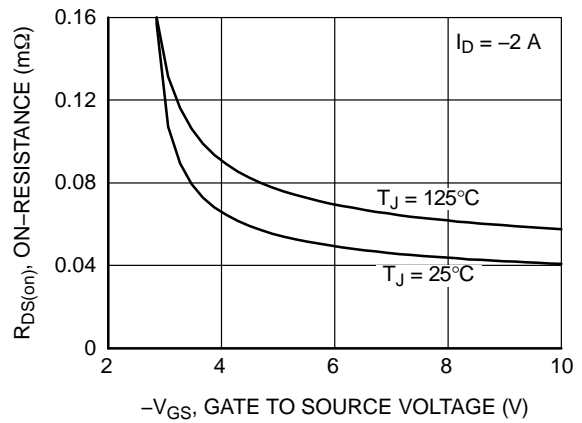


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

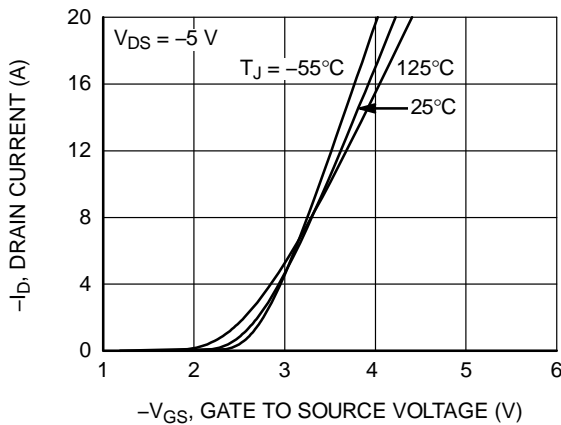


Figure 5. Transfer Characteristics

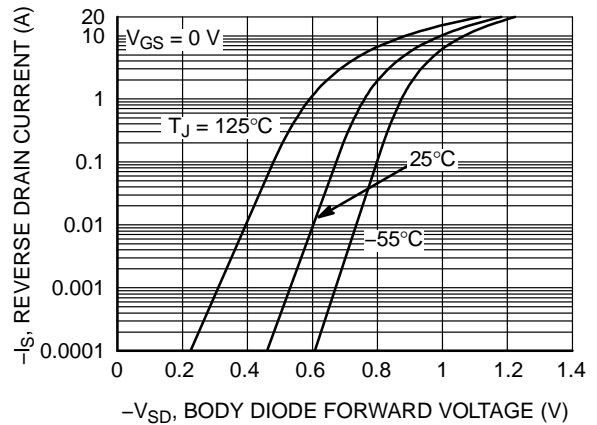


Figure 6. Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

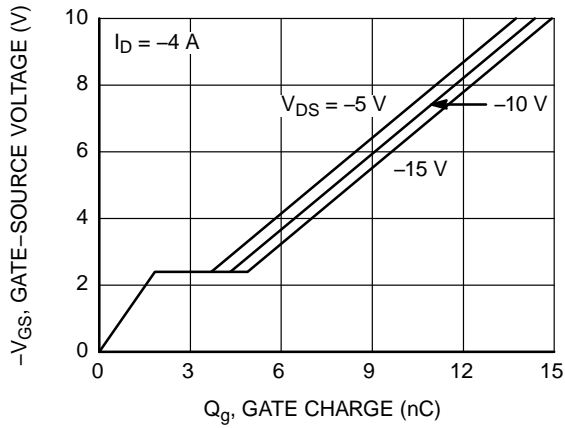


Figure 7. Gate Charge Characteristics

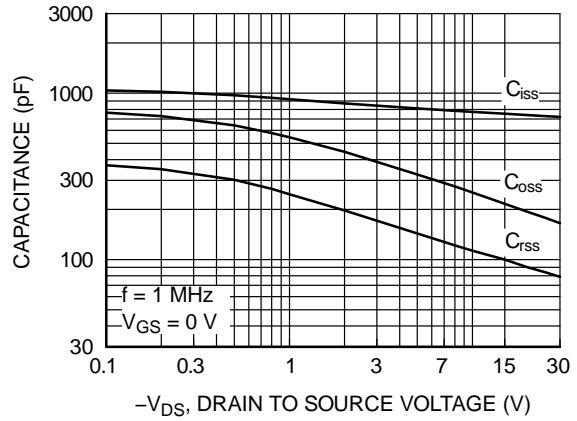


Figure 8. Capacitance Characteristics

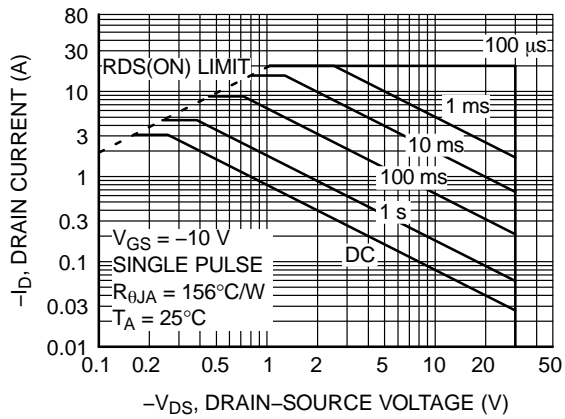


Figure 9. Maximum Safe Operating Area

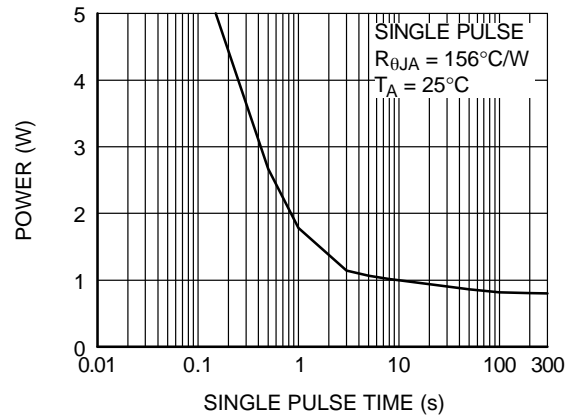


Figure 10. Single Pulse Maximum Power Dissipation

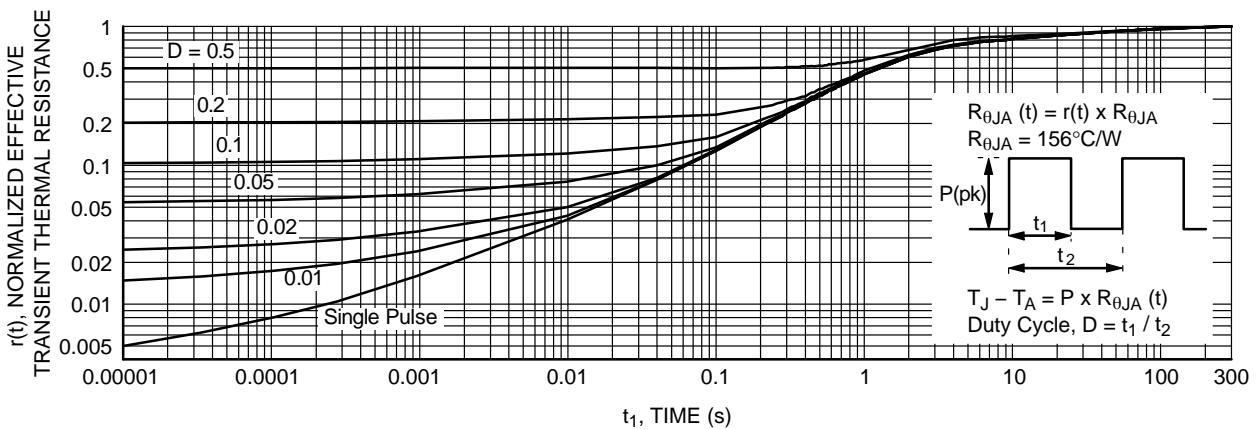


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

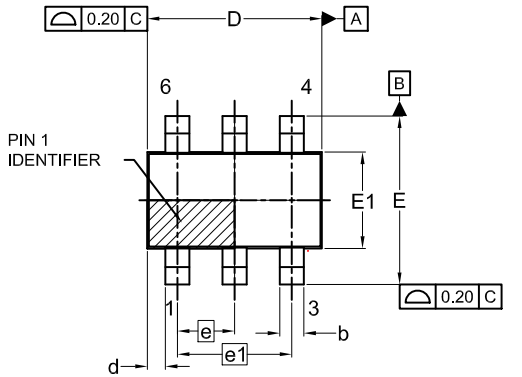
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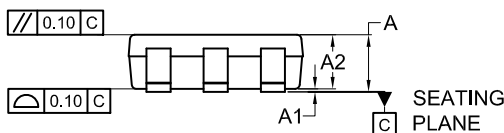
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SCALE 2:1

TSOT23 6-Lead
CASE 419BL
ISSUE A

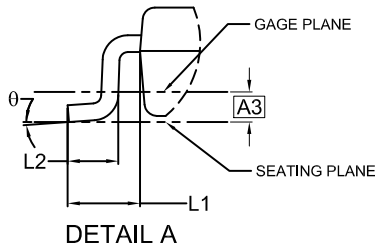
DATE 31 AUG 2020



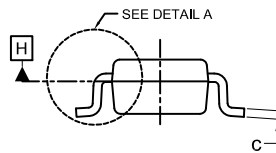
TOP VIEW



FRONT VIEW

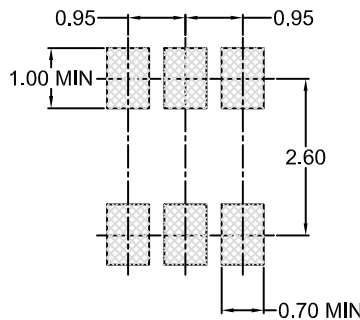


DETAIL A



SIDE VIEW

SYMM
⌀



LAND PATTERN
RECOMMENDATION

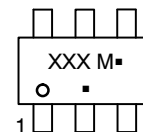
*FOR ADDITIONAL INFORMATION ON OUR
Pb-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR
SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
⌀	0°	--	10°

GENERIC
MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TSOT23 6-Lead	PAGE 1 OF 1

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