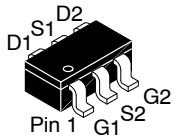
MOSFET – Dual, N-Channel, Shielded Gate, POWERTRENCH®

100 V, 1.2 A, 350 mΩ

FDC8602

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
100 V	350 mΩ @ 10 V	1.2 A
	575 mΩ @ 6 V	



TSOT23 6−Lead
(SUPERSOT™ −6)
CASE 419BL

General Description

This N−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for $R_{DS(on)}$, switching performance and ruggedness.

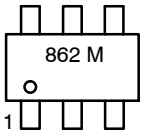
Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 350 mΩ at V_{GS} = 10 V, I_D = 1.2 A
- Max $R_{DS(on)}$ = 575 mΩ at V_{GS} = 6 V, I_D = 0.9 A
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- Fast Switching Speed
- 100% UIL Tested
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Applications

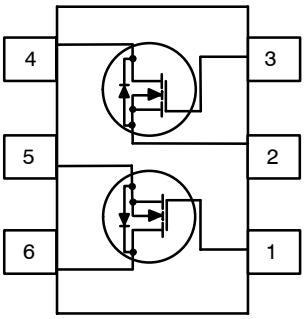
- Load Switch
- Synchronous Rectifier

MARKING DIAGRAM



862 = Specific Device Code
M = Date Code

PIN ASSIGNMENT



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current: Continuous (Note 1a) Pulsed	 1.2 5	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	1.5	mJ
P_D	Power Dissipation: (Note 1a) (Note 1b)	 0.96 0.69	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
FDC8602	TSOT23 6−Lead (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	60	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	130	

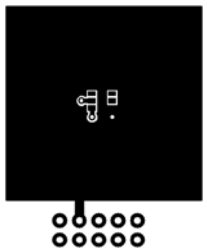
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	73	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	3.2	4	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	–8	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 1.2 A	–	285	350	mΩ
		V_{GS} = 6 V, I_D = 0.9 A	–	409	575	
		V_{GS} = 10 V, I_D = 1.2 A, T_J = 125°C	–	489	600	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 1.2 A	–	1.3	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	–	53	70	pF
C_{oss}	Output Capacitance		–	17	25	pF
C_{rss}	Reverse Transfer Capacitance		–	0.8	5	pF
R_g	Gate Resistance		–	1.6	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 1.2 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	3.5	10	ns
t_r	Rise Time		–	1.7	10	ns
$t_{d(off)}$	Turn-Off Delay Time		–	5.4	11	ns
t_f	Fall Time		–	2.3	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_D = 1.2 A	–	1.2	2	nC
		V_{GS} = 0 V to 5 V, V_{DD} = 50 V, I_D = 1.2 A	–	0.6	1	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 50 V, I_D = 1.2 A	–	0.4	–	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 50 V, I_D = 1.2 A	–	0.4	–	nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.2 A (Note 2)	–	0.86	1.3	V
t_{rr}	Reverse Recovery Time	I_F = 1.2 A, di/dt = 100 A/μs	–	27	43	ns
Q_{rr}	Reverse Recovery Charge		–	12	21	nC

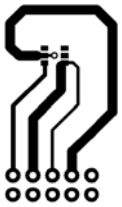
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 130°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 180°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C; N−ch: L = 3 mH, I_{AS} = 1 A, V_{DD} = 100 V, V_{GS} = 10 V.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

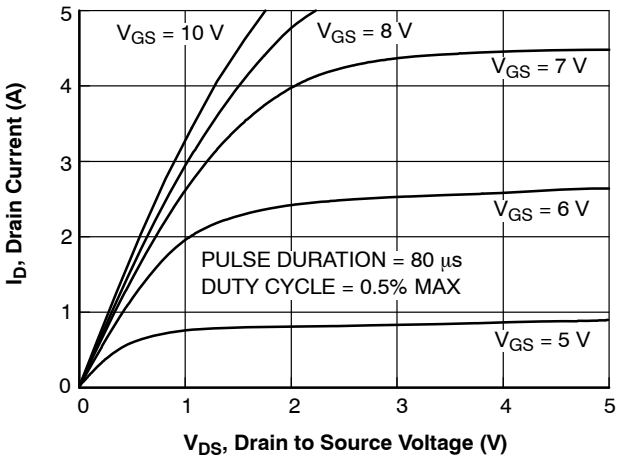


Figure 1. On Region Characteristics

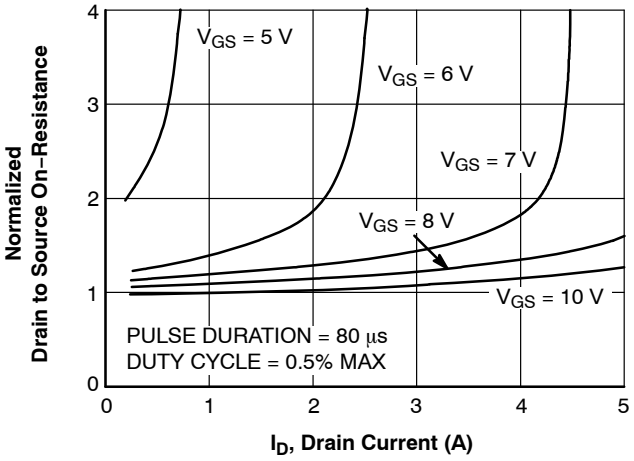


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

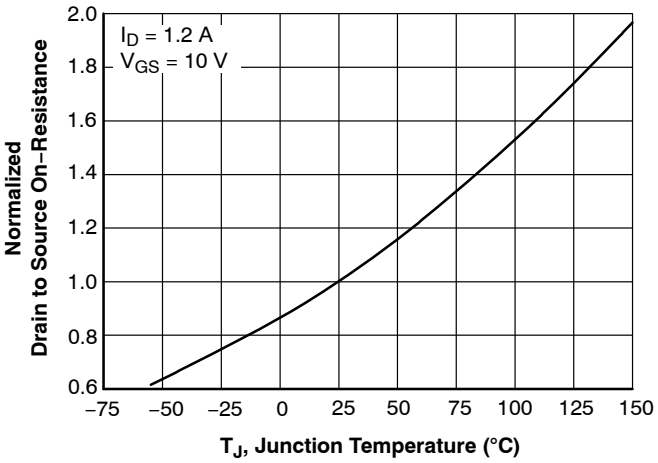


Figure 3. Normalized On Resistance vs. Junction Temperature

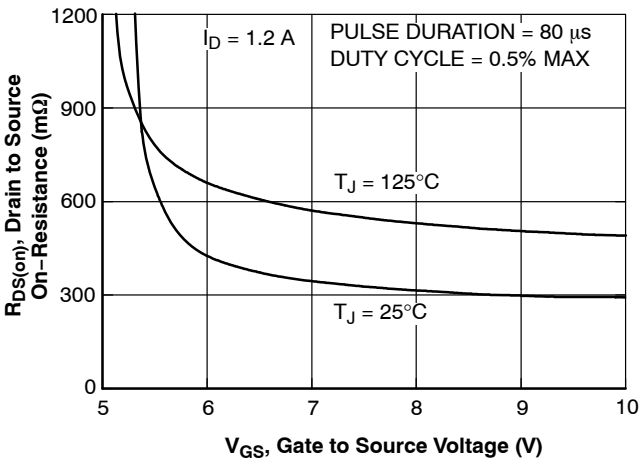


Figure 4. On−Resistance vs. Gate to Source Voltage

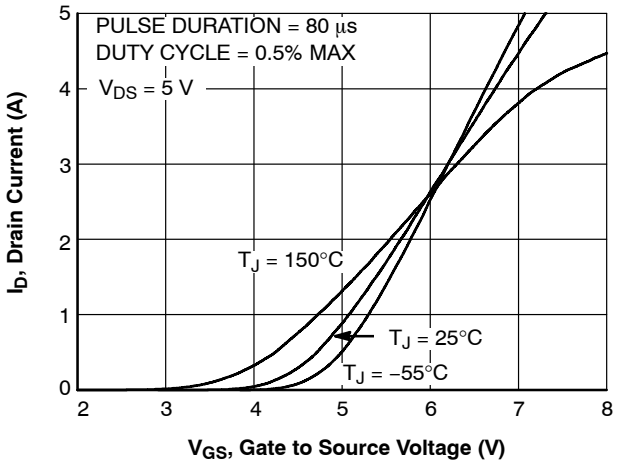


Figure 5. Transfer Characteristics

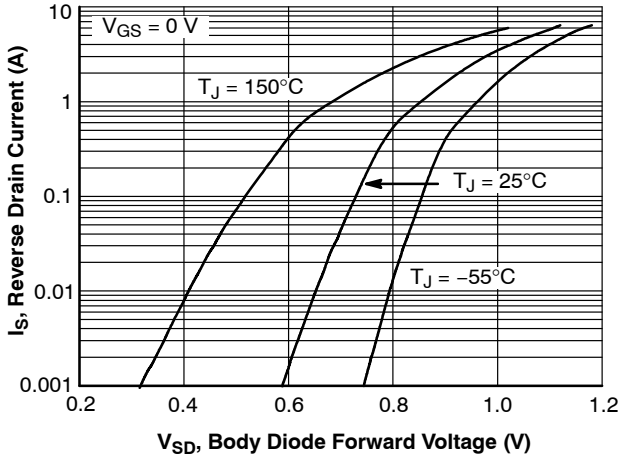


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

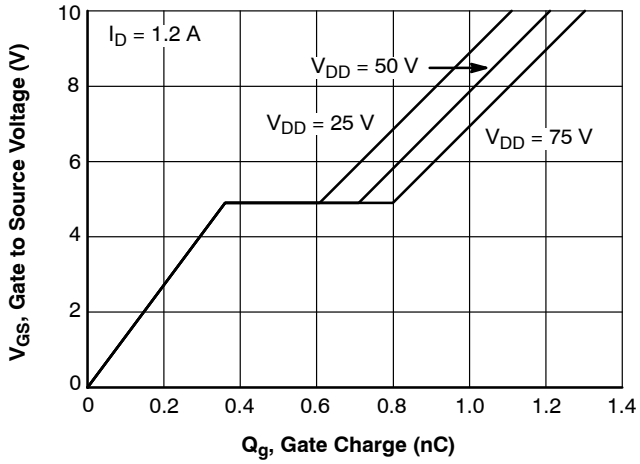


Figure 7. Gate Charge Characteristics

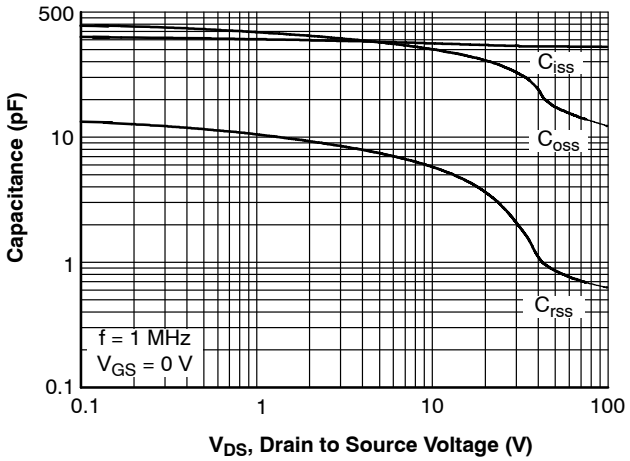


Figure 8. Capacitance vs. Drain to Source Voltage

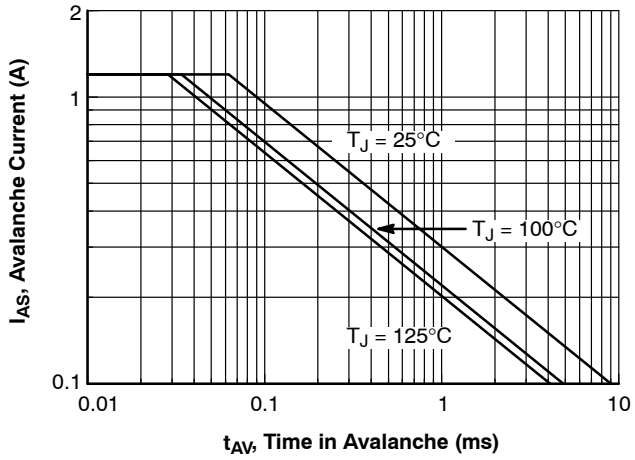


Figure 9. Unclamped Inductive Switching Capability

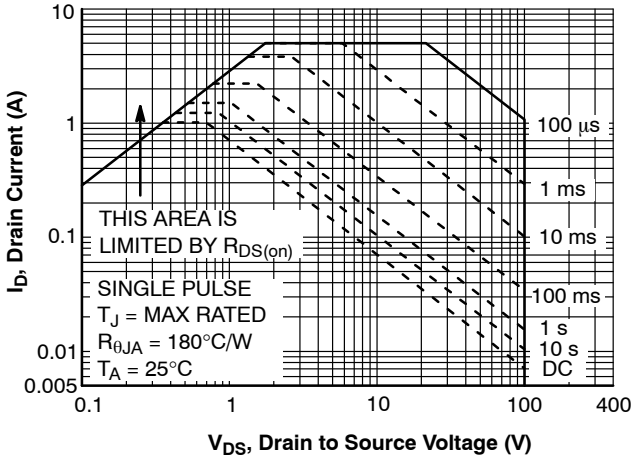


Figure 10. Forward Bias Safe Operating Area

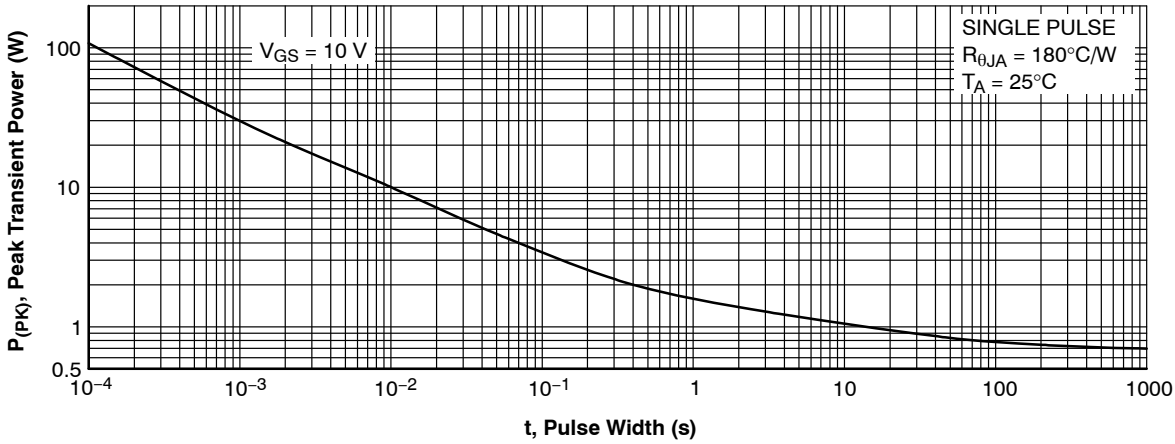


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

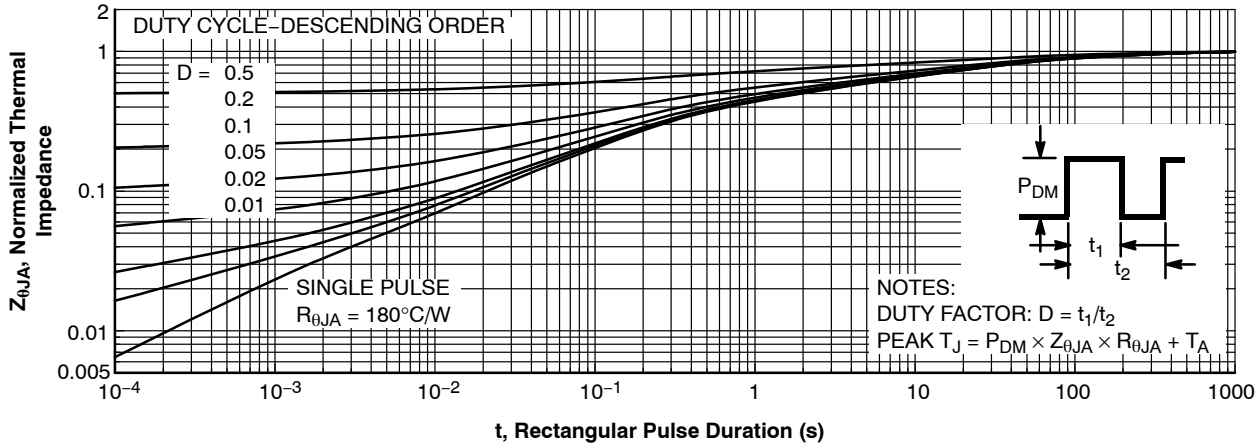
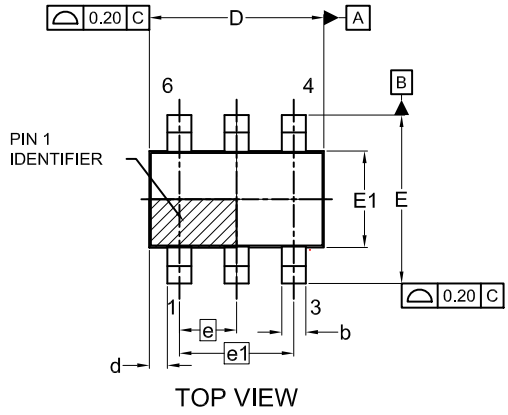


Figure 12. Junction−to−Ambient Transient Thermal Response Curve

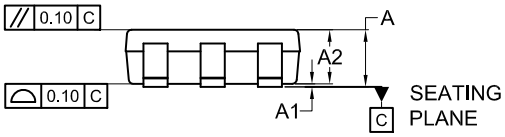
1
SCALE 2:1

TSOT23 6−Lead
CASE 419BL
ISSUE A

DATE 31 AUG 2020

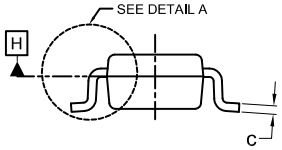


TOP VIEW

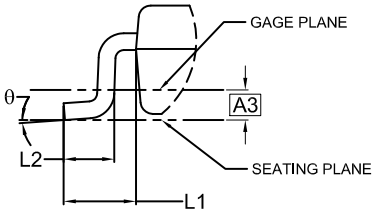


FRONT VIEW

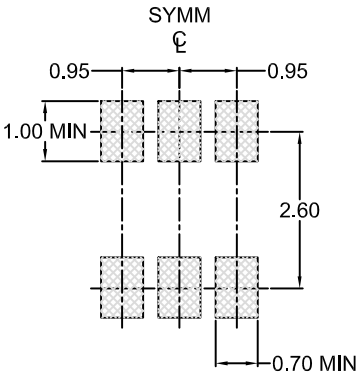
NOTE 4



SIDE VIEW



DETAIL A



LAND PATTERN
RECOMMENDATION

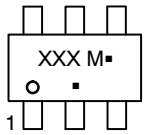
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3		0.25 BSC	
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d		0.30 REF	
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e		0.95 BSC	
e1		1.90 BSC	
L1		0.60 REF	
L2	0.20	0.40	0.60
θ	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSOT23 6−Lead**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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