MOSFET – N-Channel, UniFET™

200 V, 16 A, 125 m Ω

FDD18N20LZ

Description

UniFET MOSFET is ON Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on–state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Features

- $R_{DS(on)} = 125 \text{ m}\Omega \text{ (Typ.)} @ V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}$
- Low Gate Charge (Typ. 30 nC)
- Low C_{RSS} (Typ. 25 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- These Device is Pb-Free and is RoHS Compliant

Applications

- LED TV
- Consumer Appliances
- Uninterruptible Power Supply



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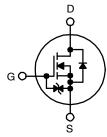
DPAK3 (TO-252 3 LD) CASE 369AS

MARKING DIAGRAM



FDD18N20LZ = Specific Device Code \$Y = ON Semiconductor Logo &Z = Assembly Plant Code &3 = 3-Digit Date Code

&K = 2-Digits Lot run Traceability Code



N-Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

MOSFET MAXIMUM RATINGS ($T_C = 25^{\circ}C$ unless otherwise noted)

Symbol	Parameter		FDD18N20LZ	Unit
V _{DSS}	Drain to Source Voltage		200	V
V_{GSS}	Gate to Source Voltage		±20	V
I _D	Drain Current	Continuous (T _C = 25°C)	16	Α
		Continuous (T _C = 100°C)	9.6	
I _{DM}	Drain Current (Note 1)	Pulsed	64	Α
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		320	mJ
I _{AR}	Avalanche Current (Note 1)		16	Α
E _{AR}	Repetitive Avalanche Energy (Note 1)		8.9	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		10	V/ns
P_{D}	Power Dissipation	(T _C = 25°C)	89	W
		Derate above 25°C	0.7	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
TL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Repetitive rating: pulse–width limited by maximum junction temperature.
2. L = 2.5 mH, I_{AS} = 16 A, V_{DD} = 50 V, R_{G} = 25 Ω , starting T_{J} = 25°C.
3. $I_{SD} \le$ 16 A, I_{AS} = 17 A, I_{AS} = 17 A, I_{AS} = 18 A, I_{AS} =

THERMAL CHARACTERISTICS

Symbol	Parameter	FDD18N20LZ	Unit
$R_{ heta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	83	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
OFF CHARA	CTERISTICS					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_J = 25^{\circ}C$	200	-	_	V
ΔBV_{DSS} / Δ	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	-	0.2	_	V/°C
T _J I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 200 V, V _{GS} = 0 V	-	-	1	μΑ
		V _{DS} = 160 V, T _C = 125°C	-	-	10	
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±10	μΑ
ON CHARAC	CTERISTICS					
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1.0	_	2.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 8 A	1	0.10	0.125	Ω
		V _{GS} = 5 V, I _D = 8 A	1	0.11	0.13	
9FS	Forward Transconductance	V _{DS} = 20 V, I _D = 2 A	-	11	-	S
DYNAMIC C	HARACTERISTICS					•
C _{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}$	_	1185	1575	pF
C _{oss}	Output Capacitance	f = 1 MHz	_	190	255	pF
C _{rss}	Reverse Transfer Capacitance		-	25	40	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 200 V, I _D = 16 A, V _{GS} = 10 V	-	30	40	nC
Q _{gs}	Gate to Source Gate Charge	(Note 4)	_	3.5	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	8.5	_	nC
SWITCHING	CHARACTERISTICS			•		
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 100 \text{ V}, I_D = 16 \text{ A}, V_{GS} = 10 \text{ V},$	-	15	40	ns
t _r	Turn-On Rise Time	$R_G = 25 \Omega$ (Note 4)	-	20	50	ns
t _{d(off)}	Turn-Off Delay Time		-	135	280	ns
t _f	Turn-Off Fall Time		-	50	110	ns
DAIN-SOUR	CE DIODE CHARACTERISTICS				•	
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	16	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	64	Α
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 4 A	-	-	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 4 A	-	105	-	ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100 A/μs	_	0.4	_	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

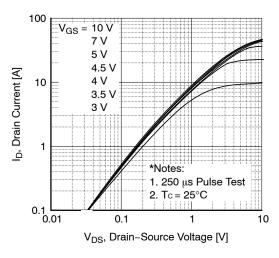


Figure 1. On-Region Characteristics

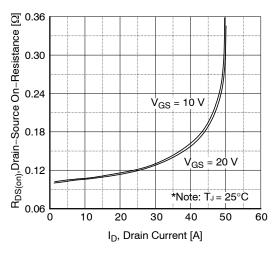


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

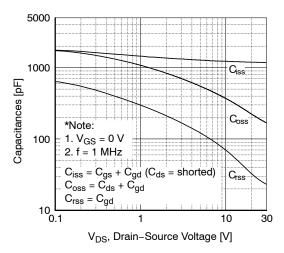


Figure 5. Capacitance Characteristics

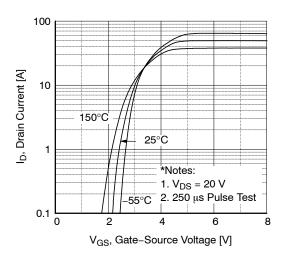


Figure 2. Transfer Characteristics

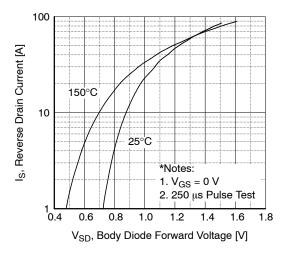


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

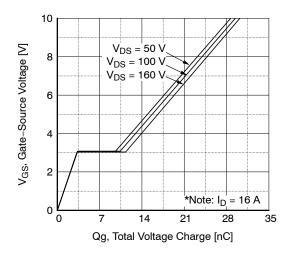


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

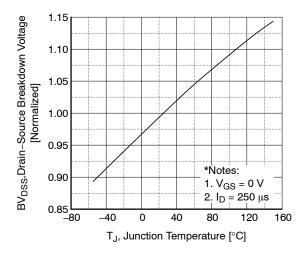


Figure 7. Breakdown Voltage Variation vs. Temperature

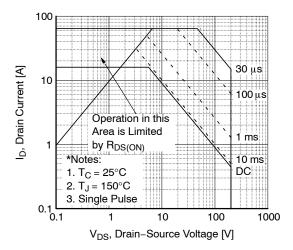


Figure 9. Maximum Safe Operating Area

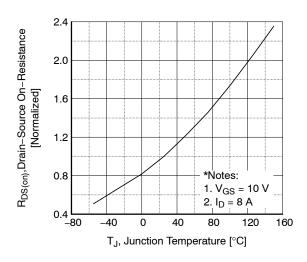


Figure 8. On–Resistance Variation vs. Temperature

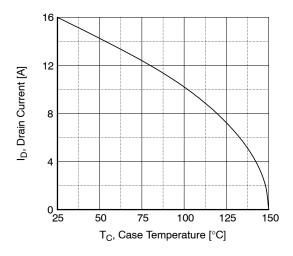


Figure 10. Maximum Drain Current vs.

Case Temperature

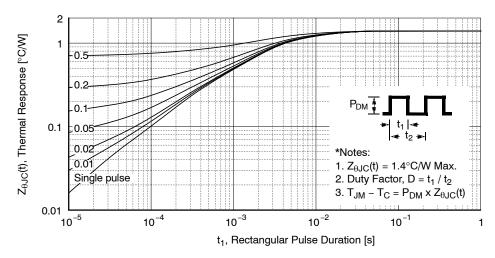


Figure 11. Transient Thermal Response Curve

PACKAGE MARKING ANDORDERING INFORMATION

Part Number	Top Mark	Package	Reel Size	Tape Width	Shipping [†]
FDD18N20LZ	FDD18N20LZ	DPAK3 (TO-252 3 LD) (Pb-Free)	330 mm	16 mm	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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DPAK3 6.10x6.54x2.29, 4.57P CASE 369AS **ISSUE B**

DATE 20 DEC 2023

- NOTES: UNLESS OTHERWISE SPECIFIED

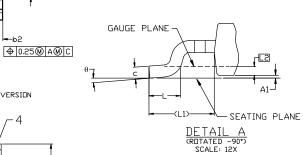
 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.

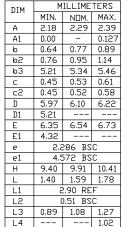
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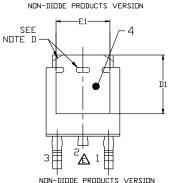
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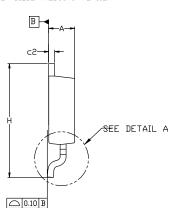
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 ASME Y14.5M-2018.
 SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED
 CORNERS OR EDGE PROTRUSION.
 FOR DIGDE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY
 STUB WITHOUT CENTER LEAD.
 DIMENSIONS ARE EXCLUSIVE OF BURRS,
 MOLD FLASH AND TIE BAR EXTRUSIONS.
 LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD
 T0228P991X239-3N.





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5.55	MIN-
	6.50 MIN
6.40 LXXX	
1	2.85 MIN
	1.25 MIN
4.5	2.286

LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

10°

XXXXXX XXXXXX **AYWWZZ**

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

XXXX = Specific Device Code

= Assembly Location Α

Υ = Year

WW = Work Week

77 = Assembly Lot Code

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