FAIRCHILD™

Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

March 2015

FDD6612A/FDU6612A

30V N-Channel PowerTrench^Ò MOSFET

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$, fast switching speed and extremely low $R_{DS(ON)}$ in a small package.

Applications

- DC/DC converter
- Motor Drives

Features

- 30 A, 30 V $R_{DS(ON)} = 20\ m\Omega\ @\ V_{GS} = 10\ V$
  $R_{DS(ON)} = 28\ m\Omega\ @\ V_{GS} = 4.5\ V$

- Low gate charge

- Fast Switching

- High performance trench technology for extremely low $R_{DS(ON)}$

D-PAK (TO-252)

I-PAK (TO-251AA)
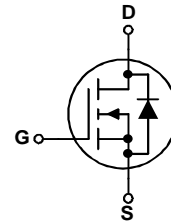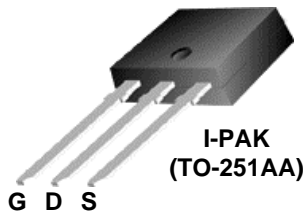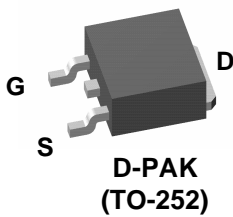
Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DSS}	Drain-Source Voltage			30	V
V_{GSS}	Gate-Source Voltage			±20	V
I_D	Continuous Drain Current	@T_C=25°C	(Note 3)	30	A
		@T_A=25°C	(Note 1a)	9.5	
		Pulsed	(Note 1a)	60	
P_D	Power Dissipation	@T_C=25°C	(Note 1)	36	W
		@T_A=25°C	(Note 1a)	2.8	
		@T_A=25°C	(Note 1b)	1.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)		3.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)		45	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)		96	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape width	Quantity
FDD6612A	FDD6612A	D-PAK (TO-252)	13''	16mm	2500 units
FDU6612A	FDU6612A	I-PAK (TO-251)	Tube	N/A	75

Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 2)						
W_{DSS}	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 27$ V, I_D=10 A			51	mJ
I_{AR}	Drain-Source Avalanche Current				10	A
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ µA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C		25		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24$ V, $V_{GS} = 0$ V			1	µA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm20$ V, $V_{DS} = 0$ V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ µA	1	2.0	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C		−5.1		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10$ V, $I_D = 9.5$ A $V_{GS} = 4.5$ V, $I_D = 8$ A $V_{GS} = 10$ V, $I_D = 9.5$ A, T_J=125°C		15 20 23	20 28 33	mΩ
g_{FS}	Forward Transconductance	$V_{DS} = 5$ V, $I_D = 9.5$ A		28		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$ V, f = 1.0 MHz		660		pF
C_{oss}	Output Capacitance			170		pF
C_{rss}	Reverse Transfer Capacitance			90		pF
R_G	Gate Resistance	$V_{GS} = 15$ Mv, f = 1.0 MHz		2.3		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15$ V, $I_D = 1$ A, $V_{GS} = 10$ V, $R_{GEN} = 6$ Ω		9	18	ns
t_r	Turn–On Rise Time			5	10	ns
$t_{d(off)}$	Turn–Off Delay Time			24	38	ns
t_f	Turn–Off Fall Time			4	8	ns
Q_g	Total Gate Charge	$V_{DS} = 15$ V, $I_D = 9.5$ A, $V_{GS} = 5$ V		6.7	9.4	nC
Q_{gs}	Gate–Source Charge			2.1		nC
Q_{gd}	Gate–Drain Charge			2.7		nC

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				2.3	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.3 A (Note 2)		0.8	1.2	V
trr	Diode Reverse Recovery Time	IF = 9.5 A, diF/dt = 100 A/µs		20		nS
Qrr	Diode Reverse Recovery Charge			10		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
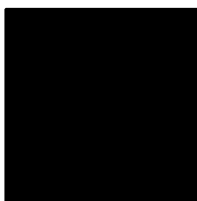
a) $R_{\theta JA}$ = 45°C/W when mounted on a 1in^2 pad of 2 oz copper

b) $R_{\theta JA}$ = 96°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. Maximum current is calculated as:

$$\sqrt{\frac{P_D}{R_{DS(ON)}}}$$

where P_D is maximum power dissipation at T_C = 25°C and $R_{DS(on)}$ is at $T_{J(max)}$ and V_{GS} = 10V. Package current limitation is 21A

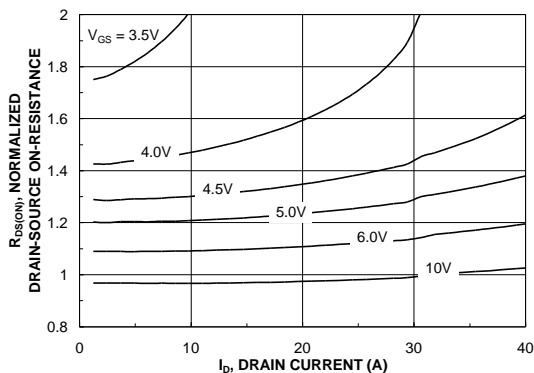## Typical Characteristics
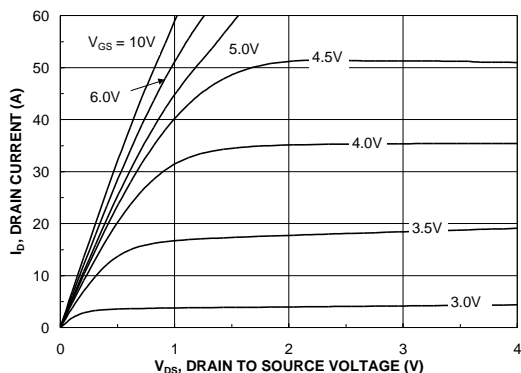
Figure 1. On-Region Characteristics

**Figure 2. On-Resistance Variation with
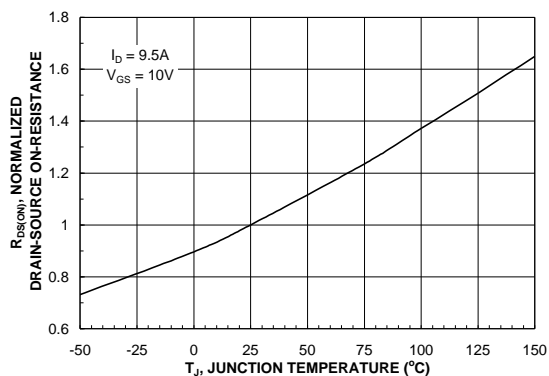Drain Current and Gate Voltage**

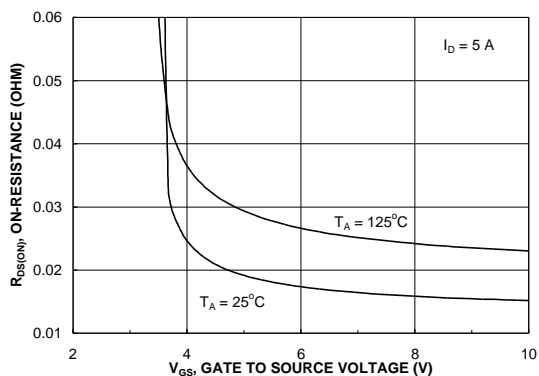**Figure 3. On-Resistance Variation
withTemperature**

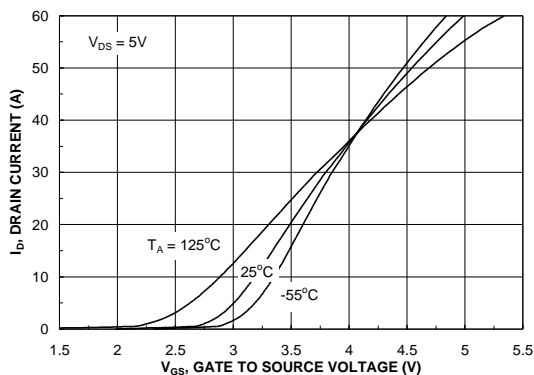**Figure 4. On-Resistance Variation with
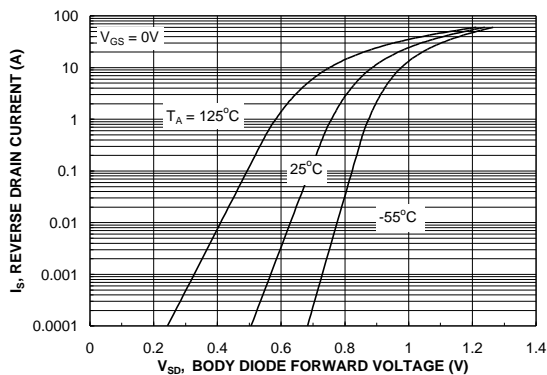Gate-to-Source Voltage**

Figure 5. Transfer Characteristics

**Figure 6. Body Diode Forward Voltage Variation
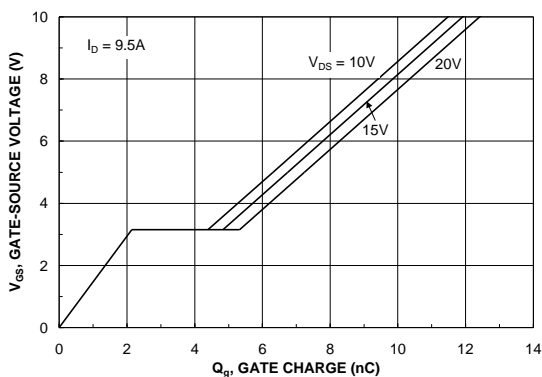with Source Current and Temperature**

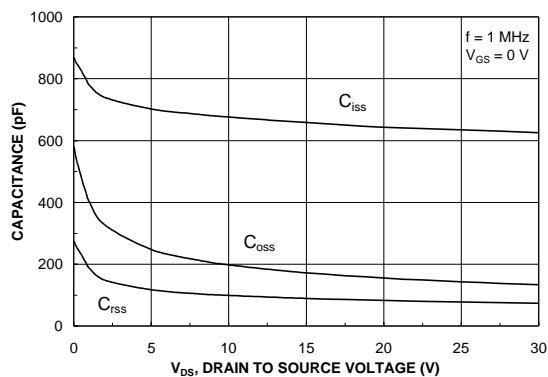# Typical Characteristics

Figure 7. Gate Charge Characteristics

Figure 8. Capacitance Characteristics
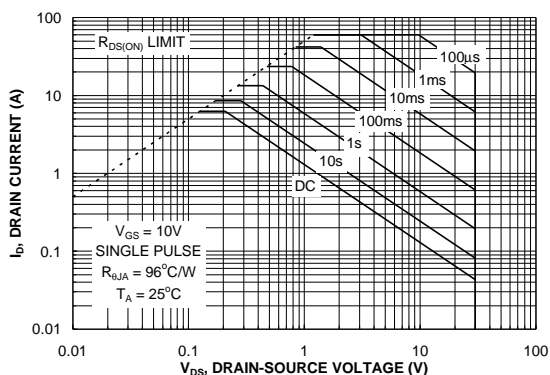
Figure 9. Maximum Safe Operating Area
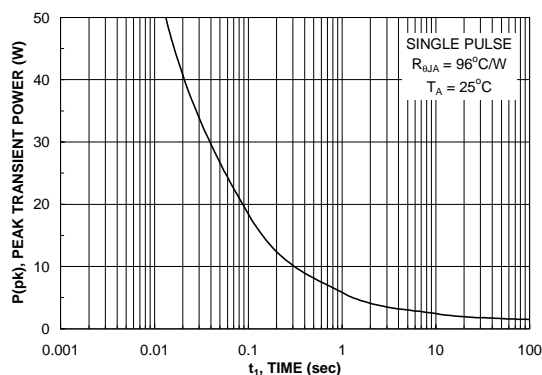
Figure 10. Single Pulse Maximum Power Dissipation

$R_{\theta JA}(t) = r(t) * R_{\theta JA}$

$R_{\theta JA} = 96^{\circ}C/W$

$T_J - T_A = P * R_{\theta JA}(t)$

Duty Cycle, $D = t_1 / t_2$
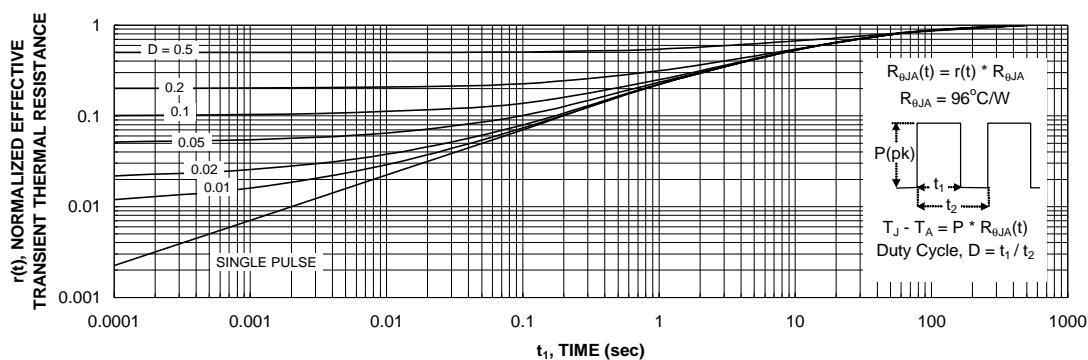
Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

6.73
6.35

A

5.46
5.21

1.27
0.89

6.22
5.97

C

⟨E⟩
1.02 MAX

0.25 MAX

1   2   3

ISOLATED PLASTIC
BODY STUB

DIODE
PRODUCTS VERSION

1   2   3

(0.59)

1.14
0.76

0.89
0.64

| ⌖ | 0.25 Ⓜ | AⓂ | C |

2.29

4.57

NON-DIODE
PRODUCTS VERSION

5.55 MIN

4

6.50 MIN

6.40

2.85 MIN

1   3

1.25 MIN

2.28

4.56

LAND PATTERN
RECOMMENDATION

SEE
NOTE D

4.32 MIN

4

5.21 MIN

3   2   1
⟨E⟩

NON-DIODE
PRODUCTS VERSION

3   2   1

DIODE
PRODUCTS VERSION

B

2.39
2.18

0.58
0.45

10.41
9.40

SEE DETAIL A

| ⌒ | 0.10 | B |

NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252,
   ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER
   ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED
   CORNERS OR EDGE PROTRUSION.
⟨E⟩ TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSIVE OF BURS,
   MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD
   TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11

GAGE PLANE

0.51

0.61
0.45

10°
0°

(1.54)

1.78
1.40

0.127 MAX

(2.90)

SEATING PLANE

DETAIL A
(ROTATED -90°)
SCALE: 12X

FAIRCHILD™

PUBLICATION ORDERING INFORMATION
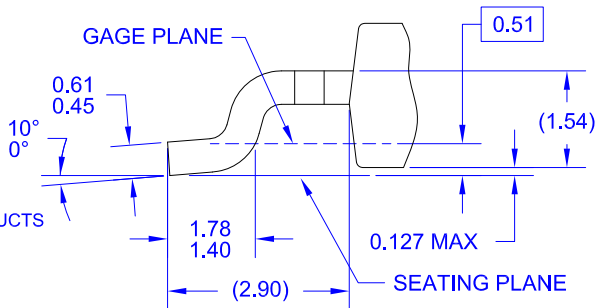
© Semiconductor Components Industries, LLC

www.onsemi.com