MOSFET – N-Channel, POWERTRENCH®

80 V, 100 A, 4.2 mΩ

FDD86367

Features

- Typical $R_{DS(on)}$ = 3.3 mΩ at V_{GS} = 10 V, I_D = 80 A
- Typical $Q_{g(tot)}$ = 68 nC at V_{GS} = 10 V, I_D = 80 A
- UIS Capability
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant

Applications

- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

MOSFET MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

| Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain−to−Source Voltage	80	V
V_{GS}	Gate−to−Source Voltage	±20	V
I_D	Drain Current – Continuous (V_{GS} = 10) (Note 1) T_C = 25°C	100	A
	Pulsed Drain Current T_C = 25°C	See Figure 4	
EAS	Single Pulse Avalanche Energy (Note 2)	82	mJ
P_D	Power Dissipation	227	W
	Derate Above 25°C	1.52	W/°C
T_J, T_{STG}	Operating and Storage Temperature	−55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.66	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	52	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Current is limited by bondwire configuration.
2. Starting T_J = 25°C, L = 40 μH, I_{AS} = 64 A, V_{DD} = 80 V during inductor charging and V_{DD} = 0V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{qJC} is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.
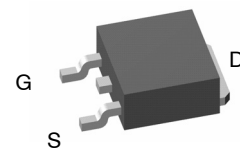
ON Semiconductor®
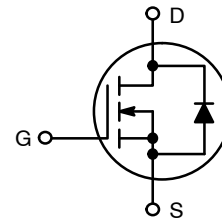
N−Channel
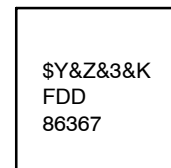

DPAK3 (TO−252 3 LD)
CASE 369AS

MARKING DIAGRAM

$Y&Z&3&K
FDD
86367

FDD86367	= Specific Device Code
$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= 3−Digit Date Code
&K	= 2−Digits Lot Run Traceability Code

ORDERING INFORMATION

FDD86367

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping[†]
FDD86367	FDD86367	DPAK3 (TO−252 3 LD) (Pb−Free)	13"	16 mm	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
B_{VDSS}	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		80	–	–	V
I_{DSS}	Drain−to−Source Leakage Current	V_{DS} = 80 V, V_{GS} = 0 V	T_J = 25°C	–	–	1	mA
			T_J = 175°C (Note 4)	–	–	1	mA
I_{GSS}	Gate−to−Source Leakage Current	V_{GS} = ±20 V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		2	3	4	V
$R_{DS(on)}$	Drain to Source On Resistance	I_D = 80 A, V_{GS}= 10 V	T_J = 25°C	–	3.3	4.2	mΩ
			T_J = 175°C (Note 4)	–	6.6	8.4	mΩ
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		–	4840	–	pF
C_{oss}	Output Capacitance			–	814	–	pF
C_{rss}	Reverse Transfer Capacitance			–	31	–	pF
R_g	Gate Resistance	V_{GS} = 0.5 V, f = 1 MHz		–	2.3	–	Ω
$Q_{g(ToT)}$	Total Gate Charge	V_{GS} = 0 to 10 V	V_{DD} = 40 V, I_D = 80 A	–	68	88	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2 V		–	8.8	–	nC
Q_{gs}	Gate−to−Source Gate Charge	V_{DD} = 40 V, I_D = 80 A		–	22	–	nC
Q_{gd}	Gate−to−Drain "Miller" Charge			–	14	–	nC
SWITCHING CHARACTERISTICS							
t_{on}	Turn−On Time	V_{DD} = 40 V, I_D = 80 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		–	–	104	ns
$t_{d(on)}$	Turn−On Delay			–	20	–	ns
t_r	Rise Time			–	49	–	ns
$t_{d(off)}$	Turn−Off Delay			–	36	–	ns
t_f	Fall Time			–	16	–	ns
t_{off}	Turn−Off Time			–	–	80	ns
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source−to−Drain Diode Voltage	I_{SD} = 80 A, V_{GS} = 0 V		–	–	1.3	V
		I_{SD} = 40 A, V_{GS} = 0 V		–	–	1.2	V
t_{rr}	Reverse−Recovery Time	V_{DD} = 64 V, I_F = 80 A, dI_{SD}/dt = 100 A/μs		–	68	102	ns
Q_{rr}	Reverse−Recovery Charge			–	66	106	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

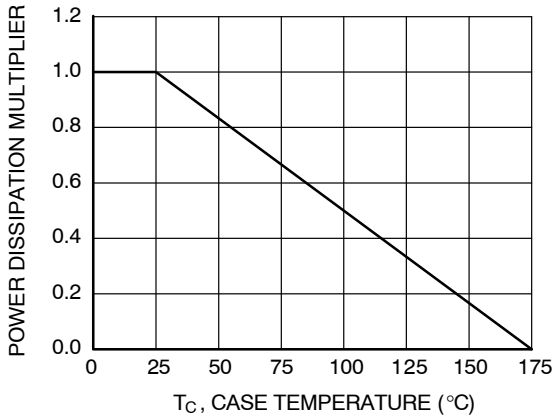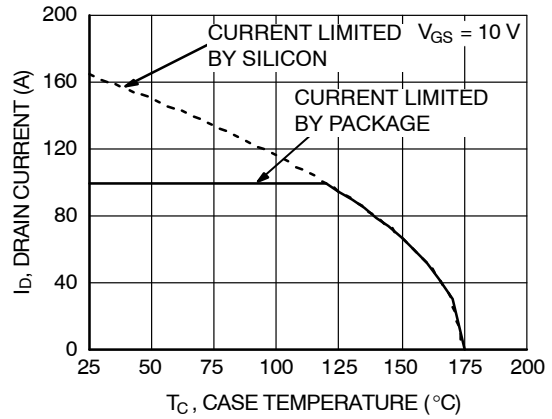**Figure 1. Normalized Power Dissipation vs. Case Temperature**

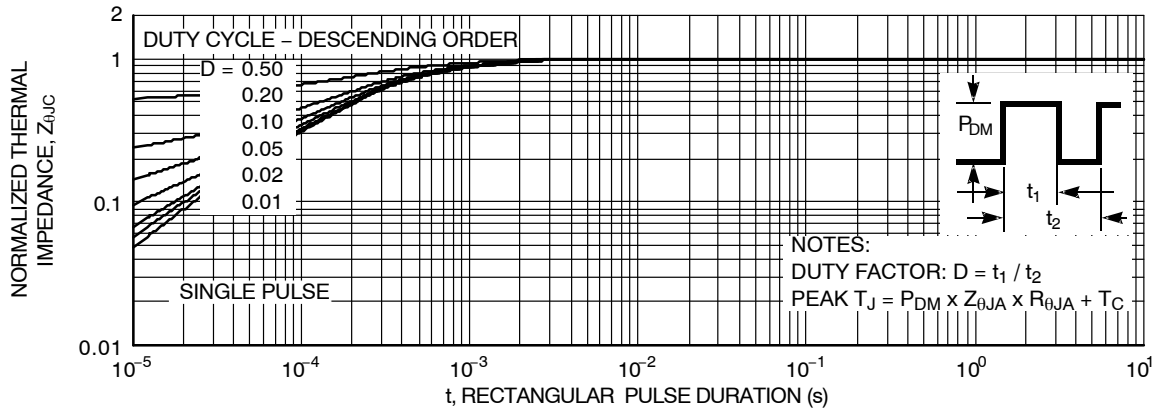**Figure 2. Maximum Continuous Drain Current vs. Case Temperature**

NOTES:
DUTY FACTOR: D = t_1 / t_2
PEAK T_J = P_{DM} x $Z_{\theta JA}$ x $R_{\theta JA}$ + T_C

Figure 3. Normalized Maximum Transient Thermal Impedance

T_C = 25°C
FOR TEMPERATURES ABOVE 25°C DERATE PEAK CURRENT AS FOLLOWS:

$$I = I_2 \left[\sqrt{\frac{175 - T_C}{150}} \right]$$
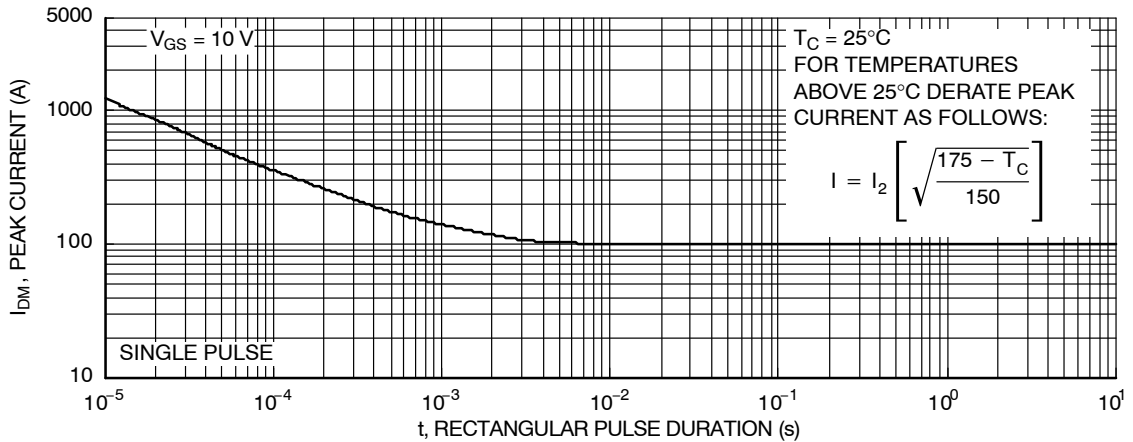
Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)
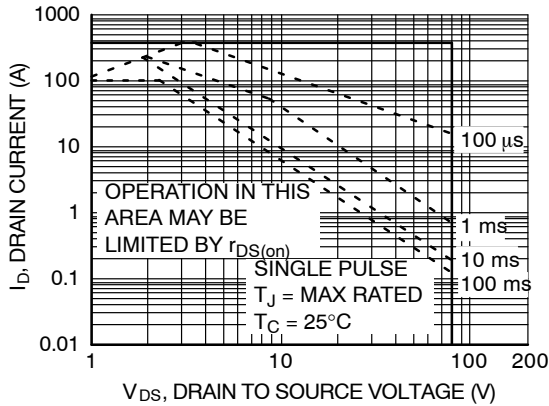
Figure 5. Forward Bias Safe Operating Area

Figure 6. Unclamped Inductive Switching Capability
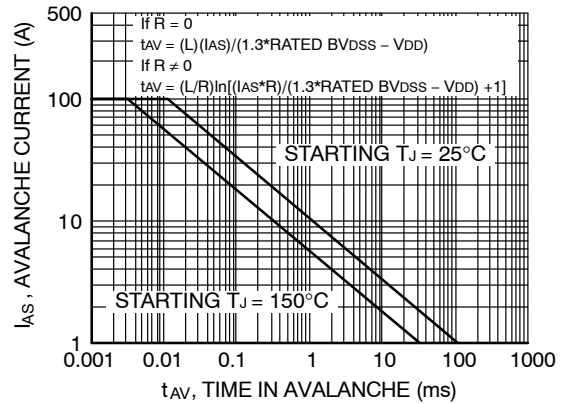
NOTE: Refer to ON Application Notes AN7514 and AN7515
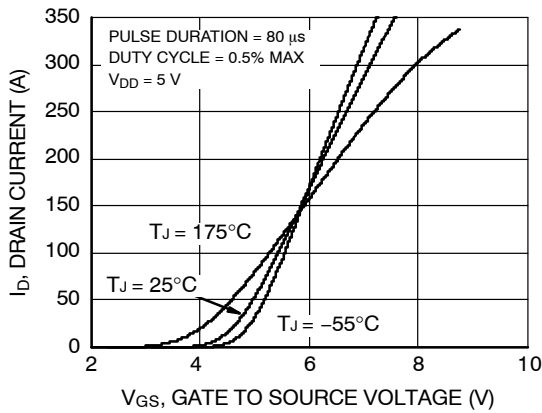
Figure 7. Transfer Characteristics
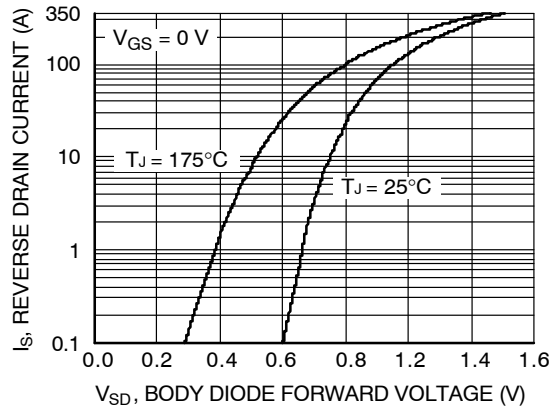
Figure 8. Forward Diode Characteristics
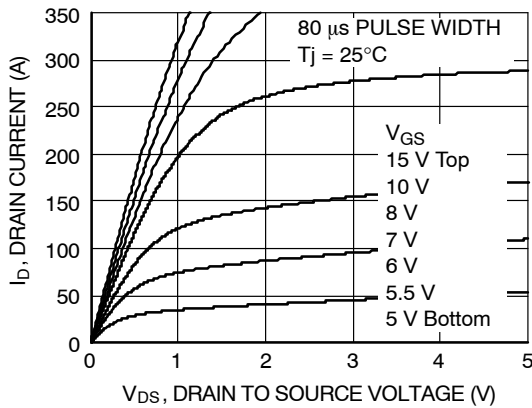
Figure 9. Saturation Characteristics
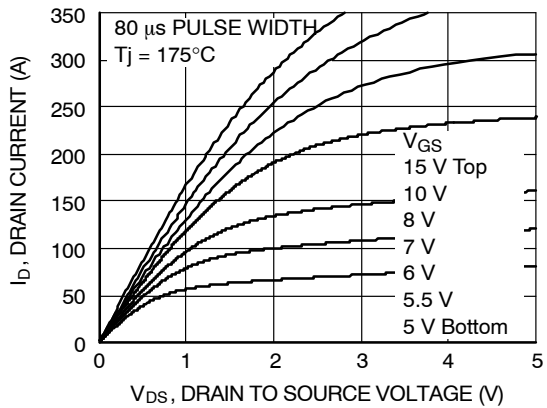
Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)
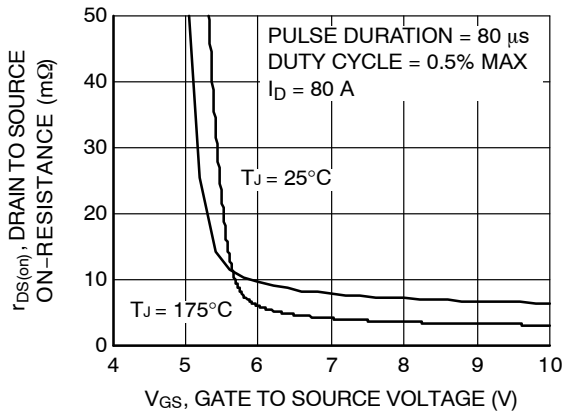
Figure 11. R$_{DSON}$ vs. Gate Voltage
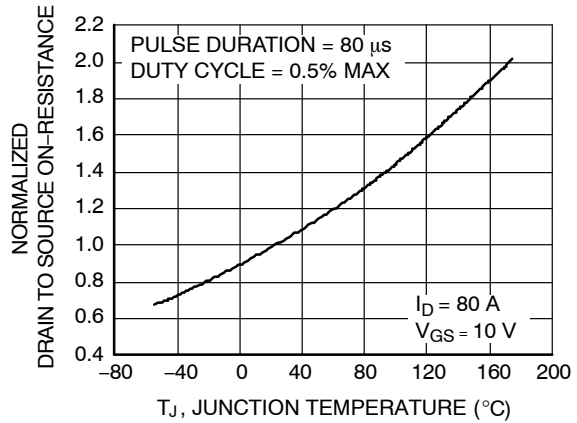
Figure 12. Normalized R$_{DSON}$ vs. Junction Temperature
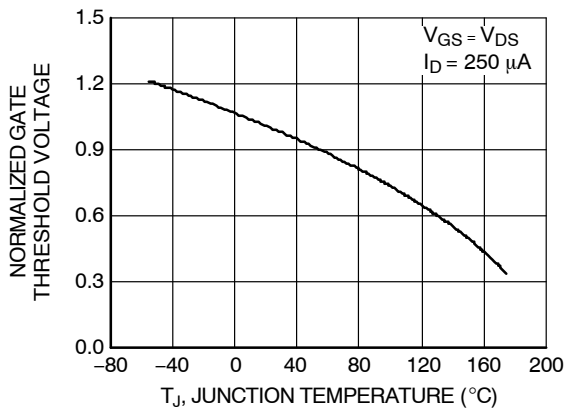
Figure 13. Normalized Gate Threshold Voltage vs. Temperature
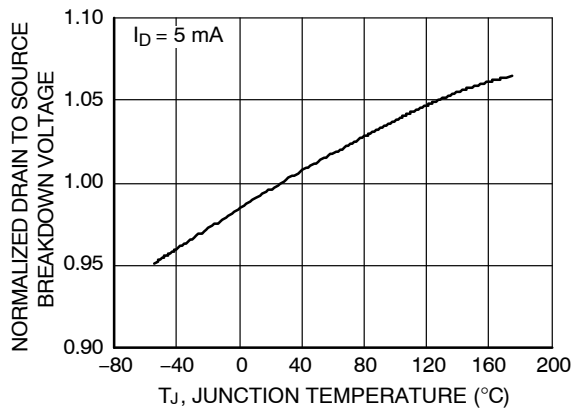
Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature
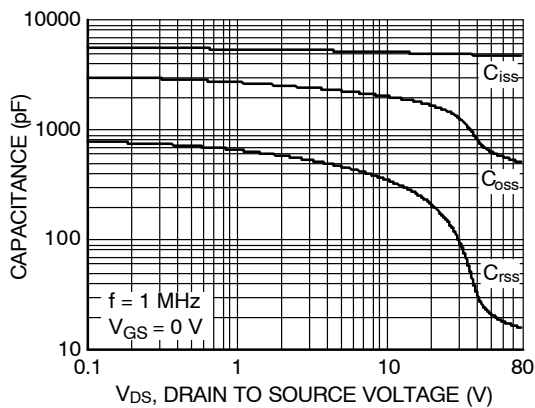
Figure 15. Capacitance vs. Drain to Source Voltage
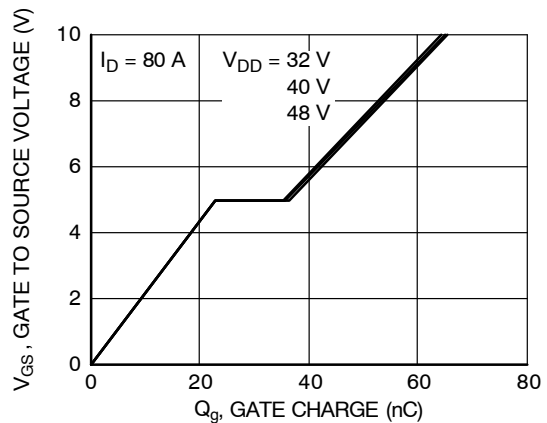
Figure 16. Gate Charge vs. Gate to Source Voltage

DPAK3 6.10x6.54x2.29, 4.57P
CASE 369AS
ISSUE B

DATE 20 DEC 2023
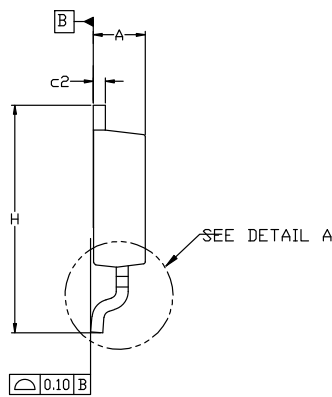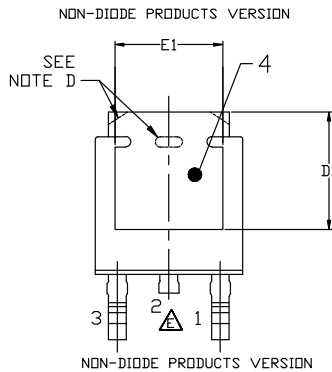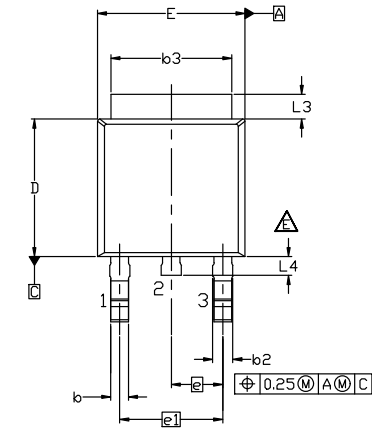
NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252,
   ISSUE F, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER
   ASME Y14.5M-2018.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED
   CORNERS OR EDGE PROTRUSION.
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY
   STUB WITHOUT CENTER LEAD.
F) DIMENSIONS ARE EXCLUSIVE OF BURRS,
   MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD
   TO228P991X239-3N.

NON-DIODE PRODUCTS VERSION

NON-DIODE PRODUCTS VERSION

GAUGE PLANE

DETAIL A
(ROTATED -90°)
SCALE: 12X

SEATING PLANE

SEE DETAIL A

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	–	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	---	---
E	6.35	6.54	6.73
E1	4.32	---	---
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	---	---	1.02
θ	0°	---	10°

5.55 MIN

6.50 MIN

6.40

2.85 MIN

1.25 MIN

2.286

4.572

LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR
SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

XXXXXX
XXXXXX
AYWWZZ
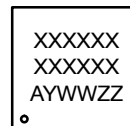
*This information is generic. Please refer to
device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may
or may not be present. Some products may
not follow the Generic Marking.

XXXX = Specific Device Code
A   = Assembly Location
Y   = Year
WW   = Work Week
ZZ   = Assembly Lot Code

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DESCRIPTION:	DPAK3 6.10x6.54x2.29, 4.57P		PAGE 1 OF 1

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