[MOSFET]{.blue} - P-Channel
PowerTrench®
-40 V, 7.5 mΩ, -90 A
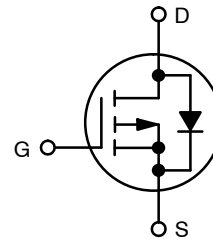
FDD9509L-F085

Features

- Typ $r_{DS(on)}$ = 6.0 mΩ at V_{GS} = −10 V; I_D = −70 A
- Typ $Q_{g(tot)}$ = 50 nC at V_{GS} = −10 V; I_D = −70 A
- UIS Capability
- Qualified to AEC Q101
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electrical Power Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12 V Systems

ON Semiconductor®

DPAK
TO−252
CASE 369AS

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain to Source Voltage	V_{DSS}	−40	V
Gate to Source Voltage	V_{GS}	±16	V
Drain Current − Continuous (V_{GS} = −10 V) (T_C = 25°C) (Note 1)	I_D	−90	A
Pulsed Drain Current (T_C = 25°C)	I_D	See Figure 4	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	82	mJ
Power Dissipation	P_D	150	W
Derate above 25°C	P_D	1.0	W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	−55 to +175	°C
Thermal Resistance (Junction to Case)	$R_{\theta JC}$	1.0	°C/W
Maximum Thermal Resistance (Junction to Ambient) (Note 3)	$R_{\theta JA}$	52	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by wirebond configuration
2. Starting Tj = 25°C, L = 40 μH, I_{AS} = −64 A, V_{DD} = −40 V during inductor charging and V_{DD} = 0 V during time in avalanche
3. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2 oz copper.

FDD9509L−F085

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
FDD9509L−F085	FDD9509L	D−PAK (TO−252)	13″	12 mm	2500 Units

ELECTRICAL CHARACTERISTICS $(T_J = 25°C$ unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = -250$ μA		−40	–	–	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = -40$ V, $V_{GS} = 0$ V	$T_J = 25°C$	–	–	−1	μA
			$T_J = 175°C$ (Note 4)	–	–	−1	mA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm16$ V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250$ μA		−1	−2	−3	V
$R_{DS(on)}$	Drain to Source On−Resistance	$V_{GS} = -4.5$ V, $I_D = -35$ A, $T_J = 25°C$		–	8.7	15	mΩ
		$V_{GS} = -10$ V, $I_D = -70$ A	$T_J = 25°C$	–	6.0	7.5	mΩ
			$T_J = 175°C$ (Note 4)	–	10	12.6	mΩ
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	$V_{DS} = -20$ V, $V_{GS} = 0$ V, $f = 1$ MHz		–	3350	–	pF
C_{oss}	Output Capacitance			–	1250	–	pF
C_{rss}	Reverse Transfer Capacitance			–	42	–	pF
R_g	Gate Resistance	$V_{GS} = -0.5$ V, $f = 1$ MHz		–	22	–	Ω
$Q_{g(tot)}$	Total Gate Charge	$V_{DD} = -20$ V, $I_D = -70$ A	$V_{GS} = 0$ V to −10 V	–	50	75	nC
$Q_{g(-4.5)}$	Total Gate Charge		$V_{GS} = 0$ V to −4.5 V	–	23	–	nC
$Q_{g(th)}$	Threshold Gate Charge		$V_{GS} = 0$ V to −1 V	–	3.5	–	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = -20$ V, $I_D = -70$ A		–	12	–	nC
Q_{gd}	Gate to Drain "Miller" Charge			–	6	–	nC
SWITCHING CHARACTERISTICS							
t_{on}	Turn-On Time	$V_{DD} = -20$ V, $I_D = -80$ A, $V_{GS} = -10$ V, $R_{GEN} = 6$ Ω		–	–	16	ns
$t_{d(on)}$	Turn-On Delay Time			–	8.0	–	ns
t_r	Turn-On Rise Time			–	4.0	–	ns
$t_{d(off)}$	Turn-Off Delay Time			–	190	–	ns
t_f	Turn-Off Fall Time			–	60	–	ns
t_{off}	Turn-Off Time			–	–	375	ns
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source to Drain Diode Voltage	$V_{GS} = 0$ V, $I_{SD} = -70$ A		–	−0.96	−1.25	V
		$V_{GS} = 0$ V, $I_{SD} = -35$ A		–	−0.88	−1.2	V
T_{rr}	Reverse Recovery Time	$I_F = -70$ A, $dI_{SD}/dt = 100$ A/μs		–	54	71	ns
Q_{rr}	Reverse Recovery Charge			–	43	57	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at $T_J = 175°C$. Product is not tested to this condition in production
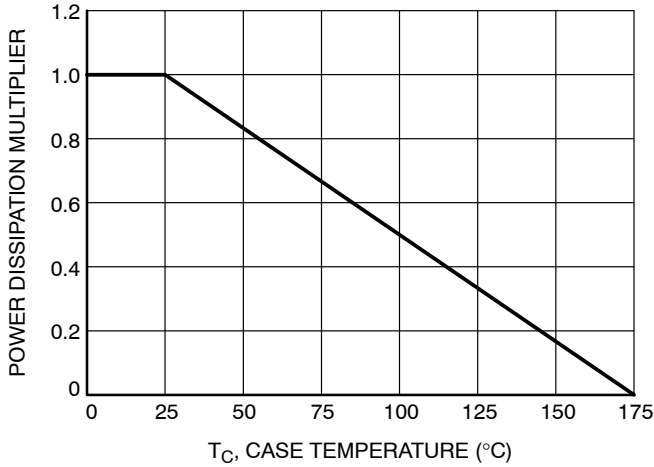
TYPICAL CHARACTERISTICS

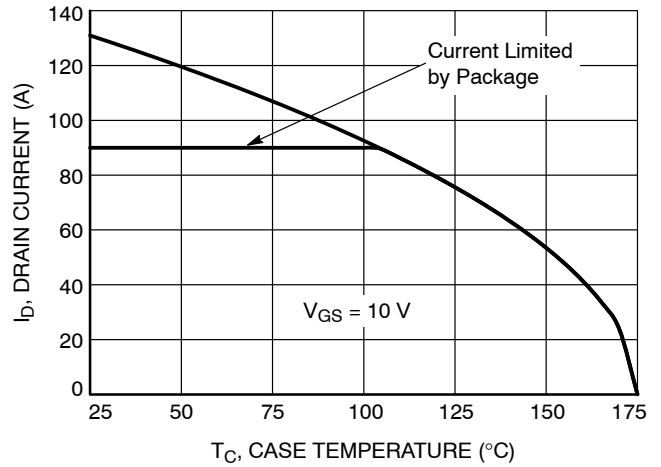Figure 1. Normalized Power Dissipation vs.
Case Temperature

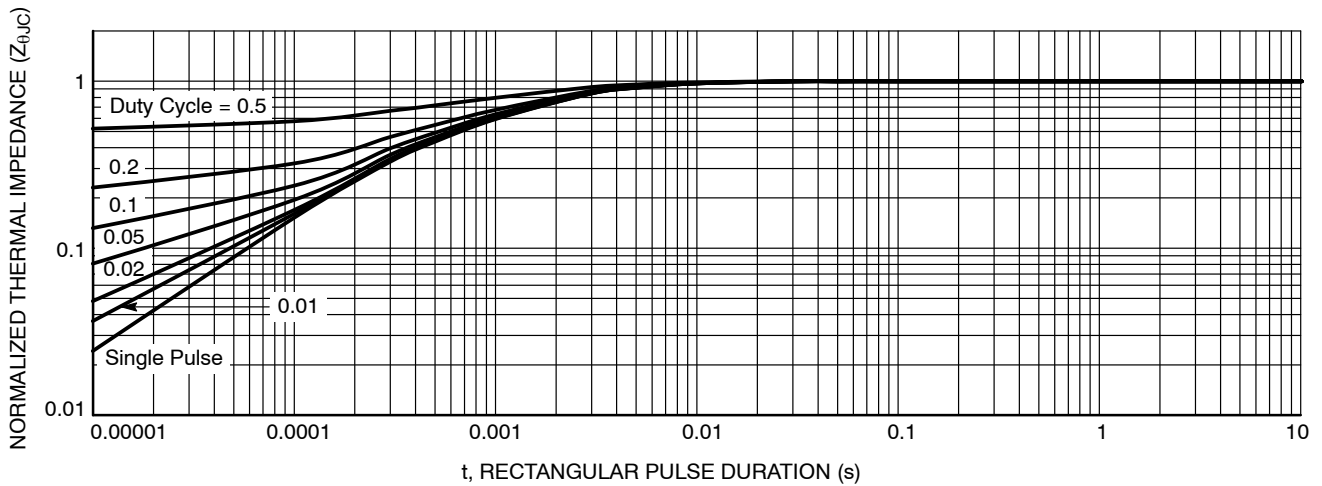Figure 2. Maximum Continuous Drain Current
vs. Case Temperature

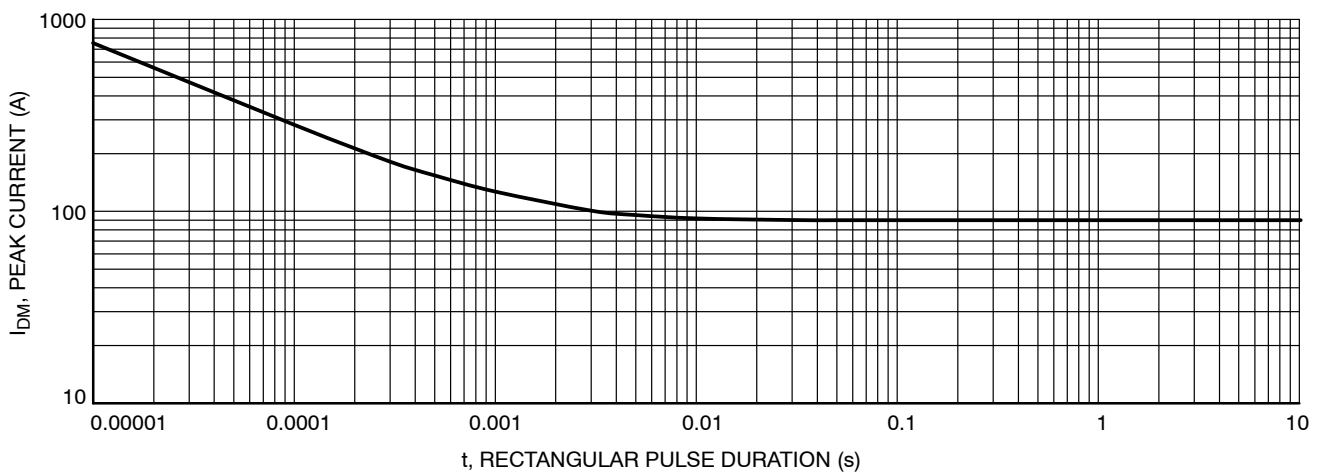Figure 3. Normalized Maximum Transient Thermal Impedance
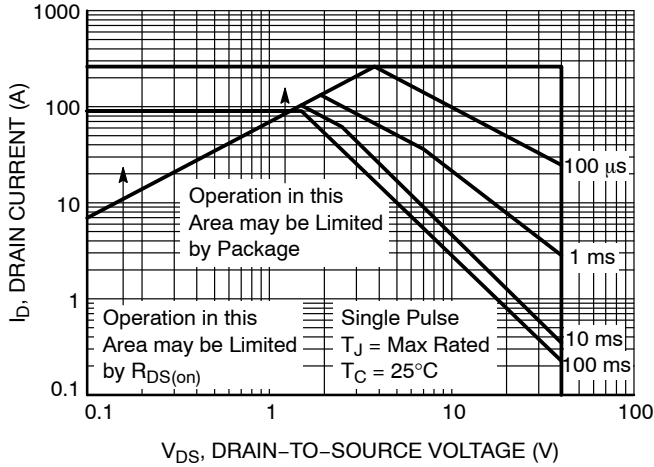
Figure 4. Peak Current Capability

FDD9509L−F085

TYPICAL CHARACTERISTICS
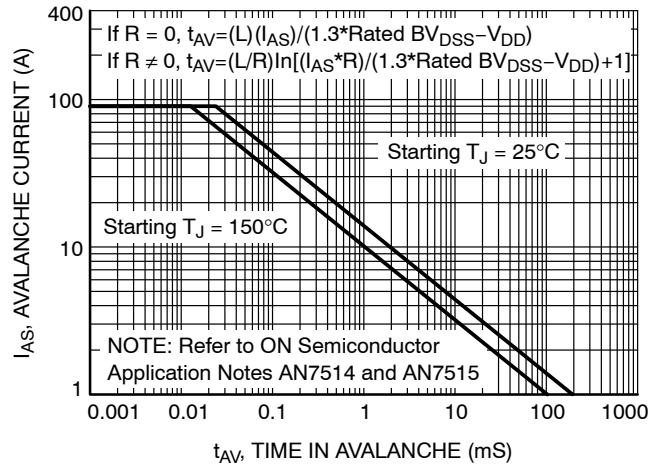

Figure 5. Forward Bias Safe Operating Area
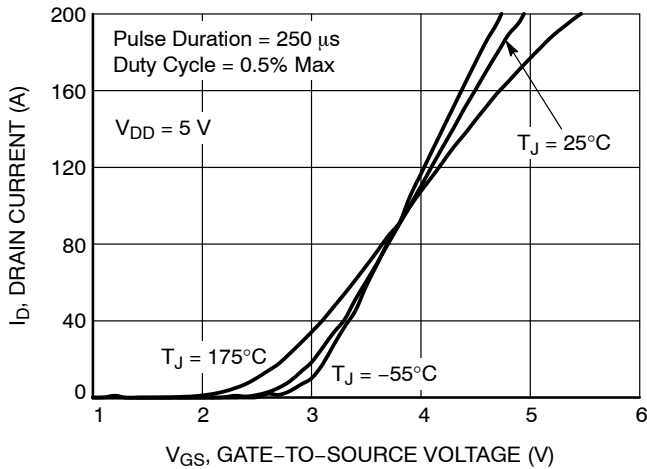

Figure 6. Unclamped Inductive Switching Capability

$$\text{If } R = 0, \; t_{AV} = (L)(I_{AS})/(1.3 \ast \text{Rated } BV_{DSS} - V_{DD})$$
$$\text{If } R \neq 0, \; t_{AV} = (L/R)\ln[(I_{AS} \ast R)/(1.3 \ast \text{Rated } BV_{DSS} - V_{DD}) + 1]$$

NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 7. Transfer Characteristics
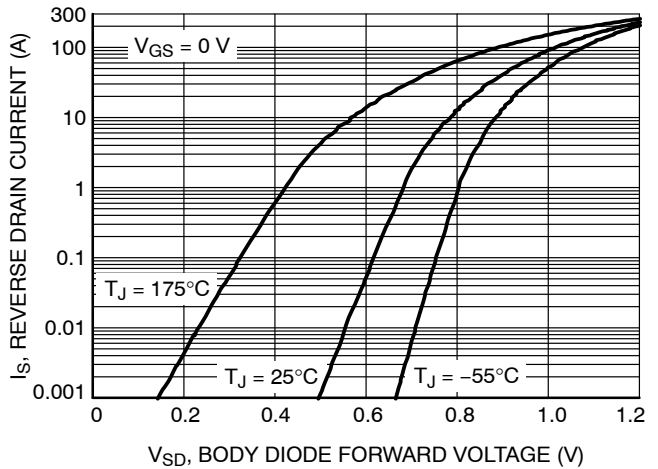
Figure 8. Forward Diode Characteristics
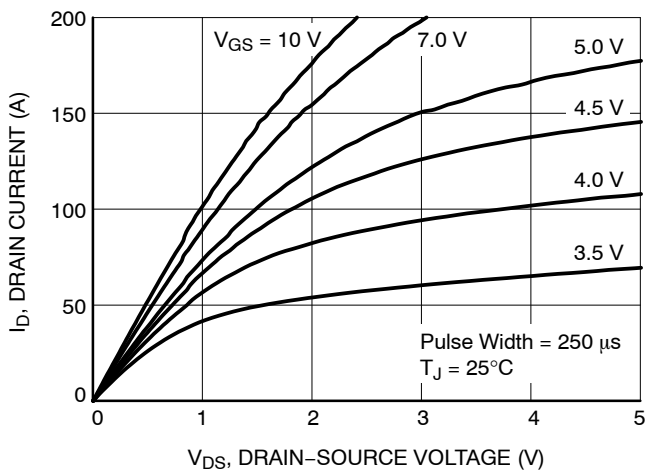
Figure 9. Saturation Characteristics
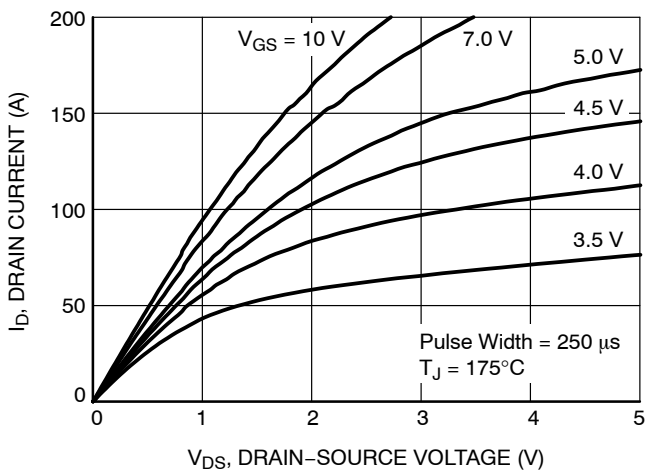
Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS
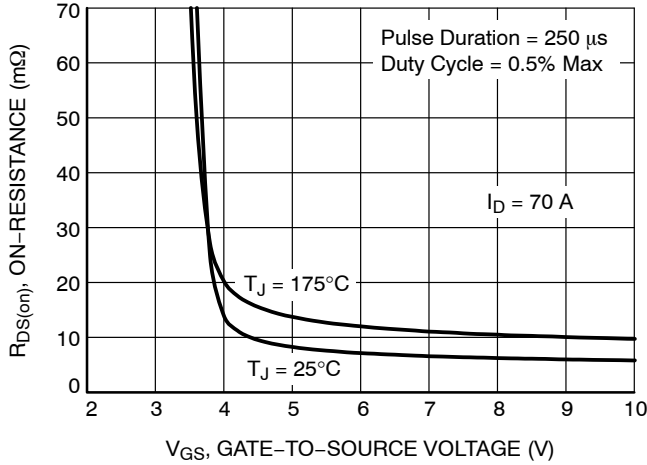
Figure 11. R$_{DS(on)}$ vs. Gate Voltage
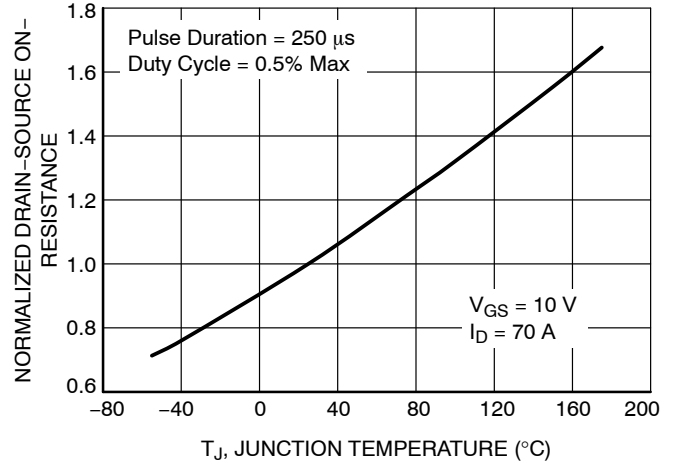
Figure 12. Normalized R$_{DS(on)}$ vs. Junction Temperature
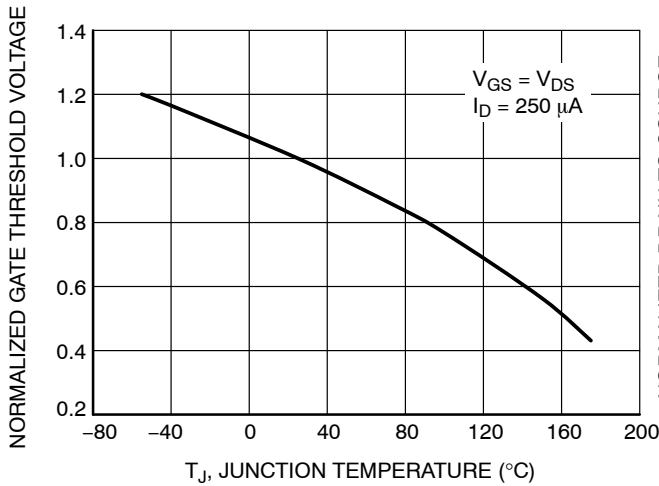
Figure 13. Normalized Gate Threshold Voltage vs. Temperature
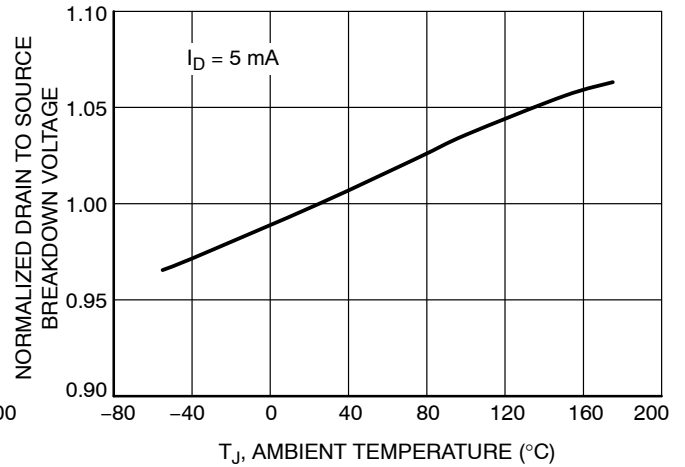
Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature
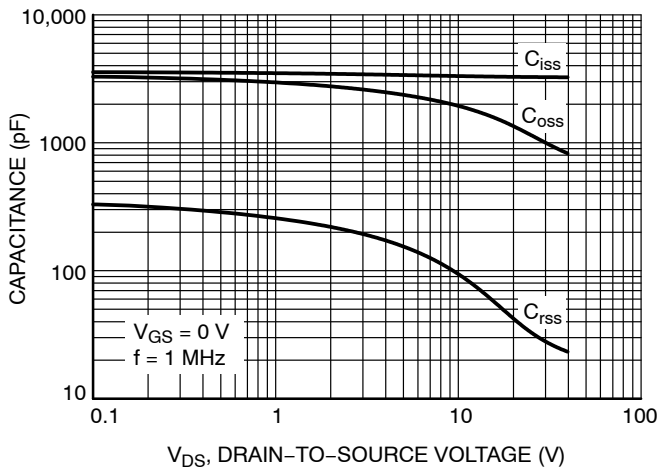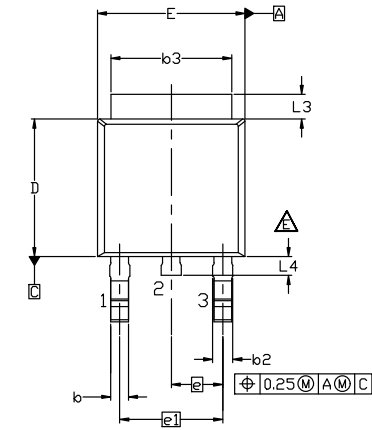

Figure 15. Capacitance vs. Drain to Source Voltage
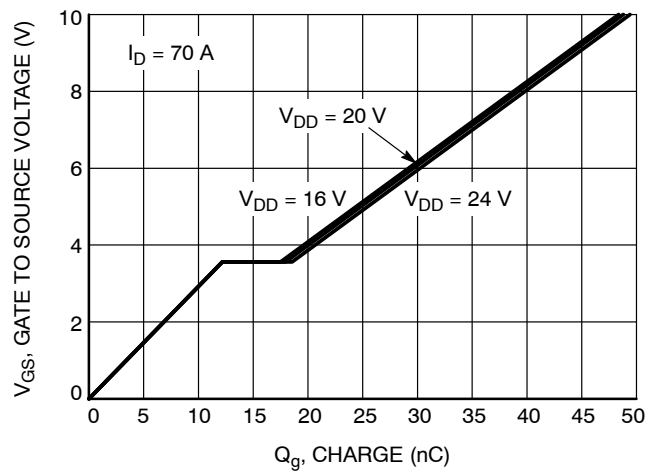
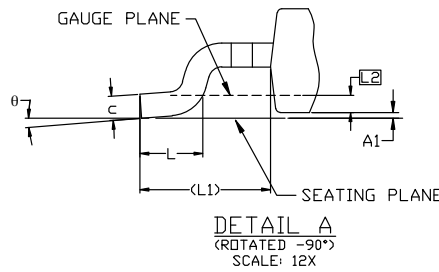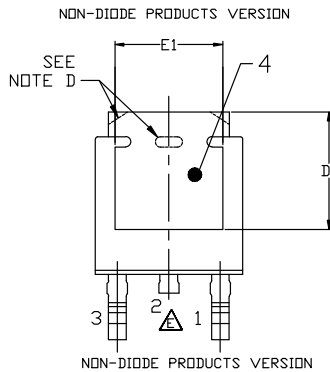
Figure 16. Gate Charge vs. Gate to Source Voltage

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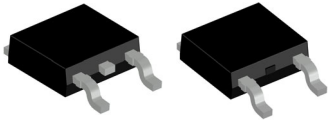
DPAK3 6.10x6.54x2.29, 4.57P
CASE 369AS
ISSUE B

DATE 20 DEC 2023

NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.
F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

NON-DIODE PRODUCTS VERSION

SEE NOTE D

NON-DIODE PRODUCTS VERSION

GAUGE PLANE

DETAIL A
(ROTATED -90°)
SCALE: 12X

SEE DETAIL A

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	–	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	---	---
E	6.35	6.54	6.73
E1	4.32	---	---
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	---	---	1.02
θ	0°	---	10°

5.55 MIN

6.50 MIN

6.40

2.85 MIN

1.25 MIN

2.286

4.572
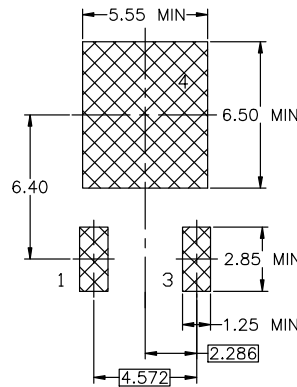
LAND PATTERN RECOMMENDATION
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXXX
XXXXXX
AYWWZZ
○
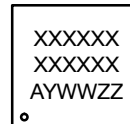
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

DOCUMENT NUMBER:	98AON13810G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK3 6.10x6.54x2.29, 4.57P	PAGE 1 OF 1

ADDITIONAL INFORMATION

◊