

# MOSFET – Dual, N-Channel, POWERTRENCH®

20 V, 3.7 A, 68 mΩ

## FDMA1028NZ

### General Description

This device is designed specifically as a single package solution for dual switching requirements in cellular handset and other ultra-portable applications. It features two independent N-Channel MOSFETs with low on-state resistance for minimum conduction losses. The MicroFET™ 2x2 offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

### Features

- 3.7 A, 20 V  
 $R_{DS(on)} = 68\text{ m}\Omega$  at  $V_{GS} = 4.5\text{ V}$   
 $R_{DS(on)} = 86\text{ m}\Omega$  at  $V_{GS} = 2.5\text{ V}$
- Low Profile – 0.8 mm Maximum – In the New Package MicroFET 2x2 mm
- HBM ESD Protection Level > 2 kV (Note 3)
- Free from Halogenated Compounds and Antimony Oxides
- This Device is Pb-Free, Halide Free and is RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)

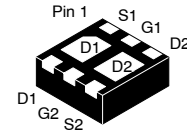
Symbol	Parameter	Ratings	Unit
V <sub>DS</sub>	Drain-Source Voltage	20	V
V <sub>GS</sub>	Gate-Source Voltage	±12	V
I <sub>D</sub>	Drain Current –Continuous (Note 1a) –Pulsed	3.7 6	A
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a) (Note 1b)	1.4 0.7	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

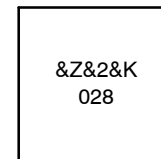
Symbol	Parameter	Ratings	Unit
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1a)	86 (Single Operation)	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1b)	173 (Single Operation)	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1c)	69 (Dual Operation)	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1d)	151 (Dual Operation)	

V <sub>DS</sub> MAX	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX
20 V	68 mΩ @ 4.5 V	3.7 A
	86 mΩ @ 2.5 V	



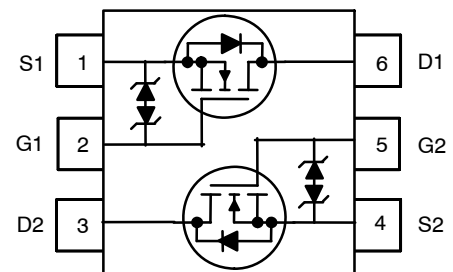
WDFN6 2x2, 0.65P  
(MicroFET 2x2)  
CASE 511DA

### MARKING DIAGRAM



&Z = Assembly Plant Code  
 &2 = 2-Digit Date Code  
 &K = 2-Digits Lot Run Traceability Code  
 028 = Device Code

### PIN CONNECTIONS



### ORDERING INFORMATION

Device	Package	Shipping†
FDMA1028NZ	WDFN6 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# FDMA1028NZ

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	20	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	-	15	-	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V	-	-	1	μA
I <sub>GSS</sub>	Gate-Body Leakage	V <sub>GS</sub> = ±12 V, V <sub>DS</sub> = 0 V	-	-	±10	μA

### ON CHARACTERISTICS (Note 2)

V <sub>GS(th)</sub>	Gate Threshold Voltage	I <sub>D</sub> = 250 μA, V <sub>DS</sub> = V <sub>GS</sub>	0.6	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	-	-4	-	mV/°C
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.7 A	-	37	68	mΩ
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 3.3 A	-	50	86	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.7 A, T <sub>J</sub> = 125°C	-	53	90	
g <sub>FS</sub>	Forward Transconductance	I <sub>D</sub> = 3.7 A, V <sub>DS</sub> = 10 V	-	16	-	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	-	340	-	pF
C <sub>oss</sub>	Output Capacitance		-	80	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	60	-	pF
R <sub>g</sub>	Gate Resistance		-	-	25	Ω

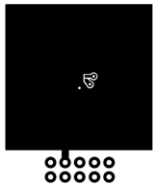
### SWITCHING CHARACTERISTICS (Note 2)

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 10 V, I <sub>D</sub> = 1 A V <sub>GS</sub> = 4.5 V, R <sub>GEN</sub> = 6 Ω	-	8	16	ns
t <sub>r</sub>	Turn-On Rise Time		-	8	16	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	14	26	ns
t <sub>f</sub>	Turn-Off Fall Time		-	3	6	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.7 A, V <sub>GS</sub> = 4.5 V	-	4	6	nC
Q <sub>gs</sub>	Gate-Source Charge		-	0.7	-	nC
Q <sub>gd</sub>	Gate-Drain Charge		-	1.1	-	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>θJC</sub> is guaranteed by design while R<sub>θJA</sub> is determined by the user's board design.

- R<sub>θJA</sub> = 86°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB. For single operation.
- R<sub>θJA</sub> = 173°C/W when mounted on a minimum pad of 2 oz copper. For single operation.
- R<sub>θJA</sub> = 69°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB. For dual operation.
- R<sub>θJA</sub> = 151°C/W when mounted on a minimum pad of 2 oz copper. For dual operation.



- a. 86°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



- b. 173°C/W when mounted on a minimum pad of 2 oz copper.



- c. 69°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



- d. 151°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS

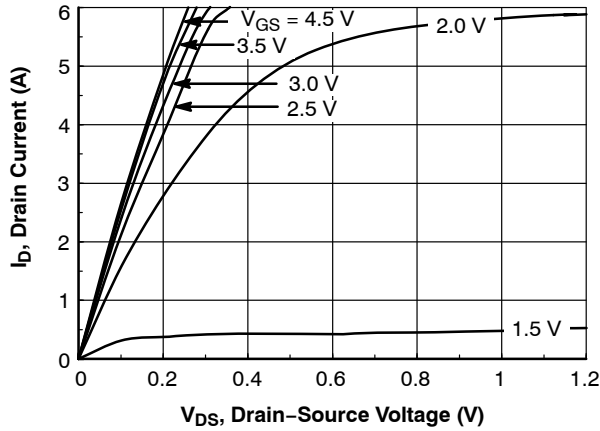


Figure 1. On-Region Characteristics

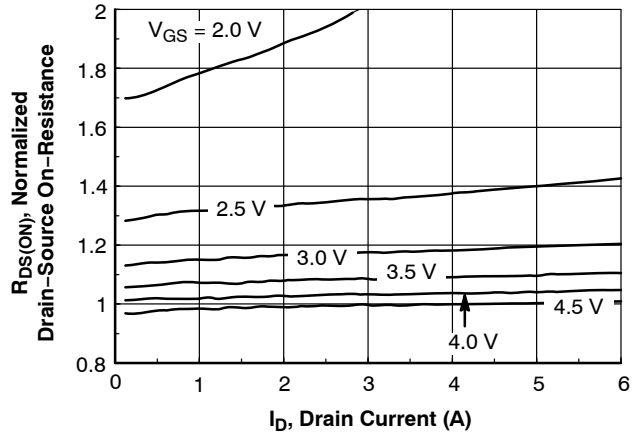


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

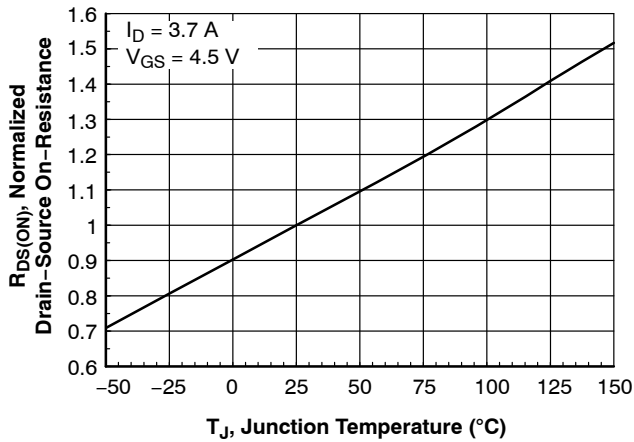


Figure 3. On-Resistance Variation with Temperature

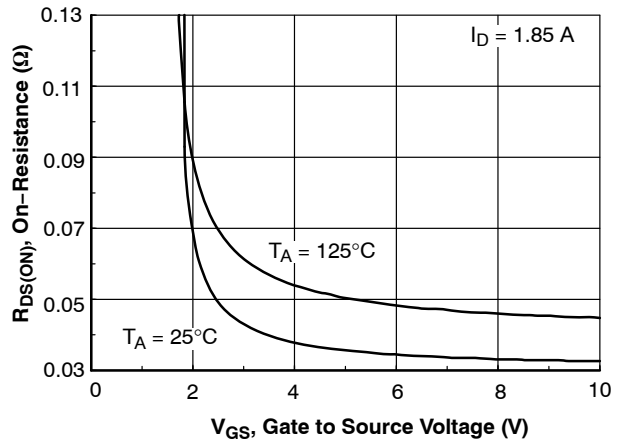


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

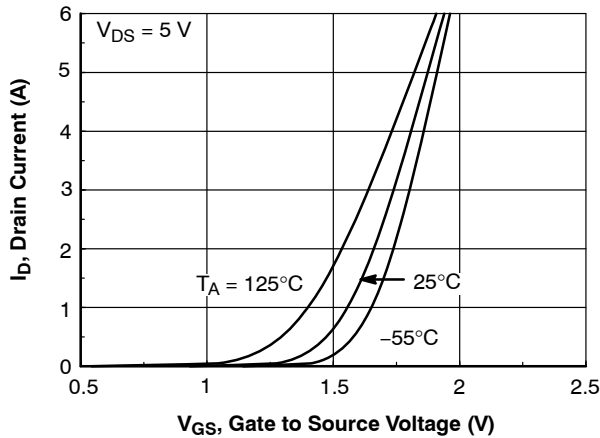


Figure 5. Transfer Characteristics

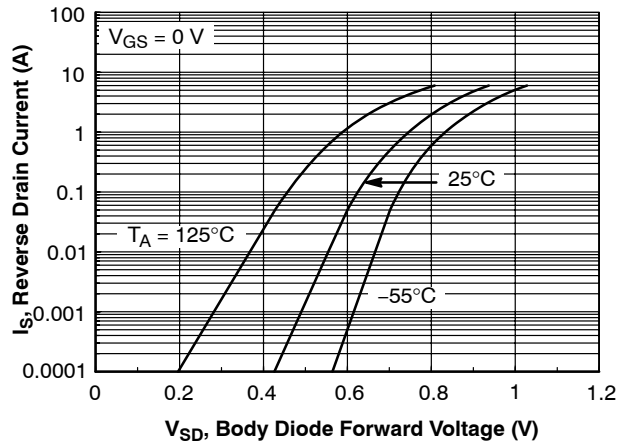


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (continued)

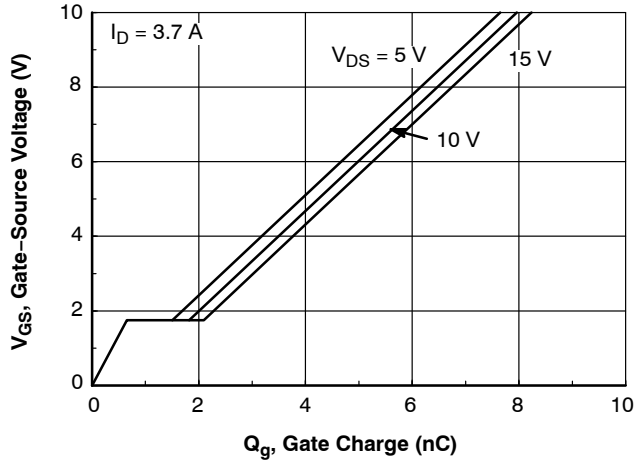


Figure 7. Gate Charge Characteristics

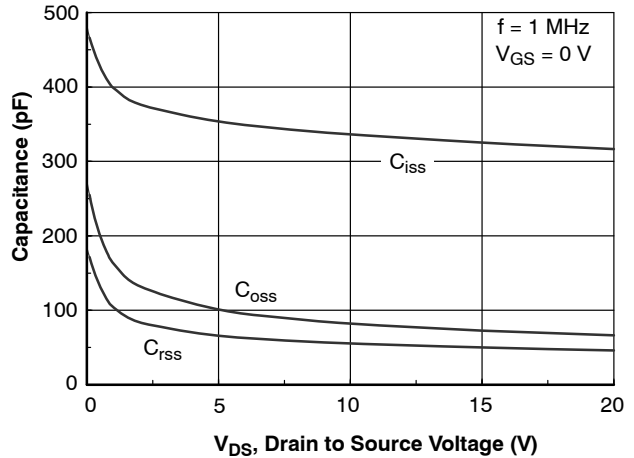


Figure 8. Capacitance Characteristics

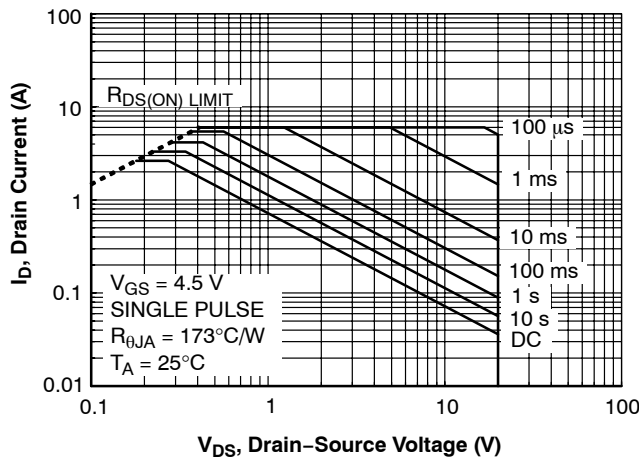


Figure 9. Maximum Safe Operating Area

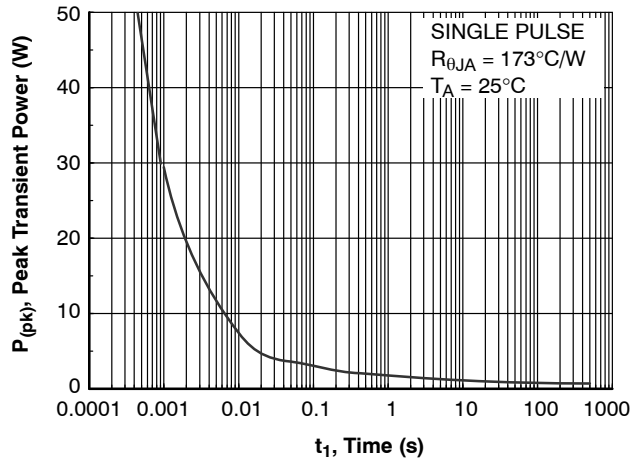


Figure 10. Single Pulse Maximum Power Dissipation

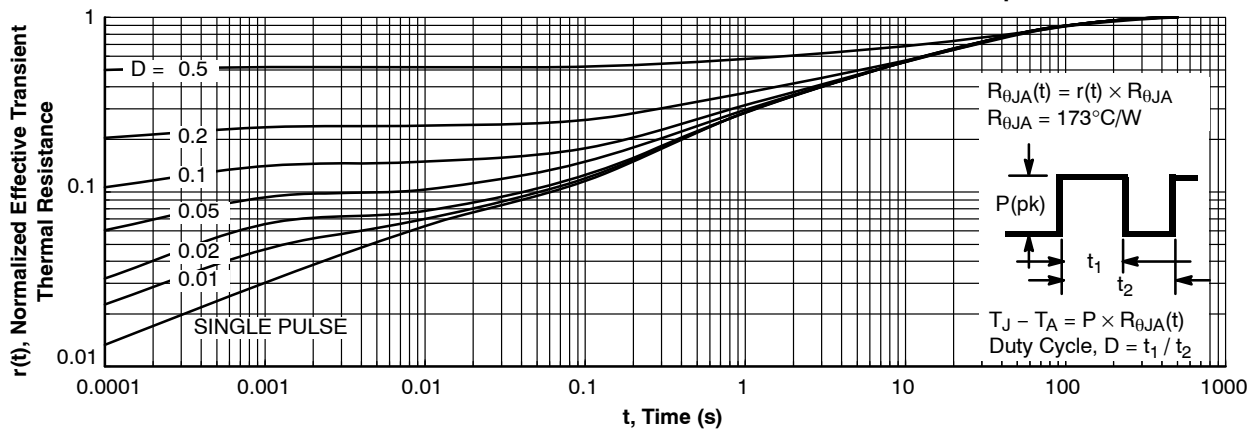


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.  
Transient thermal response will change depending on the circuit board design.

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# MECHANICAL CASE OUTLINE

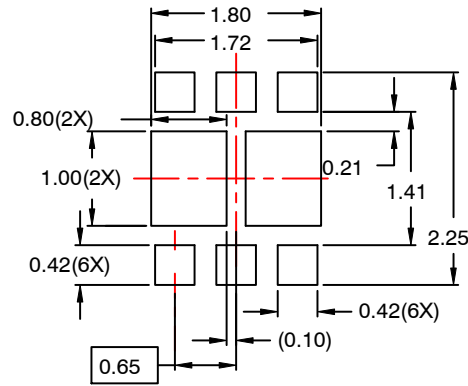
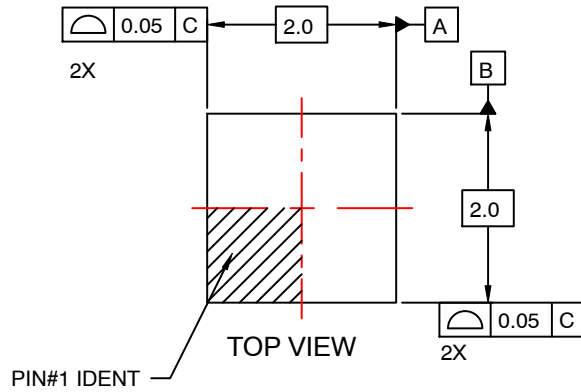
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ON Semiconductor®

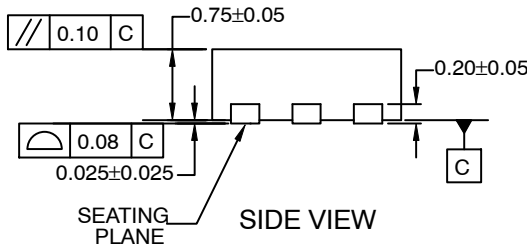


WDFN6 2x2, 0.65P  
CASE 511DA  
ISSUE O

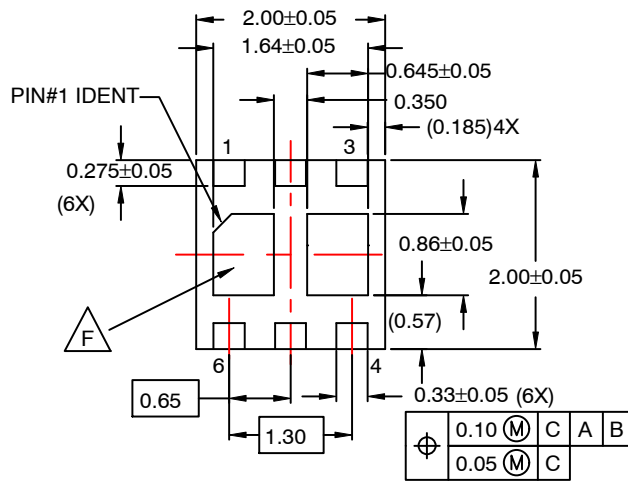
DATE 31 JUL 2016



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

- A. CONFORM TO JEDEC REGISTRATIONS MO-229, VARIATION VCCC, EXCEPT WHERE NOTED.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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