

MOSFET – Single, P-Channel, POWERTRENCH®

-20 V, -7.8 A, 30 mΩ

FDMA510PZ

General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance.

The MicroFET™ 2x2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Features

- Max $R_{DS(on)}$ = 30 mΩ at $V_{GS} = -4.5$ V, $I_D = -7.8$ A
- Max $R_{DS(on)}$ = 37 mΩ at $V_{GS} = -2.5$ V, $I_D = -6.6$ A
- Max $R_{DS(on)}$ = 50 mΩ at $V_{GS} = -1.8$ V, $I_D = -5.5$ A
- Max $R_{DS(on)}$ = 90 mΩ at $V_{GS} = -1.5$ V, $I_D = -2.0$ A
- Low Profile – 0.8 mm Maximum in the New Package MicroFET 2x2 mm
- HBM ESD Protection Level > 3 kV Typical (Note 3)
- Free from Halogenated Compounds and Antimony Oxides
- This Device is Pb-Free, Halide Free and is RoHS Compliant

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

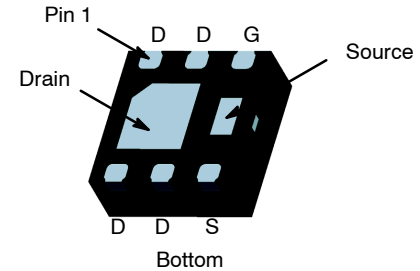
Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	± 8	V
I_D	Drain Current		A
	– Continuous (Note 1a)	-7.8	
	– Pulsed	-24	
P_D	Power Dissipation (Note 1a)	2.4	W
	Power Dissipation (Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

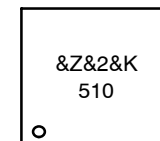
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
-20 V	30 mΩ @ -4.5 V	-7.8 A
	37 mΩ @ -2.5 V	
	50 mΩ @ -1.8 V	
	90 mΩ @ -1.5 V	



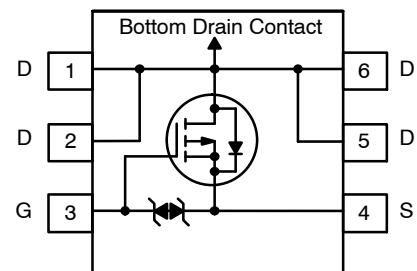
WDFN6 2x2, 0.65P
 (MicroFET 2x2)
 CASE 511CZ

MARKING DIAGRAM



&Z = Assembly Plant Code
 &2 = 2-Digit Date Code
 &K = 2-Digits Lot Run Traceability Code
 510 = Specific Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
FDMA510PZ	WDFN8 MicroFET 2X2 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FDMA510PZ

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
--------	-----------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0 V	-20	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	-13	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -16 V, V _{GS} = 0 V	-	-	-1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±8 V, V _{DS} = 0 V	-	-	±10	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = -250 μA	-0.4	-0.7	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25°C	-	3	-	mV/°C
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = -4.5 V, I _D = -7.8 A	-	27	30	mΩ
		V _{GS} = -2.5 V, I _D = -6.6 A	-	34	37	
		V _{GS} = -1.8 V, I _D = -5.5 A	-	46	50	
		V _{GS} = -1.5 V, I _D = -2.0 A	-	60	90	
		V _{GS} = -4.5 V, I _D = -7.8 A, T _J = 125°C	-	36	40	
g _{FS}	Forward Transconductance	V _{DD} = -5 V, I _D = -7.8 A	-	26	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	-	1110	1480	pF
C _{oss}	Output Capacitance		-	205	275	pF
C _{rss}	Reverse Transfer Capacitance		-	185	280	pF

SWITCHING CHARACTERISTICS

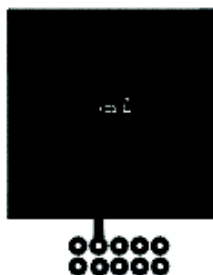
t _{d(on)}	Turn-On Delay Time	V _{DD} = -10 V, I _D = -7.8 A, V _{GS} = -4.5 V, R _{GEN} = 6 Ω	-	7	14	ns
t _r	Rise Time		-	9	18	ns
t _{d(off)}	Turn-Off Delay Time		-	125	200	ns
t _f	Fall Time		-	64	103	ns
Q _g	Total Gate Charge		V _{DD} = -5 V, I _D = -7.8 A, V _{GS} = -4.5 V	-	19	27
Q _{gs}	Gate to Source Charge	-		2.1	-	nC
Q _{gd}	Gate to Drain "Miller" Charge	-		4.2	-	nC

DRAIN-SOURCE CHARACTERISTICS

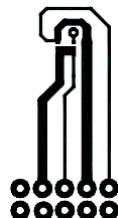
I _S	Maximum Continuous Drain-Source Diode Forward Current	-	-	-2	A	
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = -2 A	-	-0.8	-1.2	V
t _{rr}	Reverse Recovery Time	I _F = -7.8 A, di/dt = 100 A / μs	-	66	106	ns
Q _{rr}	Reverse Recovery Charge		-	44	71	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θJA} is determined by the user's board design.



a. 52°C/W when mounted on a 1 in² pad of 2 oz copper



b. 145°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

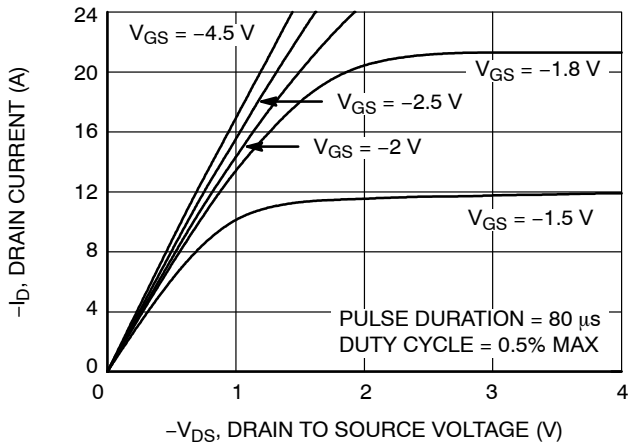


Figure 1. On-Region Characteristics

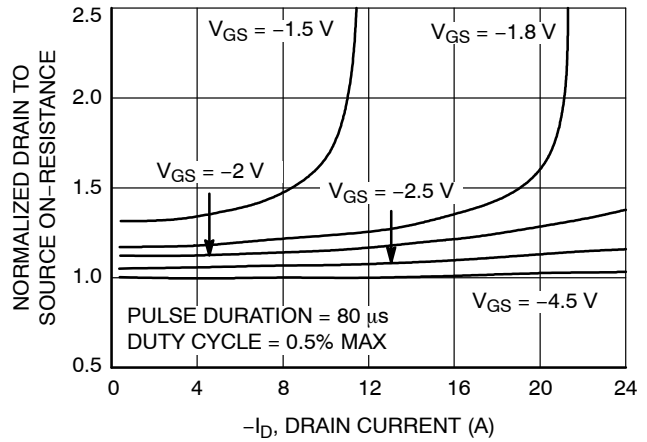


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

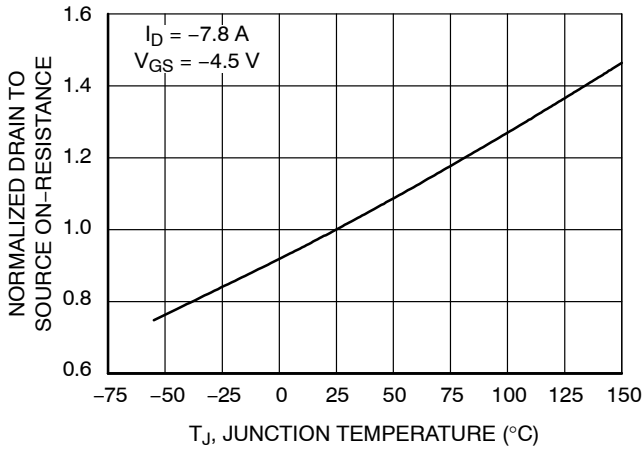


Figure 3. Normalized On-Resistance vs. Junction Temperature

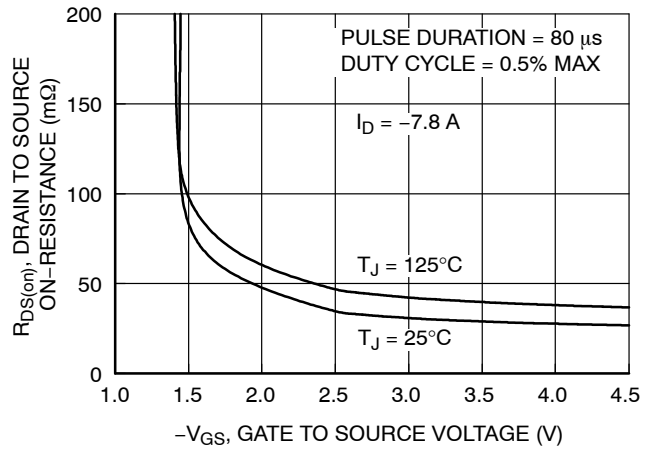


Figure 4. On-Resistance vs. Gate to Source Voltage

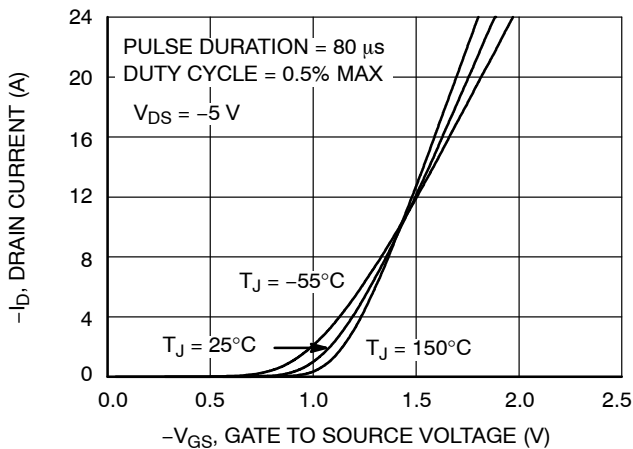


Figure 5. Transfer Characteristics

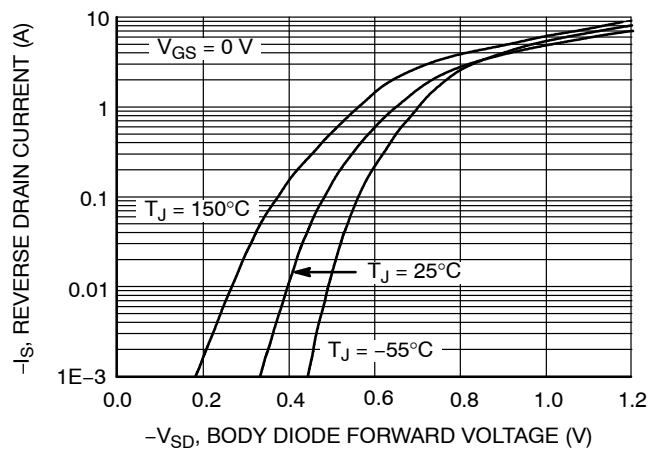


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)

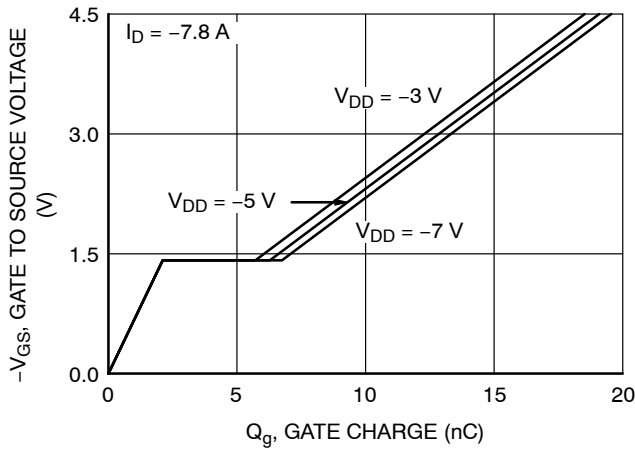


Figure 7. Gate Charge Characteristics

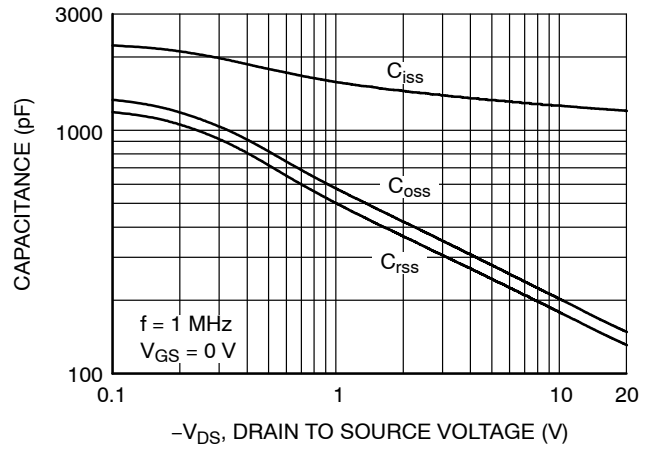


Figure 8. Capacitance vs. Drain to Source Voltage

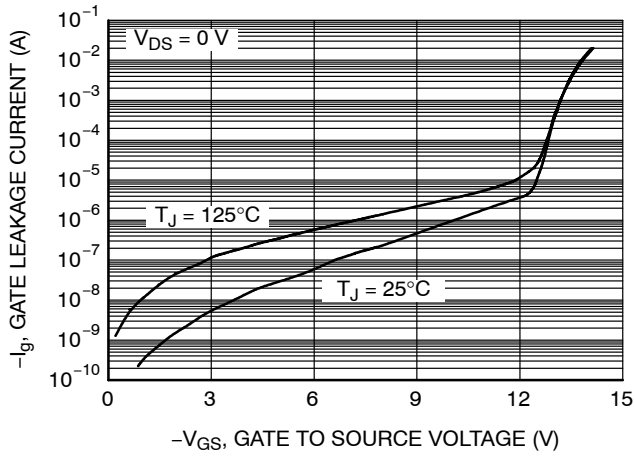


Figure 9. Gate Leakage Current vs. Gate to Source Voltage

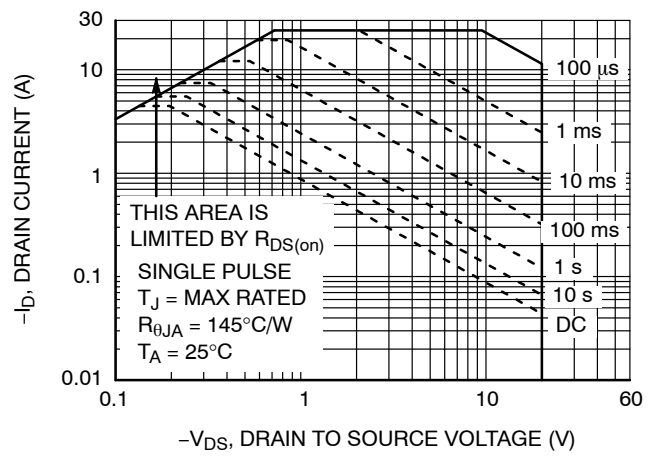


Figure 10. Forward Bias Safe Operating Area

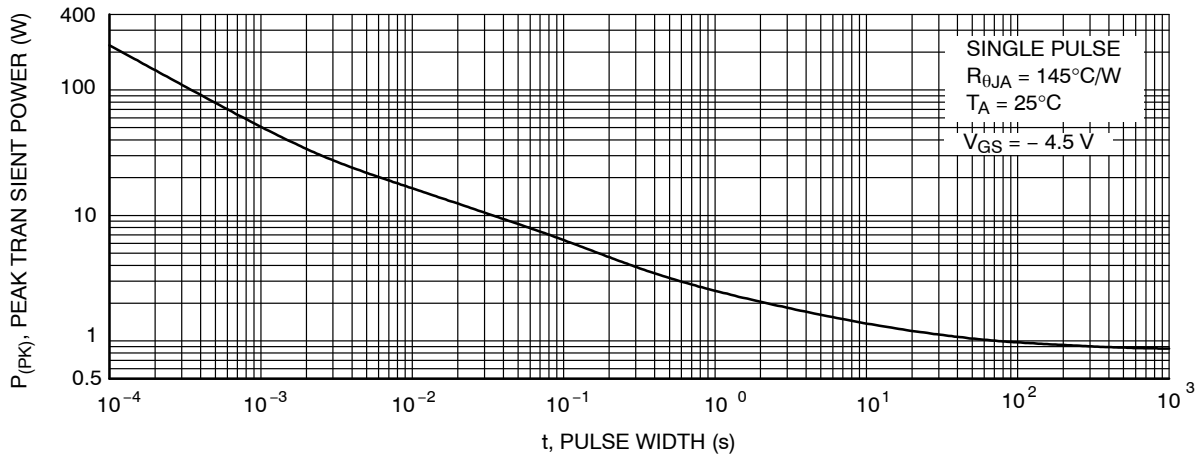


Figure 11. Single Pulse Maximum Power Dissipation

FDMA510PZ

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)

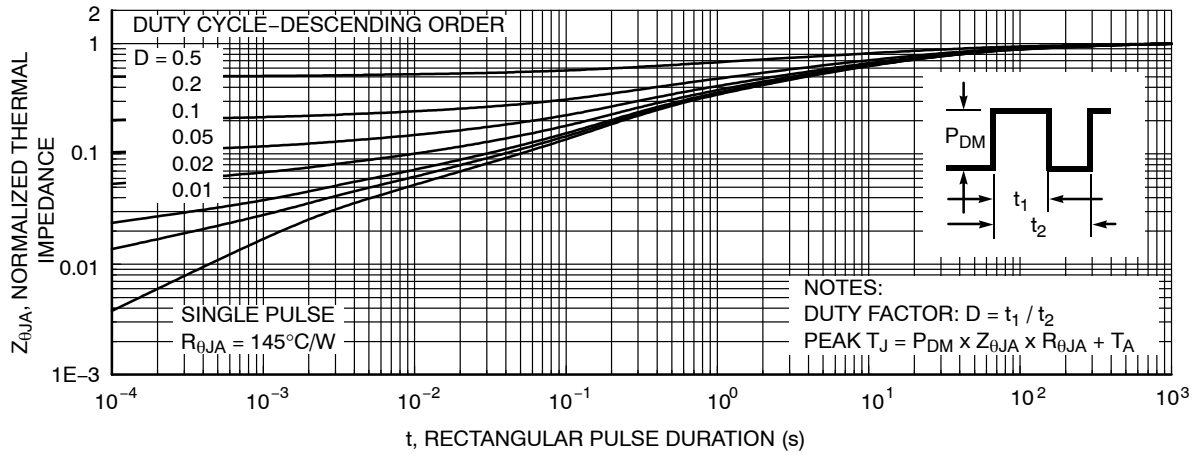


Figure 12. Transient Thermal Response Curve

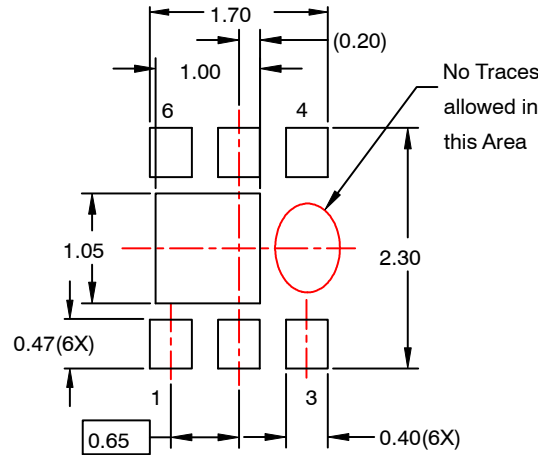
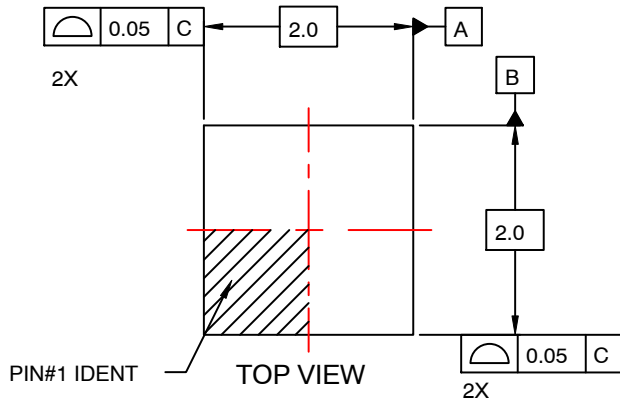
POWERTRENCH is registered trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

MicroFET is trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

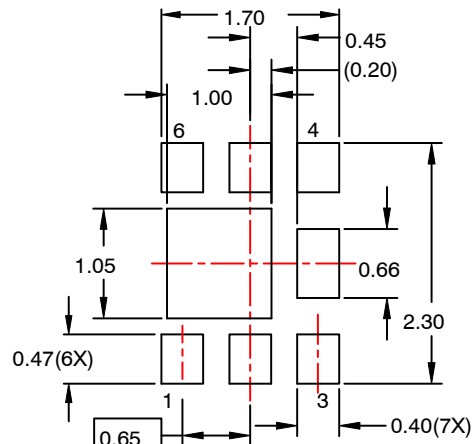
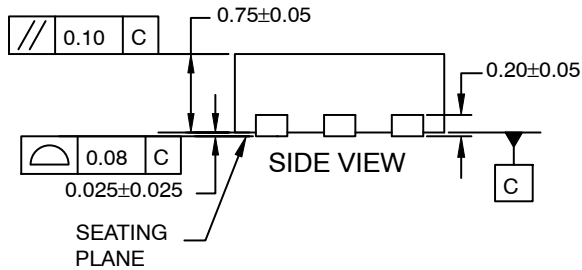


WDFN6 2x2, 0.65P
CASE 511CZ
ISSUE O

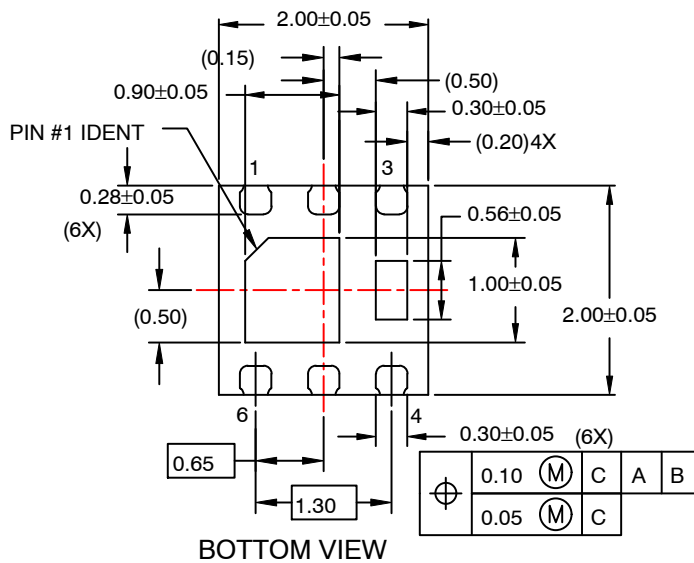
DATE 31 JUL 2016



**RECOMMENDED
 LAND PATTERN OPT 1**



**RECOMMENDED
 LAND PATTERN OPT 2**



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

DOCUMENT NUMBER:	98AON13614G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	WDFN6 2X2, 0.65P	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales