

# MOSFET – N-Channel, POWERTRENCH®

30 V, 9.0 A, 16 mΩ

## FDMA8878, FDMA8878-F130

### General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been optimized for  $R_{DS(on)}$ , switching performance.

### Features

- Max  $R_{DS(on)}$  = 16 mΩ @  $V_{GS} = 10\text{ V}$ ,  $I_D = 9.0\text{ A}$
- Max  $R_{DS(on)}$  = 19 mΩ @  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 8.5\text{ A}$
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- Fast Switching Speed
- Pb-Free, Halide Free and RoHS Compliant

### Applications

- DC-DC Buck Converters
- Load Switch in NB
- Notebook Battery Power Management

### ABSOLUTE MAXIMUM RATINGS

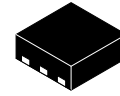
$T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage (Note 3)	$\pm 20$	V
$I_D$	Drain Current Continuous (Package Limited), $T_C = 25^\circ\text{C}$ Continuous, $T_A = 25^\circ\text{C}$ (Note 1a) Pulsed	10	A
		9.0 40	
$P_D$	Power Dissipation, $T_A = 25^\circ\text{C}$ (Note 1a) (Note 1b)	2.4	W
		0.9	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

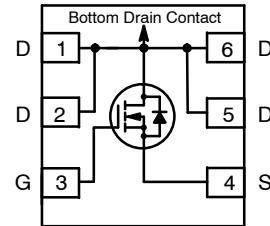
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

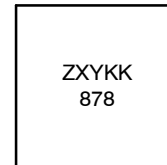
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a) (Note 1b)	52 145	$^\circ\text{C}/\text{W}$



WDFN6  
CASE 511CZ

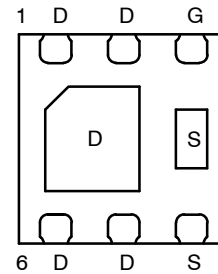


### MARKING DIAGRAM



Z = Assembly Plant Code  
XY = 2-Digit Date Code  
KK = Lot Run Code  
878 = Specific Device Code

### PIN ASSIGNMENT



### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# FDMA8878, FDMA8878-F130

**ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{V}$	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	26	–	mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{V}, V_{GS} = 0 \text{V}$	–	–	1	$\mu\text{A}$
$I_{GSS}$	Gate–Body Leakage	$V_{GS} = \pm 20 \text{V}, V_{DS} = 0 \text{V}$	–	–	$\pm 100$	nA

**ON CHARACTERISTICS**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.2	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	–5	–	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On–Resistance	$I_D = 9.0 \text{A}, V_{GS} = 10 \text{V}$ ,	–	13	16	m $\Omega$
		$I_D = 8.5 \text{A}, V_{GS} = 4.5 \text{V}$	–	16	19	
		$I_D = 9.0 \text{A}, V_{GS} = 10 \text{V}$ , $T_J = 125^\circ\text{C}$	–	17	21	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5 \text{V}, I_D = 9.0 \text{A}$	–	41	–	S

**DYNAMIC CHARACTERISTICS**

$C_{iss}$	Input Capacitance	$V_{DS} = -15 \text{V}, V_{GS} = 0 \text{V}$ , $f = 1.0 \text{MHz}$	–	539	720	pF
$C_{oss}$	Output Capacitance		–	172	230	
$C_{rss}$	Reverse Transfer Capacitance		–	24	35	
$R_G$	Gate Resistance		–	1.3	–	

**SWITCHING CHARACTERISTICS**

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15 \text{V}, I_D = 9.0 \text{A}$ , $V_{GS} = 10 \text{V}, R_{GEN} = 6 \Omega$	–	6	12	ns
$t_r$	Rise Time		–	2	10	
$t_{d(off)}$	Turn–Off Delay Time		–	14	25	
$t_f$	Fall Time		–	2	10	
$Q_g(TOT)$	Total Gate Charge	$V_{GS} = 0 \text{V to } 10 \text{V}, V_{DD} = 15 \text{V}$ , $I_D = 9.0 \text{A}$	–	8.5	12	nC
		$V_{GS} = 0 \text{V to } 4.5 \text{V}, V_{DD} = 15 \text{V}$ , $I_D = 9.0 \text{A}$	–	4.1	5.8	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 15 \text{V}, I_D = 9.0 \text{A}$	–	1.6	–	nC
$Q_{gd}$	Gate to Drain “Miller” Charge		–	1.2	–	

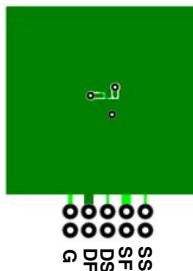
**DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{V}, I_S = 2.0 \text{A}$ (Note 2)	–	0.75	1.2	V
		$V_{GS} = 0 \text{V}, I_S = 9.0 \text{A}$ (Note 2)	–	0.86	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 9.0 \text{A}, di/dt = 100 \text{A}/\mu\text{s}$	–	16	28	ns
$Q_{rr}$	Reverse Recovery Charge		–	4	10	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**NOTES:**

- $R_{\theta JA}$  is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user’s board design.



a)  $52^\circ\text{C}/\text{W}$  when mounted on a  $1 \text{ in}^2$  pad of 2 oz. copper.



b)  $145^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz. copper.

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%
- As an N–ch device, the negative  $V_{GS}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

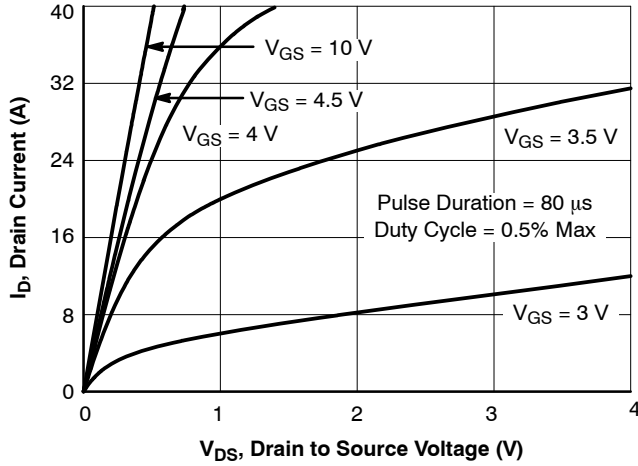


Figure 1. On-Region Characteristics

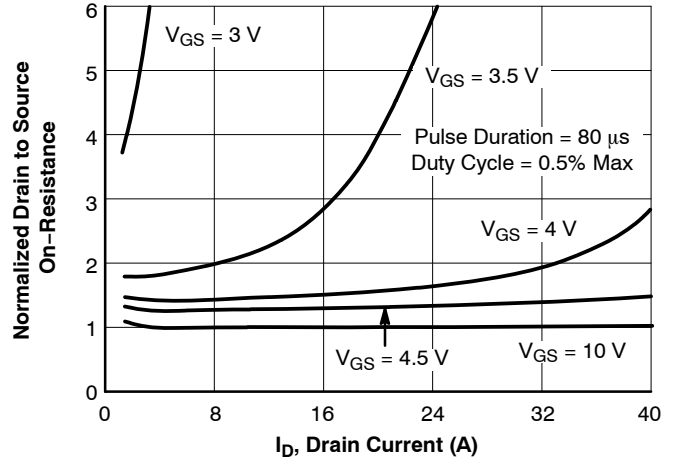


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

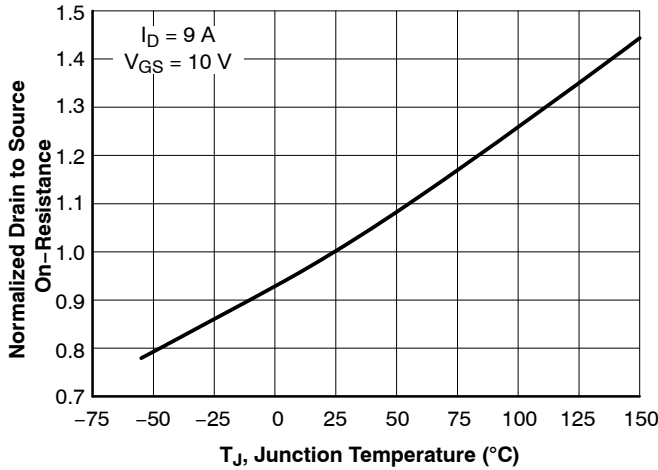


Figure 3. Normalized On-Resistance vs. Junction Temperature

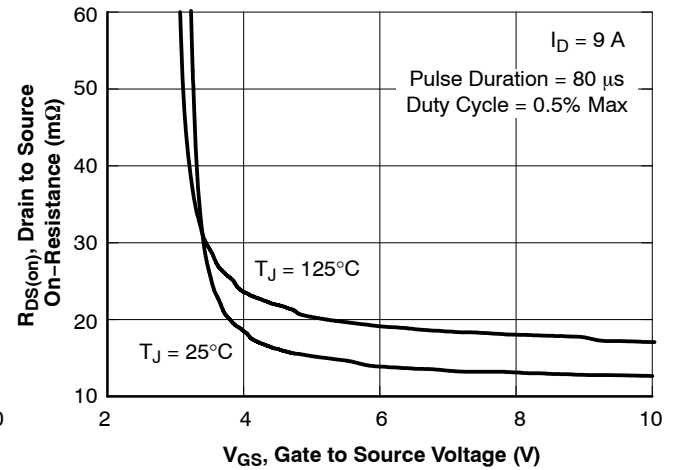


Figure 4. On-Resistance vs. Gate-to-Source Voltage

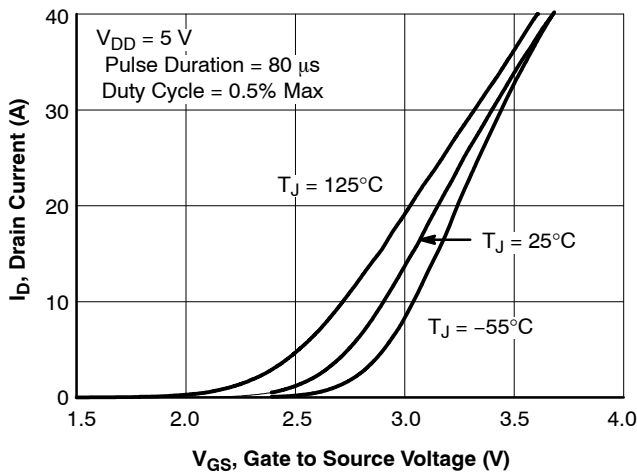


Figure 5. Transfer Characteristics

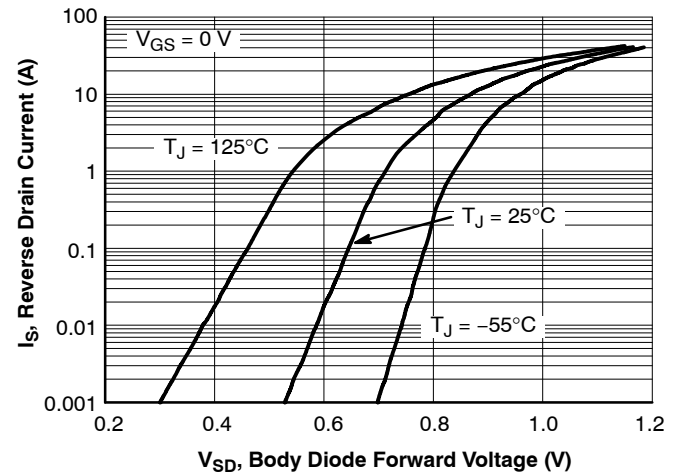


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

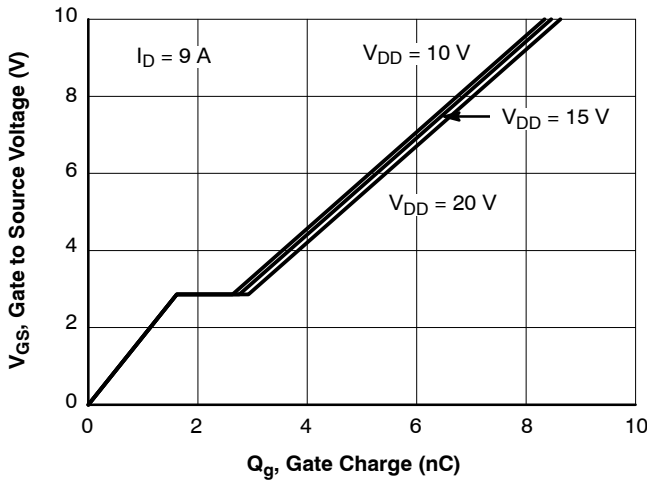


Figure 7. Gate Charge Characteristics

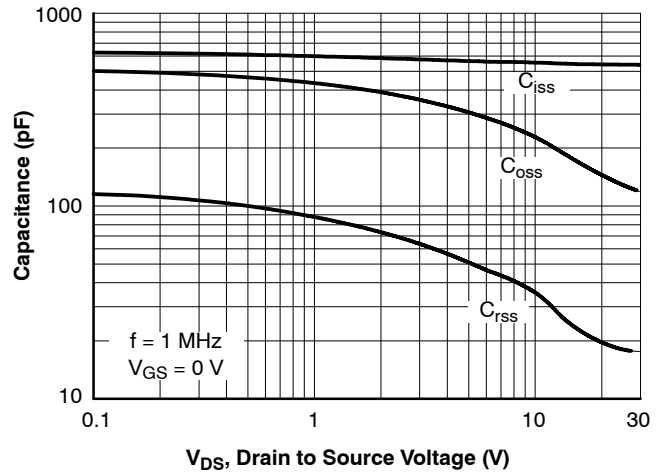


Figure 8. Capacitance Characteristics

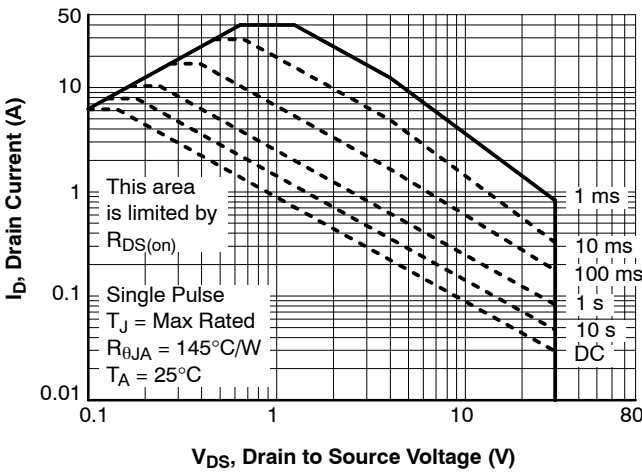


Figure 9. Maximum Safe Operating Area

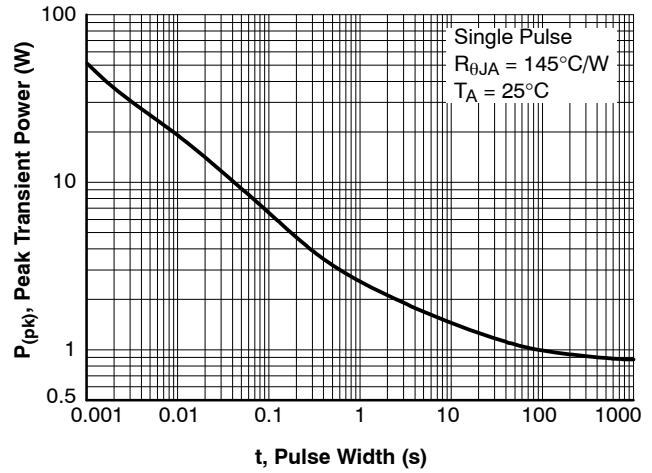


Figure 10. Single Pulse Maximum Power Dissipation

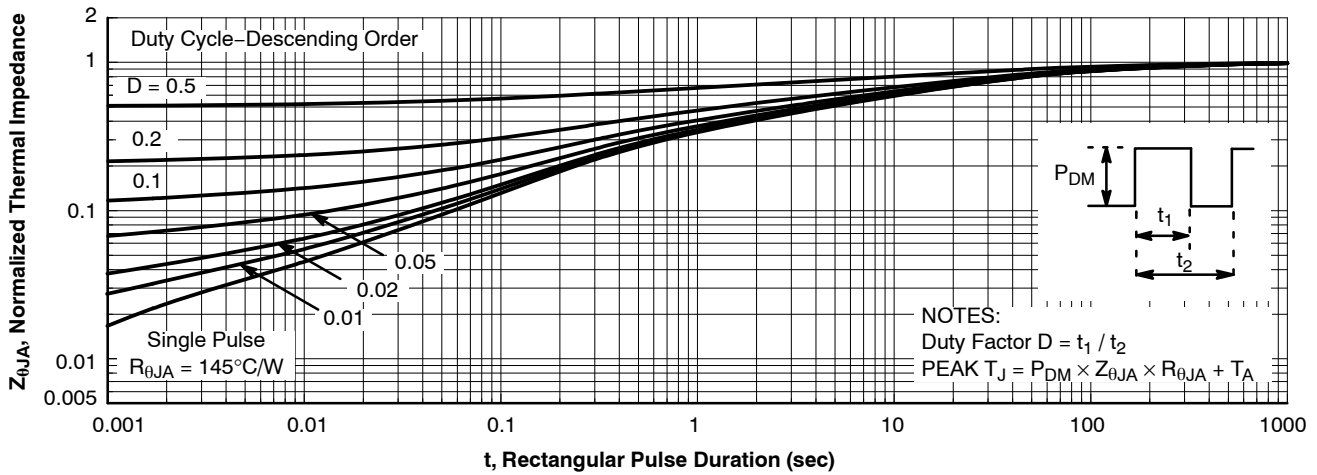


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

## FDMA8878, FDMA8878-F130

### ORDERING INFORMATION

Device Order Number	Package Type	Pin 1 Orientation in Tape Cavity	Shipping†
FDMA8878	WDFN6 (Pb-Free/Halide Free)	Top Left	3000 / Tape & Reel
FDMA8878-F130	WDFN6 (Pb-Free/Halide Free)	Top Right	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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# MECHANICAL CASE OUTLINE

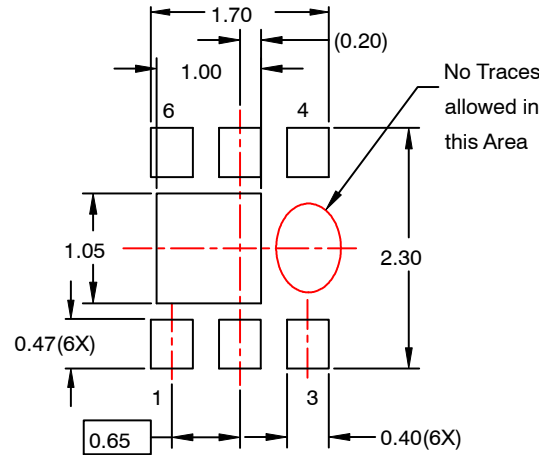
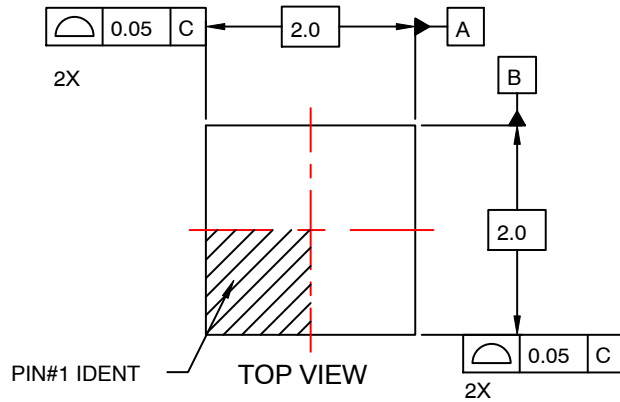
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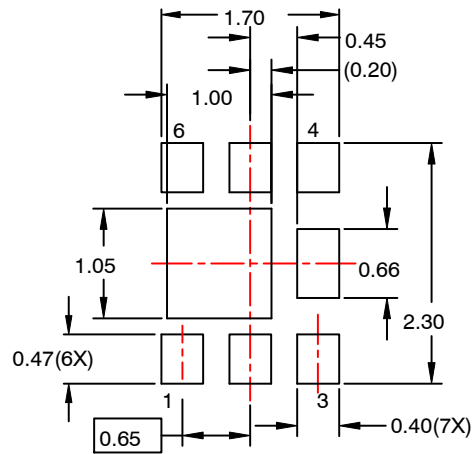
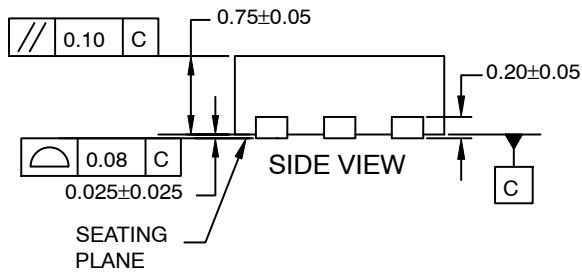


WDFN6 2x2, 0.65P  
CASE 511CZ  
ISSUE O

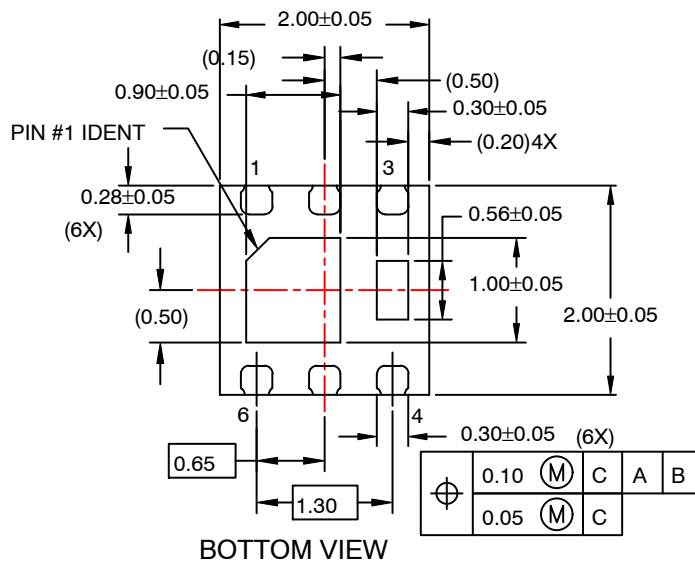
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RECOMMENDED  
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RECOMMENDED  
LAND PATTERN OPT 2



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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