

SyncFET™ – N-Channel, POWERTRENCH®

30 V, 21 A, 4.4 mΩ

FDMC0310AS, FDMC0310AS-F127

General Description

The FDMC0310AS has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic schottky body diode.

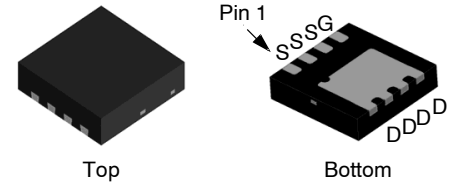
Features

- Max $r_{DS(on)}$ = 4.4 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 19\text{ A}$
- Max $r_{DS(on)}$ = 5.2 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 17.5\text{ A}$
- Advanced Package and Silicon Combination for Low $r_{DS(on)}$ and High Efficiency
- SyncFET Schottky Body Diode
- MSL1 Robust Package Design
- 100% UIL Tested
- These Devices are Pb-Free and are RoHS Compliant

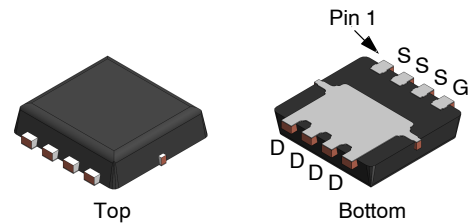
Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/GPU Low Side Switch
- Networking Point of Load Low Side Switch
- Telecom Secondary Side Rectification

$V_{DS\text{ MAX}}$	$r_{DS(on)\text{ MAX}}$	$I_D\text{ MAX}$
30 V	4.4 mΩ @ 10 V	21 A
	5.2 mΩ @ 4.5 V	

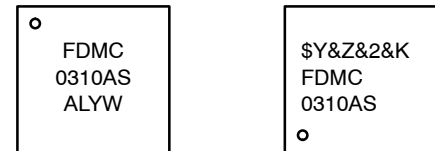


WDFN8 3.3x3.3, 0.65P
(MLP SAWN)
CASE 511DH



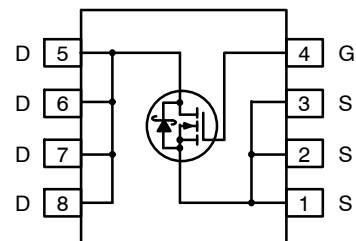
WDFN8 3.3x3.3, 0.65P
(MLP PUNCH)
CASE 511DQ - Option C

MARKING DIAGRAM



FDMC0310AS = Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week
\$Y = onsemi Logo
&Z = Assembly Plant Code
&2 = Numeric Date Code
&K = Lot Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

FDMC0310AS, FDMC0310AS-F127

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit	
V_{DS}	Drain to Source Voltage	30	V	
V_{DSst}	Drain to Source Transient Voltage ($t_{\text{Transient}} < 100 \text{ ns}$)	33	V	
V_{GS}	Gate to Source Voltage (Note 1)	± 20	V	
I_D	Drain Current	Continuous, $T_C = 25^\circ\text{C}$	21	A
		Continuous, $T_A = 25^\circ\text{C}$ (Note 3a)	19	A
		Pulsed	100	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	66	mJ	
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	36	W
		$T_A = 25^\circ\text{C}$ (Note 3a)	2.4	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+150$	$^\circ\text{C}$	

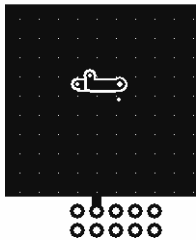
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
- E_{AS} of 66 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 0.3 \text{ mH}$, $I_{AS} = 21 \text{ A}$, $V_{DD} = 27 \text{ V}$, $V_{GS} = 10 \text{ V}$. 100% tested at $L = 3 \text{ mH}$, $I_{AS} = 10.2 \text{ A}$.

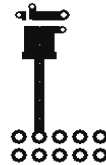
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 3a)	53	

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- a. $53^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



- b. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

FDMC0310AS, FDMC0310AS-F127

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0 V	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, referenced to 25°C	–	26	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	–	–	500	μA
I _{GSS}	Gate to Source Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V	–	–	100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 1 mA	1.2	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 10 mA, referenced to 25°C	–	–5	–	mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 19 A	–	3.8	4.4	mΩ
		V _{GS} = 4.5 V, I _D = 17.5 A	–	4.5	5.2	
		V _{GS} = 10 V, I _D = 19 A, T _J = 125°C	–	4.5	5.8	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 19 A	–	106	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	–	2380	3165	pF
C _{oss}	Output Capacitance		–	885	1175	pF
C _{rss}	Reverse Transfer Capacitance		–	100	150	pF
R _g	Gate Resistance		0.1	0.7	2.5	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 15 V, I _D = 19 A V _{GS} = 10 V, R _{GEN} = 6 Ω	–	11	20	ns
t _r	Rise Time		–	5	10	ns
t _{d(off)}	Turn-Off Delay Time		–	30	48	ns
t _f	Fall Time		–	4	10	ns
Q _g	Total Gate Charge	V _{GS} = 0 V to 10 V V _{DD} = 15 V, I _D = 19 A	–	37	52	nC
		V _{GS} = 0 V to 4.5 V V _{DD} = 15 V, I _D = 19 A	–	18	25	nC
Q _{gs}	Gate to Source Charge	V _{DD} = 15 V, I _D = 19 A	–	6	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	6	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2 A (Note 4)	–	0.6	0.8	V
		V _{GS} = 0 V, I _S = 19 A (Note 4)	–	0.8	1.2	V
t _{rr}	Reverse Recovery Time	I _F = 19 A, di/dt = 300 A/μs	–	29	47	ns
Q _{rr}	Reverse Recovery Charge		–	33	53	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

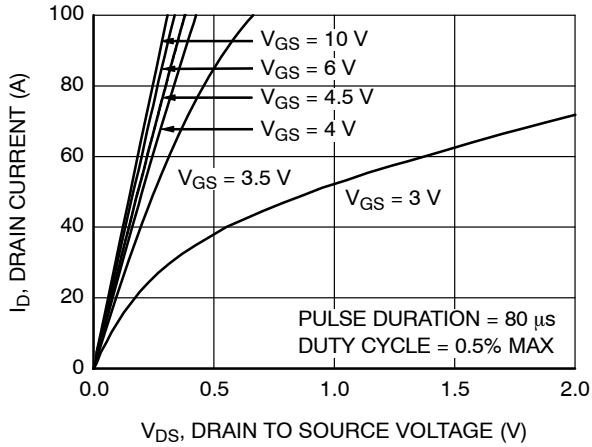


Figure 1. On Region Characteristics

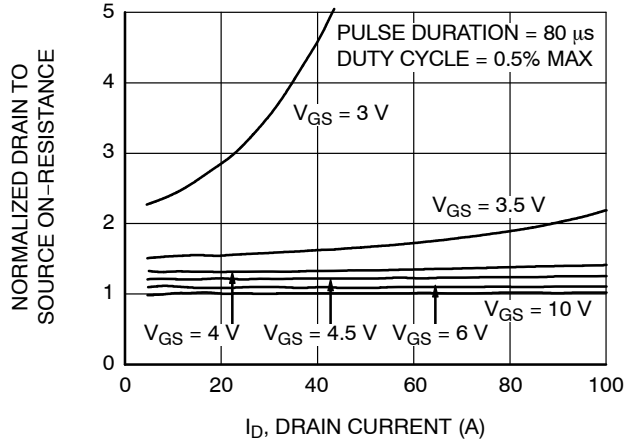


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

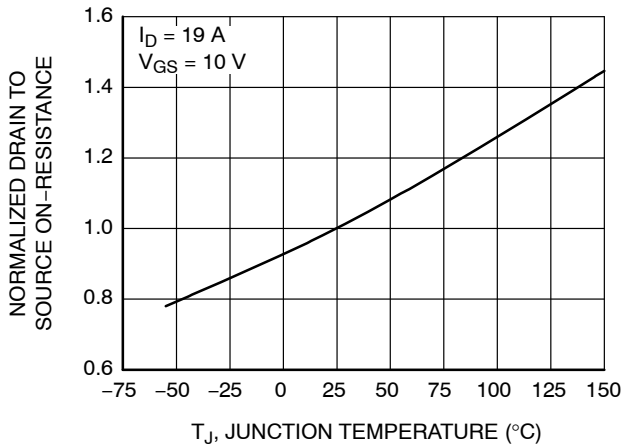


Figure 3. Normalized On-Resistance vs. Junction Temperature

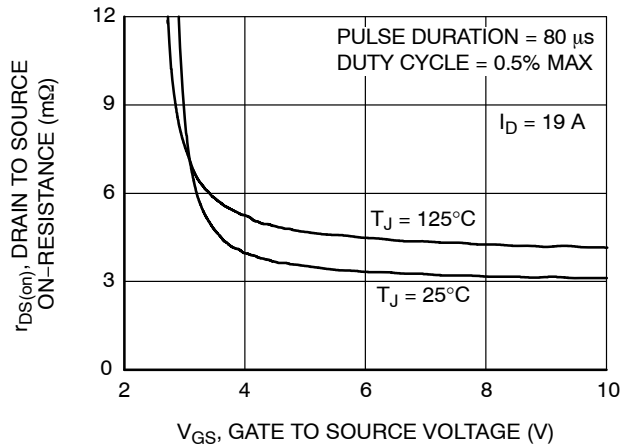


Figure 4. On-Resistance vs. Gate to Source Voltage

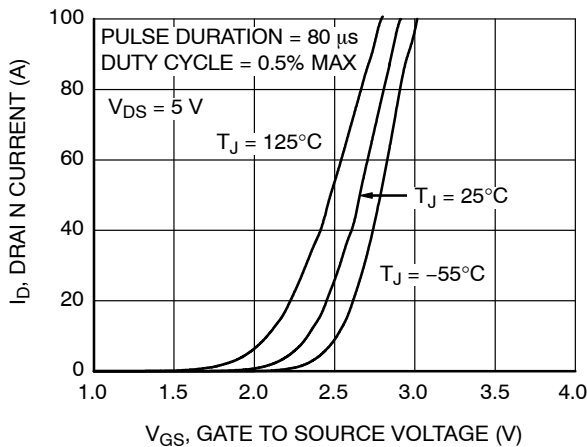


Figure 5. Transfer Characteristics

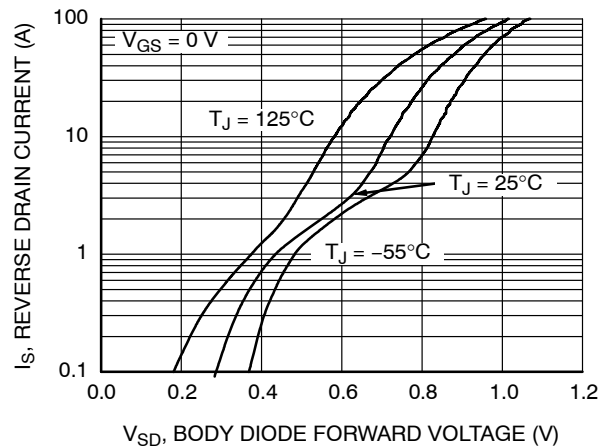


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

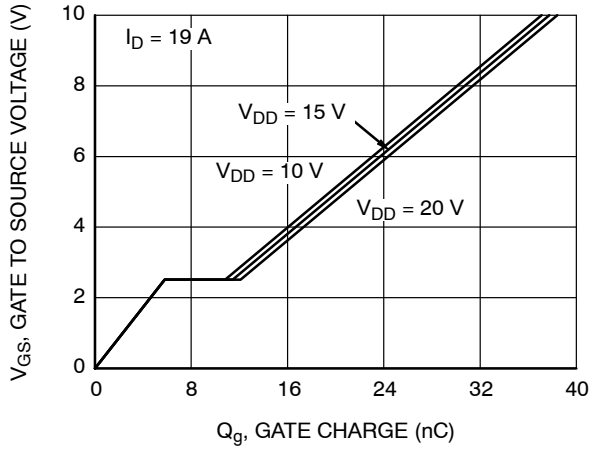


Figure 7. Gate Charge Characteristics

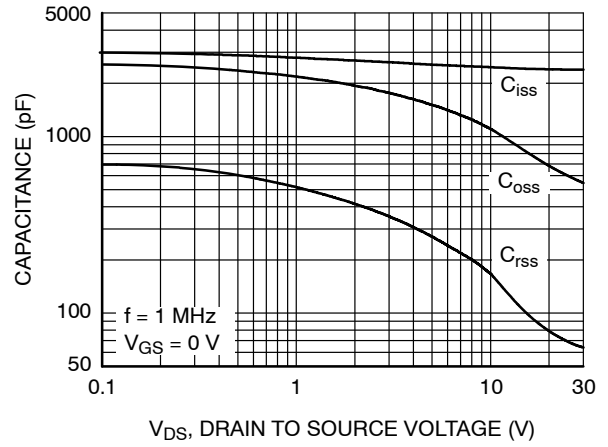


Figure 8. Capacitance vs. Drain to Source Voltage

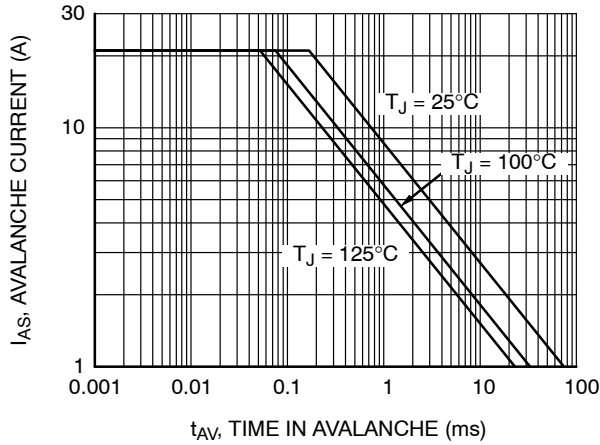


Figure 9. Unclamped Inductive Switching Capability

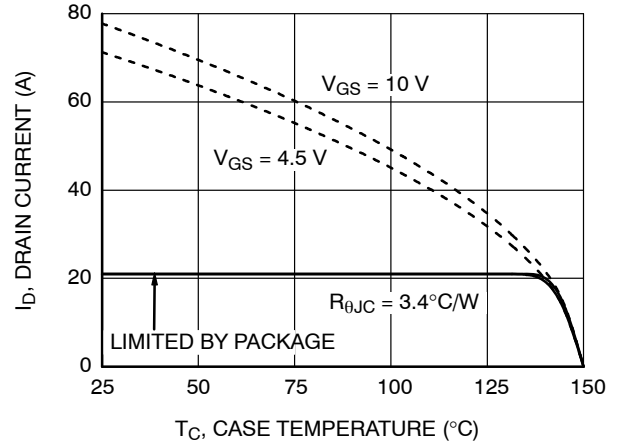


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

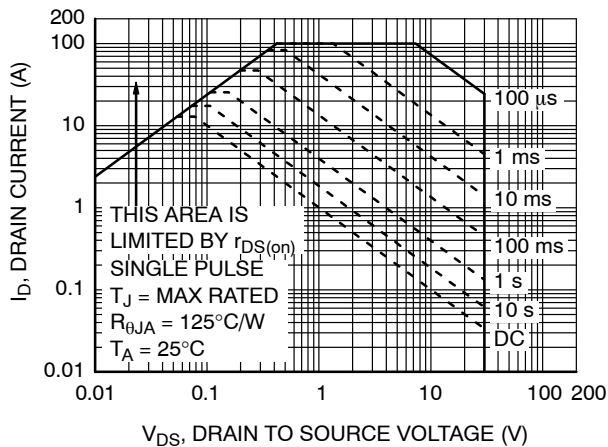


Figure 11. Forward Bias Safe Operating Area

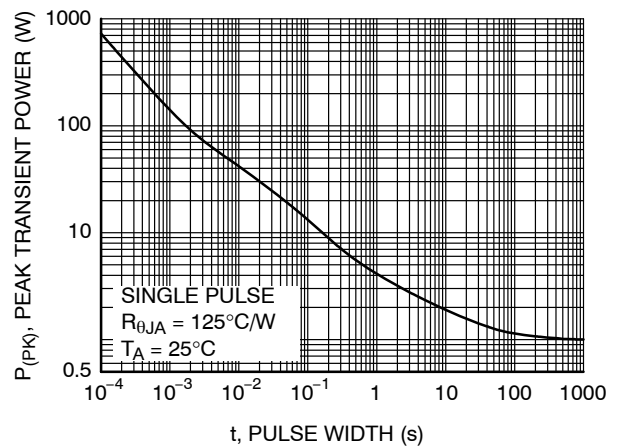


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

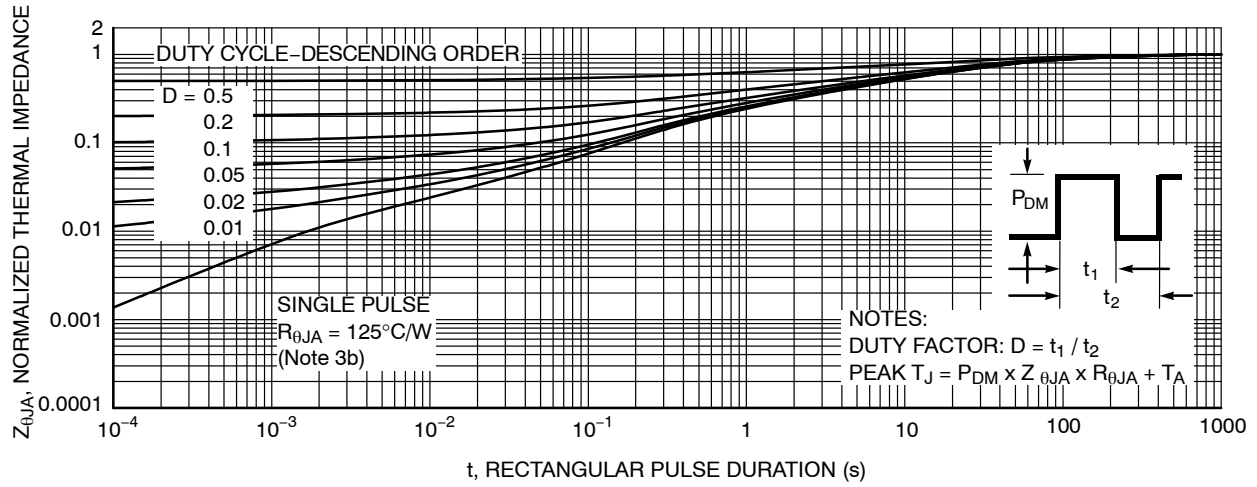


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

FDMC0310AS, FDMC0310AS-F127

TYPICAL CHARACTERISTICS (continued)

SyncFET Schottky Body Diode Characteristics

onsemi SyncFET process embeds a Schottky diode in parallel with POWERTRENCH MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMC0310AS.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

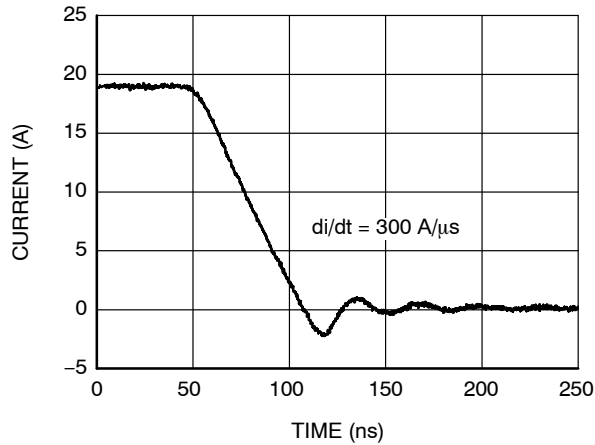


Figure 14. SyncFET Body Diode Reverse Recovery Characteristics

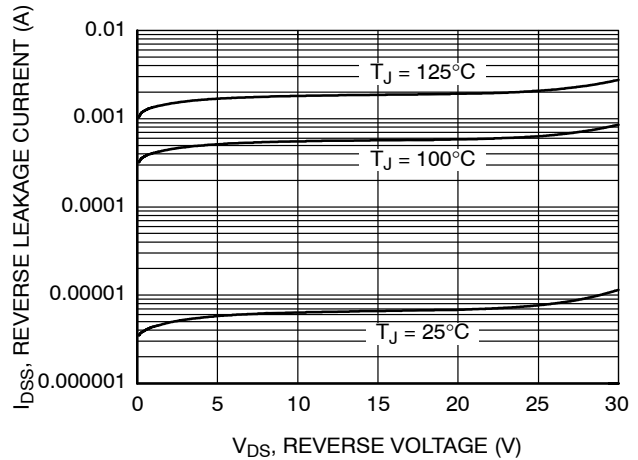


Figure 15. SyncFET Body Diode Reverse Leakage vs. Drain-Source Voltage

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping [†]
FDMC0310AS	FDMC0310AS	WDFN8 3.3x3.3, 0.65P MLP (SAWN) (Pb-Free)	13"	12 mm	3000 / Tape & Reel
FDMC0310AS-F127	FDMC0310AS	WDFN8 3.3x3.3, 0.65P MLP (PUNCH) (Pb-Free)	13"	12 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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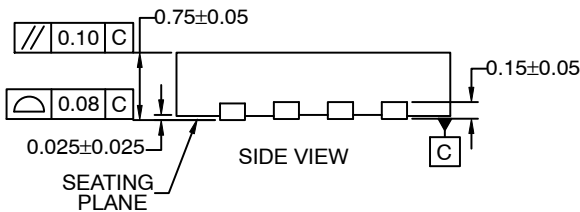
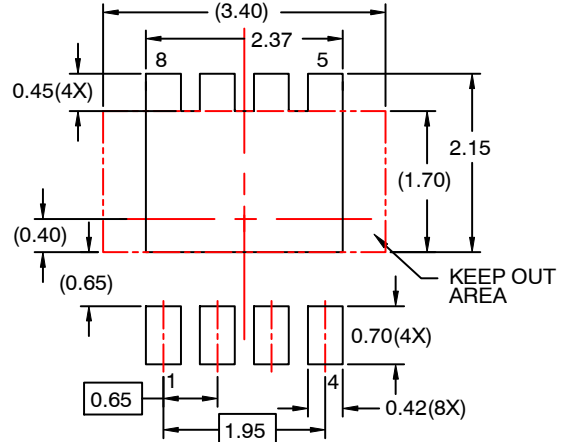
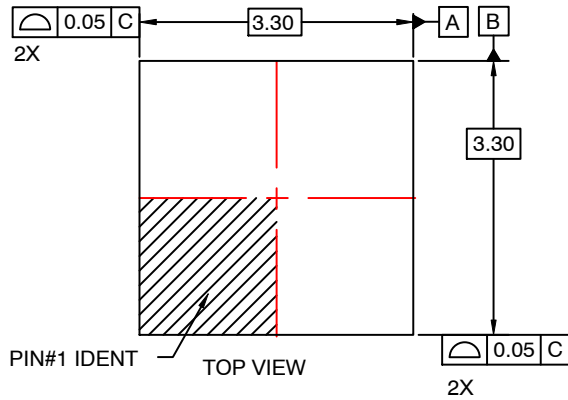
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



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CASE 511DH
ISSUE O

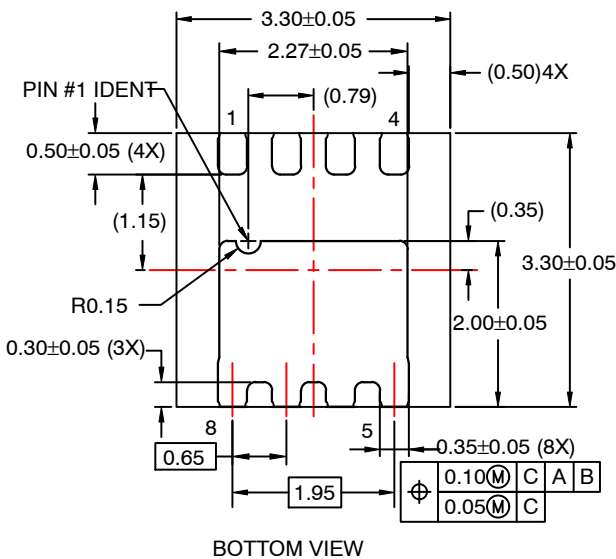
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RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

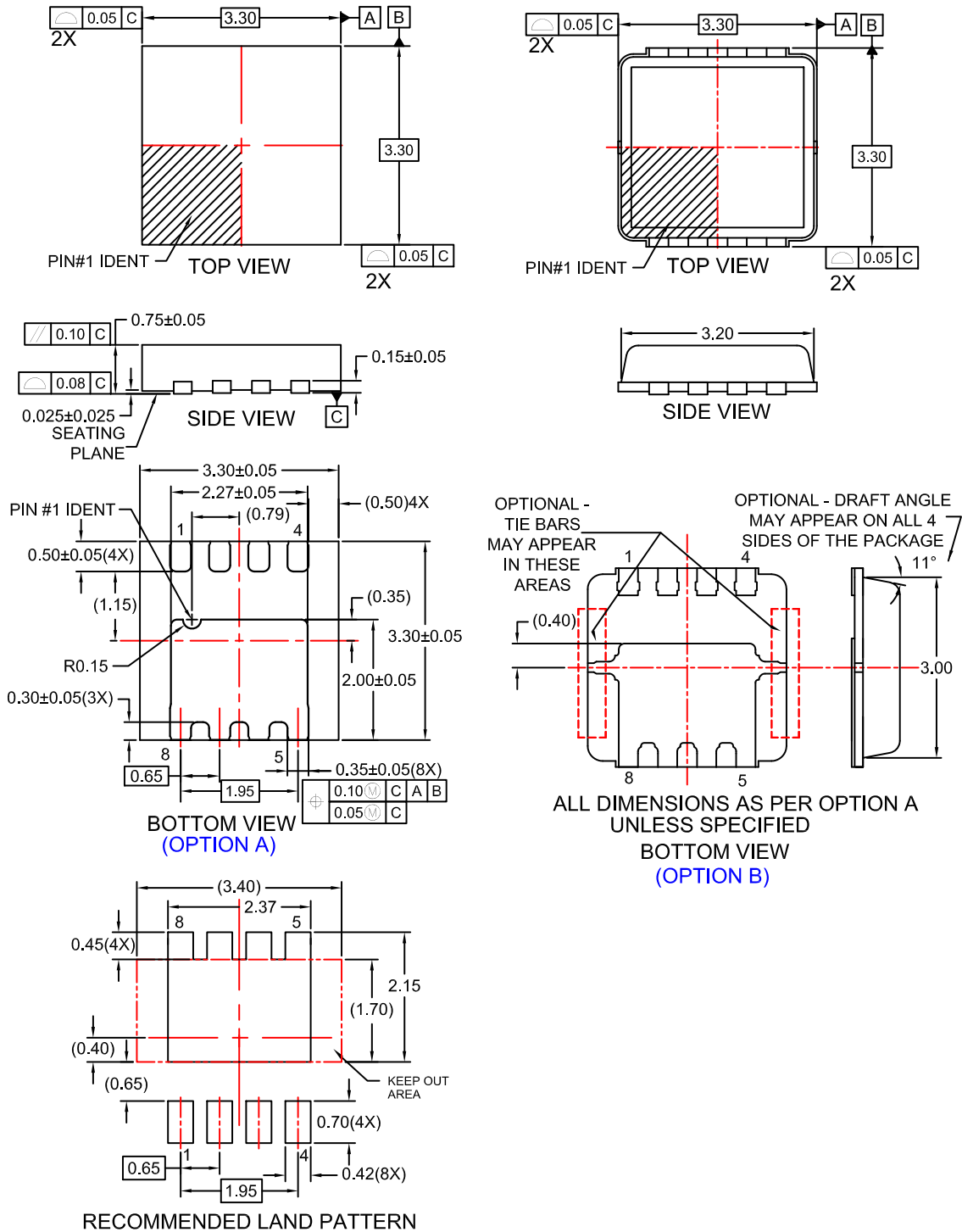


WDFN8 3.3x3.3, 0.65P

CASE 511DQ

ISSUE O

DATE 31 OCT 2016

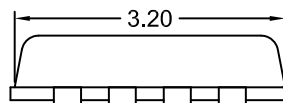
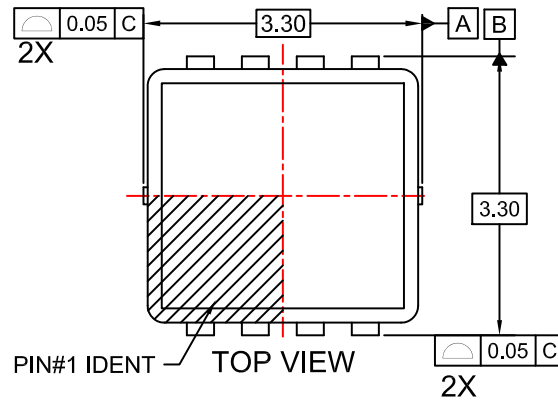


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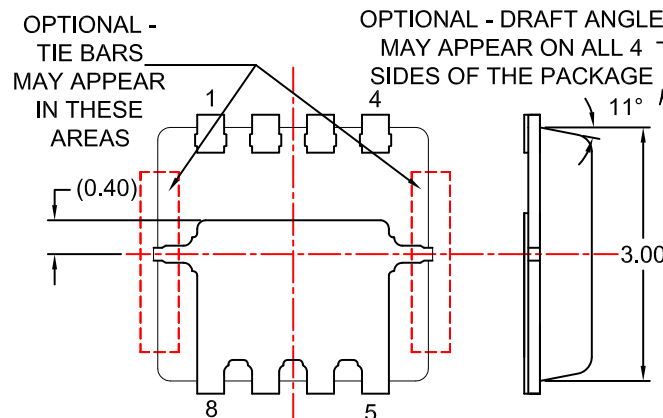
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CASE 511DQ
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SIDE VIEW



ALL DIMENSIONS AS PER OPTION A
UNLESS SPECIFIED

BOTTOM VIEW
(OPTION C)

NOTES:

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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
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