

MOSFET – P-Channel, POWERTRENCH®

-30 V, -20 A, 14.4 mΩ

FDMC6675BZ

Description

The FDMC6675BZ has been designed to minimize losses in load switch applications. Advancements in both silicon and package technologies have been combined to offer the lowest $R_{DS(on)}$ and ESD protection.

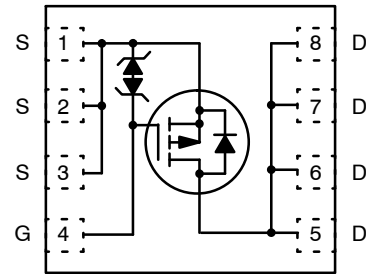
Features

- Max $R_{DS(on)}$ = 14.4 mΩ at $V_{GS} = -10$ V, $I_D = -9.5$ A
- Max $R_{DS(on)}$ = 27.0 mΩ at $V_{GS} = -4.5$ V, $I_D = -6.9$ A
- HBM ESD Protection Level of 8 kV Typical (Note 3)
- Extended V_{GSS} Range (-25 V) for Battery Applications
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

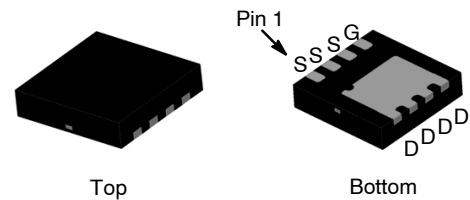
Typical Applications

- Load Switch in Notebook and Server
- Notebook Battery Pack Power Management

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
-30 V	14.4 mΩ @ -10 V	-20 A

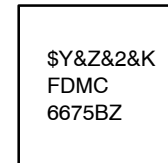


P-Channel



WDFN8 3.3x3.3, 0.65P
CASE 511DR

MARKING DIAGRAM



- \$Y = onsemi Logo
- &Z = Assembly Plant Code
- &2 = Numeric Date Code
- &K = Lot Code
- FDMC6675BZ = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMC6675BZ

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, Unless otherwise specified)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	-30	V
V_{GS}	Gate to Source Voltage	± 25	V
I_D	Drain Current –Continuous (Package Limited) $T_C = 25^\circ\text{C}$	-20	A
	–Continuous (Silicon Limited) $T_C = 25^\circ\text{C}$	-40	
	–Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	-9.5	
	–Pulsed	-32	
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	36	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.4	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Shipping (Qty / Packing) [†]
FDMC6675BZ	FDMC6675BZ	WDFN8 3.3x3.3, 0.65P (MLP) (Pb-Free/Halogen Free)	13"	12 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu\text{A}, V_{GS} = 0 \text{V}$	-30	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, referenced to 25°C	-	-20	-	$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24 \text{V}, V_{GS} = 0 \text{V}$ $V_{DS} = -24 \text{V}, V_{GS} = 0 \text{V}, T_J = 125^\circ\text{C}$	-	-	-1 -100	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25 \text{V}, V_{DS} = 0 \text{V}$	-	-	± 10	μA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu\text{A}$	-1.0	-1.9	-3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, referenced to 25°C	-	6.0	-	$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10 \text{V}, I_D = -9.5 \text{A}$	-	10.7	14.4	$\text{m}\Omega$
		$V_{GS} = -4.5 \text{V}, I_D = -6.9 \text{A}$	-	17.4	27.0	
		$V_{GS} = -10 \text{V}, I_D = -9.5 \text{A}, T_J = 125^\circ\text{C}$	-	15.2	20.5	
g_{FS}	Forward Transconductance	$V_{DD} = -5 \text{V}, I_D = -9.5 \text{A}$	-	28	-	S

FDMC6675BZ

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	2154	2865	pF
C_{oss}	Output Capacitance		-	392	525	pF
C_{rss}	Reverse Transfer Capacitance		-	349	525	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{ V}, I_D = -9.5\text{ A}, V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$	-	11	20	ns
t_r	Rise Time		-	10	20	
$t_{d(off)}$	Turn-off Delay Time		-	44	71	
t_f	Fall Time		-	26	42	
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to } -10\text{ V}, V_{DD} = -15\text{ V}, I_D = -9.5\text{ A}$	-	46	65	nC
	Total Gate Charge	$V_{GS} = 0\text{ V to } -5\text{ V}, V_{DD} = -15\text{ V}, I_D = -9.5\text{ A}$	-	26	37	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = -15\text{ V}, I_D = -9.5\text{ A}$	-	6.4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	$V_{DD} = -15\text{ V}, I_D = -9.5\text{ A}$	-	13	-	nC

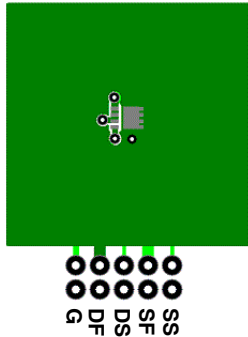
DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -9.5\text{ A}$ (Note 2)	-	-0.89	-1.3	V
		$V_{GS} = 0\text{ V}, I_S = -1.6\text{ A}$ (Note 2)	-	-0.73	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -9.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	24	38	ns
Q_{rr}	Reverse Recovery Charge		-	15	27	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ determined by the user's board design.



- a) 53°C/W when mounted on a 1 in² pad of 2 oz copper



- b) 125°C/W when mounted on a minimum pad

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS
($T_J = 25\text{ }^\circ\text{C}$ UNLESS OTHERWISE NOTED)

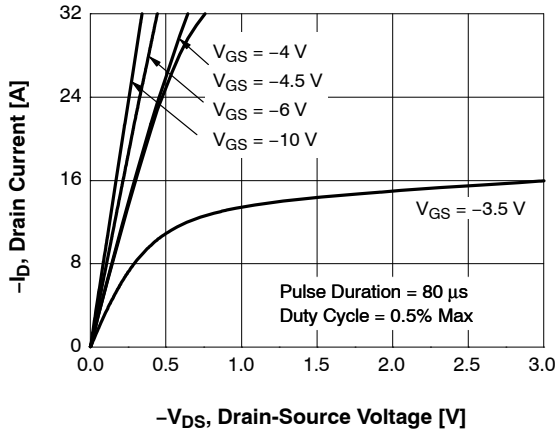


Figure 1. On-Region Characteristics

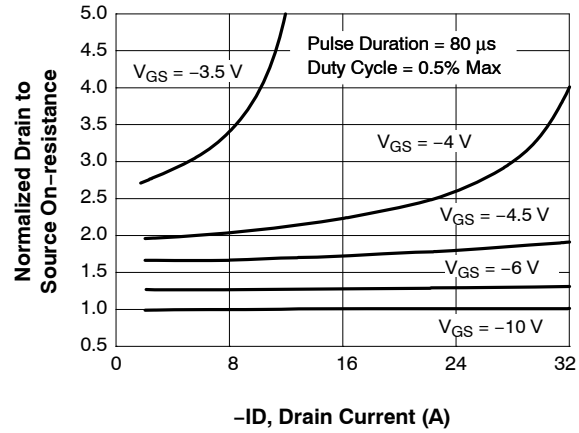


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

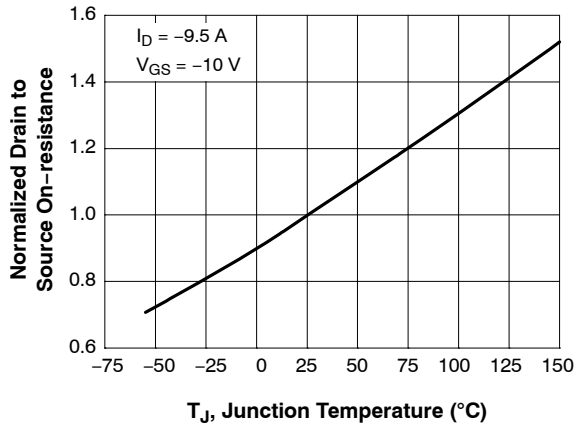


Figure 3. Normalized On Resistance vs Junction Temperature

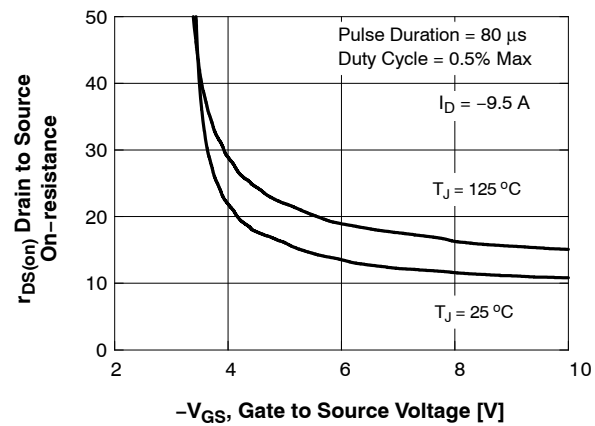


Figure 4. On-Resistance vs Gate to Source Voltage

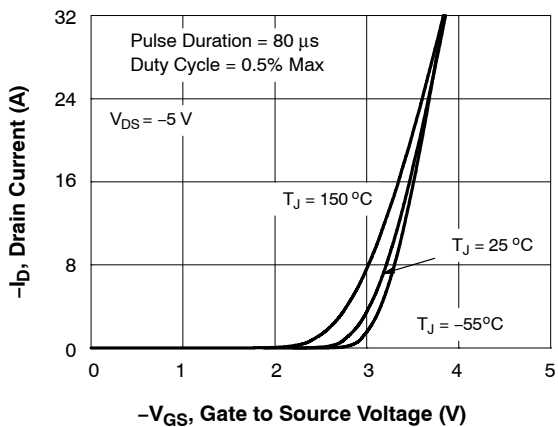


Figure 5. Transfer Characteristics

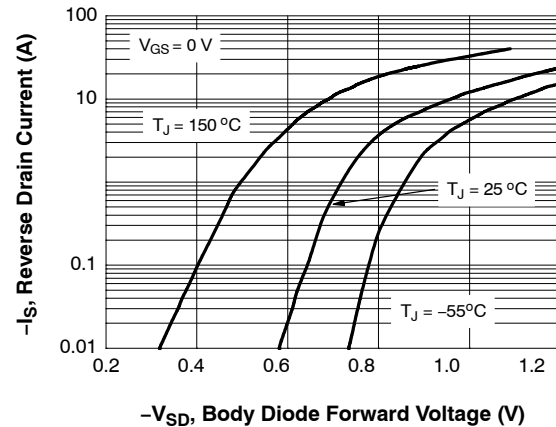


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

FDMC6675BZ

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

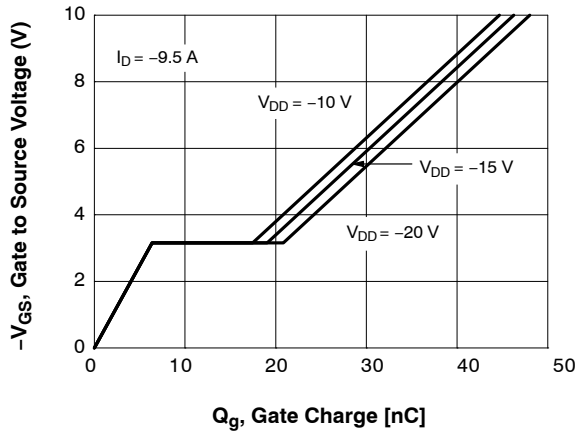


Figure 7. Gate Charge Characteristics

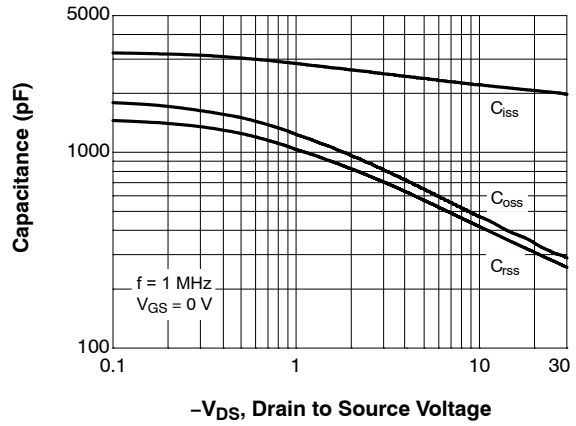


Figure 8. Capacitance vs Drain to Source Voltage

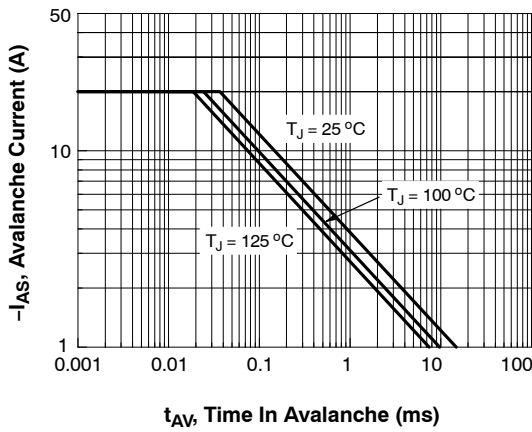


Figure 9. Unclamped Inductive Switching Capability

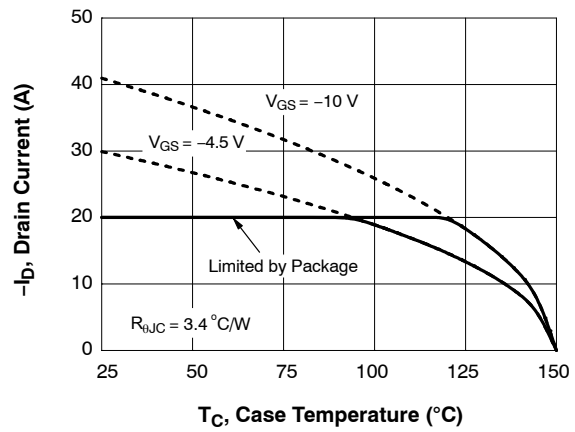


Figure 10. Maximum Continuous Drain Current vs Case Temperature

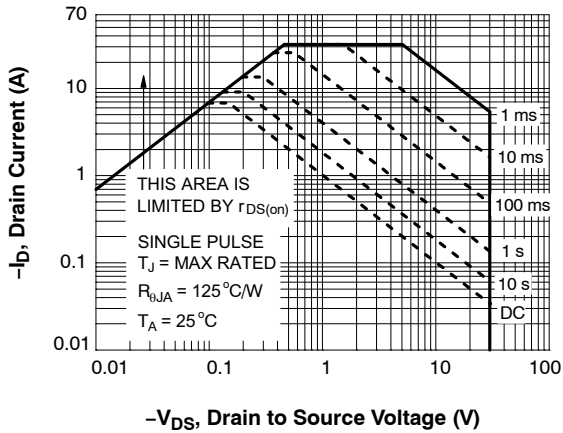


Figure 11. Forward Bias Safe Operating Area

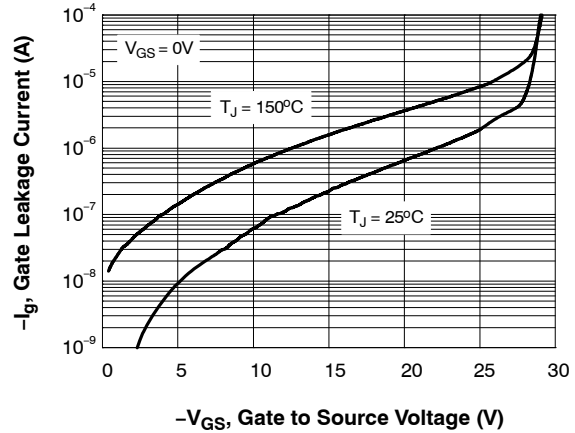


Figure 12. I_{gss} vs V_{gss}

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

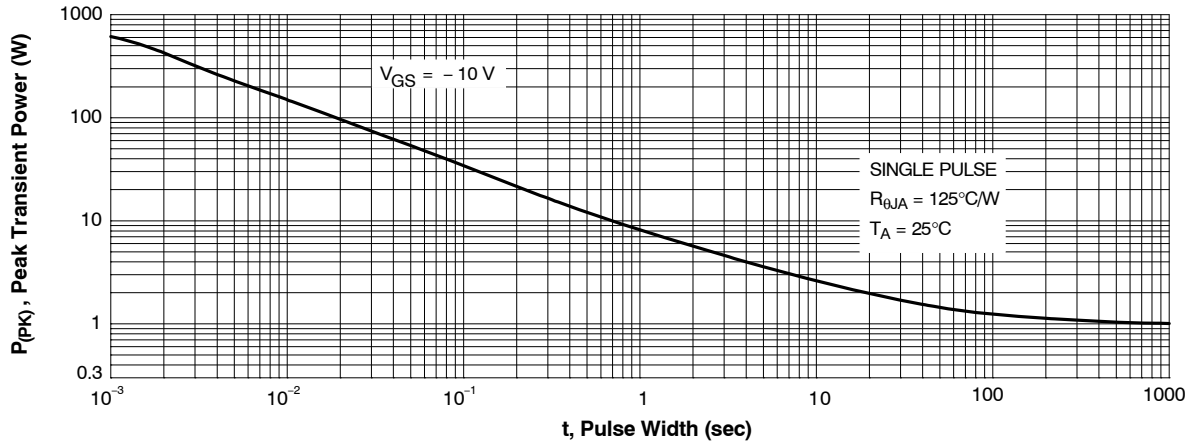


Figure 13. Single Pulse Maximum Power Dissipation

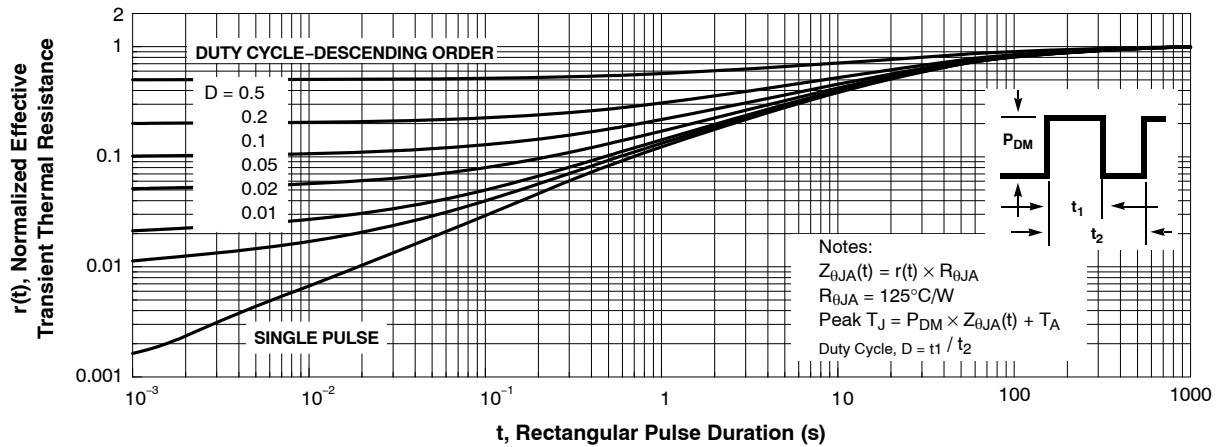
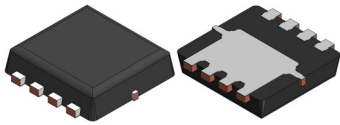


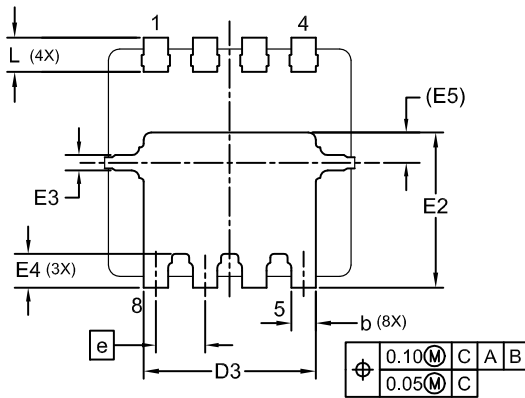
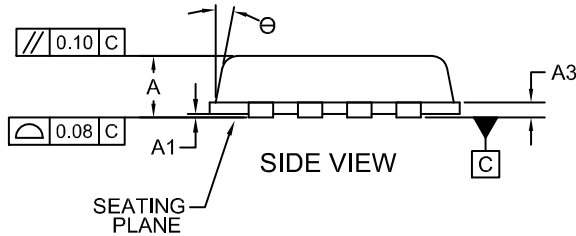
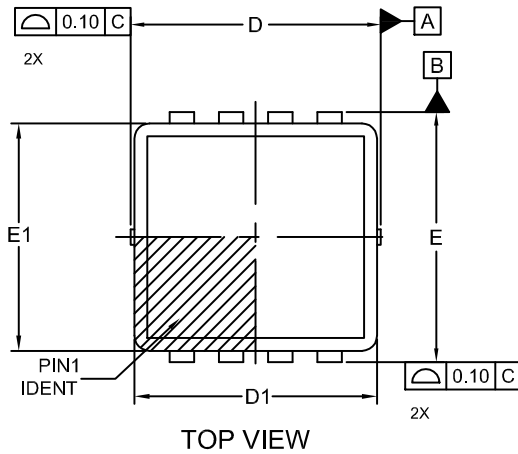
Figure 14. Junction-to-Ambient Transient Thermal Response Curve

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



WDFN8 3.3x3.3, 0.65P
CASE 511DR
ISSUE B

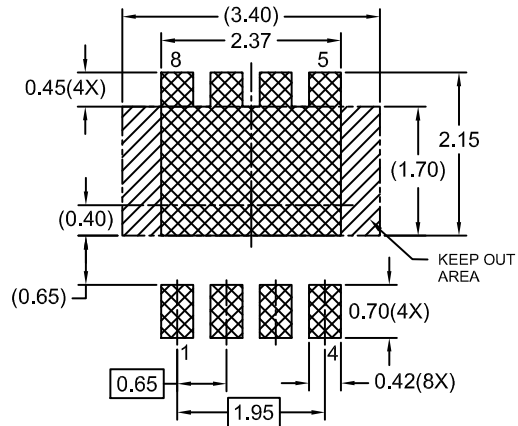
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NOTES:

- A. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- B. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
- C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS. MOLD FLASH PROTRUSION OR GATE BURR DOES NOT EXCEED 0.150MM.

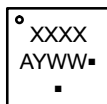
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.15	0.20	0.25
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D1	3.10	3.20	3.30
D3	2.17	2.27	2.37
E	3.20	3.30	3.40
E1	2.90	3.00	3.10
E2	1.95	2.05	2.15
E3	0.15	0.20	0.25
E4	0.30	0.40	0.50
E5	0.40 REF		
e	0.65 BSC		
L	0.30	0.40	0.50
θ	0°	-	12°



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

(Note: Microdot may be in either location)

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