

# MOSFET - P-Channel, POWERTRENCH®

-20 V, -56 A, 6.5 m $\Omega$ 

### FDMC6688P

#### **General Description**

This P-Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been optimized for  $R_{DS(on)}$ , switching performance and ruggedness.

#### **Features**

- Max  $R_{DS(on)} = 6.5 \text{ m}\Omega$  at  $V_{GS} = -4.5 \text{ V}$ ,  $I_D = -14 \text{ A}$
- Max  $R_{DS(on)} = 9.8 \text{ m}\Omega$  at  $V_{GS} = -2.5 \text{ V}$ ,  $I_D = -11 \text{ A}$
- Max  $R_{DS(on)} = 20 \text{ m}\Omega$  at  $V_{GS} = -1.8 \text{ V}$ ,  $I_D = -9 \text{ A}$
- High Performance Trench Technology for Extremely Low R<sub>DS(on)</sub>
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- This Device is Pb-Free, Halide Free and is RoHS Compliant

#### **Applications**

- · Load Switch
- Battery Management
- Power Management
- Reverse Polarity Protection

#### MOSFET MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)

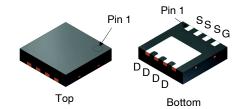
Symbol	Parameter	Ratings	Unit
V <sub>DS</sub>	Drain to Source Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	±8	V
I <sub>D</sub>	Drain Current -Continuous, T <sub>C</sub> = 25°C -Continuous, T <sub>A</sub> = 25°C (Note 1a) -Pulsed (Note 3)	-56 -14 -226	Α
P <sub>D</sub>	Power Dissipation $T_C = 25^{\circ}C$ $T_A = 25^{\circ}C$ (Note 1a)	30 2.3	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

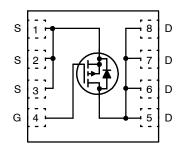
Symbol	Parameter	Value	Unit
$R_{ heta JC}$	Thermal Resistance, Junction to Case	3.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	°C/W

V <sub>DS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX
-20 V	6.5 mΩ @ -4.5 V	-56 A
	9.8 mΩ @ –2.5 V	
	20 mΩ @ -1.8 V	



PQFN8 3.3X3.3, 0.65P (Power 33) CASE 483AX

#### **PIN ASSIGNMENT**



#### MARKING DIAGRAM

ZYWWKK FDMC 6688P

Z = Assembly Plant Code
YWW = Date Code (Year & Week)
KK = Lot Traceability Code
FDMC6688P = Specific Device Code

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
FDMC6688P	PQFN8 (Power 33) (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

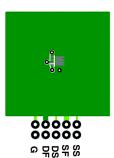
#### **ELECTRICAL CHARACTERISTICS** (T<sub>.I</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
OFF CHARACT	TERISTICS					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-20	-	-	V
$\Delta BV_{DSS} / \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA, referenced to 25°C	_	-16	-	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	-1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA
ON CHARACTI	ERISTICS					
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu A$	-0.4	-0.75	-1	V
$\Delta V_{GS(th)} / \Delta T_{J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = -250 μA, referenced to 25°C	_	3	-	mV/°C
R <sub>DS(on)</sub>	Static Drain to Source On-Resistance	$V_{GS} = -4.5 \text{ V}, I_D = -14 \text{ A}$	-	5.3	6.5	mΩ
		$V_{GS} = -2.5 \text{ V}, I_D = -11 \text{ A}$	-	7	9.8	
		$V_{GS} = -1.8 \text{ V}, I_D = -9 \text{ A}$	-	10.7	20	
		$V_{GS} = -4.5 \text{ V}, I_D = -14 \text{ A},$ $T_J = 125^{\circ}\text{C}$	-	7.3	11	
9FS	Forward Transconductance	$V_{DS} = -5 \text{ V}, I_D = -14 \text{ A}$	-	80	-	S
DYNAMIC CHA	RACTERISTICS					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$	-	4956	7435	pF
C <sub>oss</sub>	Output Capacitance	f = 1 MHz	-	678	1020	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	7	-	618	930	pF
Rg	Gate Resistance		-	4.5	-	Ω
SWITCHING CI	HARACTERISTICS					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD}$ = -10 V, $I_{D}$ = -14 A, $V_{GS}$ = -4.5 V, $R_{GEN}$ = 6 Ω	-	19	35	ns
t <sub>r</sub>	Rise Time	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$	-	33	53	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	119	190	ns
t <sub>f</sub>	Fall Time		-	68	109	ns
Qg	Total Gate Charge	V <sub>DD</sub> = -10 V, I <sub>D</sub> = -14 A, V <sub>GS</sub> = -4.5 V	-	44	61	nC
Q <sub>gs</sub>	Gate to Source Charge	$V_{GS} = -4.5 \text{ V}$	-	7.4	-	nC
$Q_gd$	Gate to Drain "Miller" Charge		-	11	-	nC
DRAIN-SOUR	CE DIODE CHARACTERISTICS					
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -14 \text{ A (Note 2)}$	-	-0.8	-1.2	V
		$V_{GS} = 0 \text{ V}, I_{S} = -2 \text{ A (Note 2)}$	-	-0.6	-1.2	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = -14 A, di/dt = 100 A/μs	-	26	41	ns
Q <sub>rr</sub>	Reverse Recovery Charge	7	-	10	20	nC

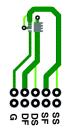
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



 a. 53°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300  $\mu s,$  Duty cycle < 2.0 %.
- 3. Pulse Id refers to Forward Bias Safe Operation Area.

#### **TYPICAL CHARACTERISTICS**

(T<sub>J</sub> = 25°C Unless Otherwise Noted)

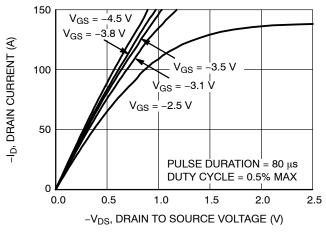


Figure 1. On-Region Characteristics

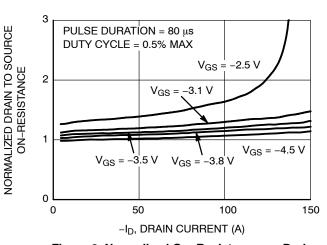


Figure 2. Normalized On–Resistance vs. Drain Current and Gate Voltage

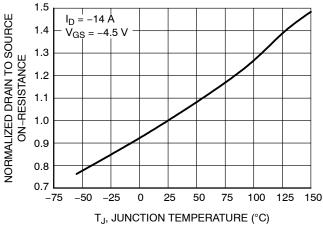


Figure 3. Normalized On-Resistance vs.

Junction Temperature

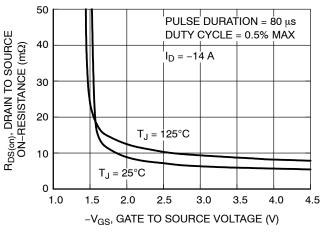


Figure 4. On-Resistance vs. Gate to Source Voltage

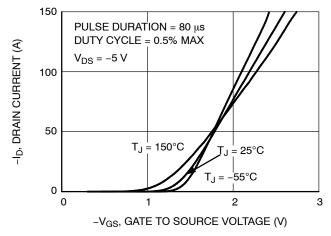


Figure 5. Transfer Characteristics

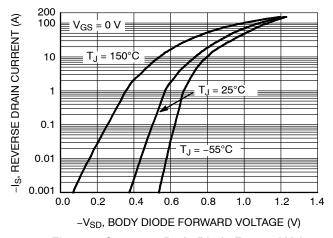


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

#### TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

(T<sub>J</sub> = 25°C Unless Otherwise Noted)

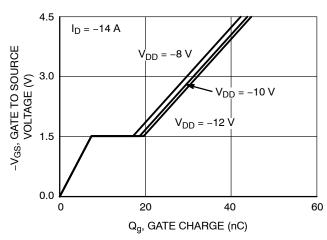


Figure 7. Gate Charge Characteristics

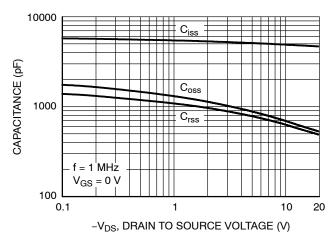


Figure 8. Capacitance vs. Drain to Source Voltage

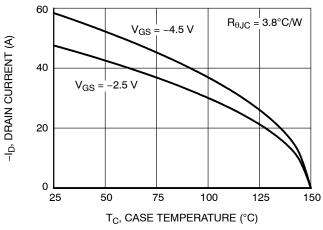


Figure 9. Maximum Continuous Drain Current vs. Case Temperature

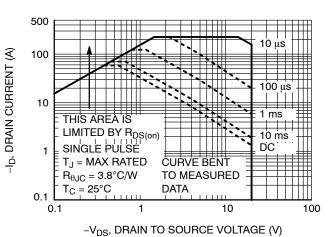


Figure 10. Forward Bias Safe Operating Area

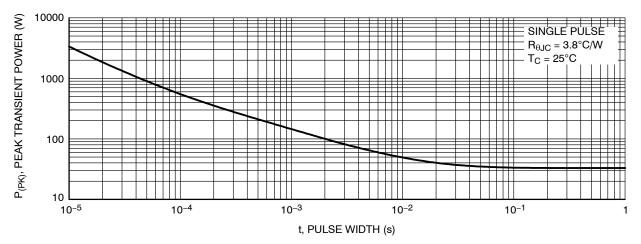


Figure 11. Single Pulse Maximum Power Dissipation

#### TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

(T<sub>J</sub> = 25°C Unless Otherwise Noted)

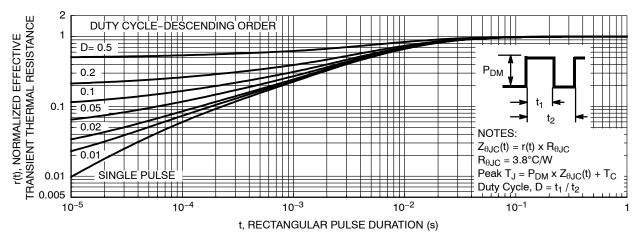


Figure 12. Junction-to-Case Transient Thermal Response Curve

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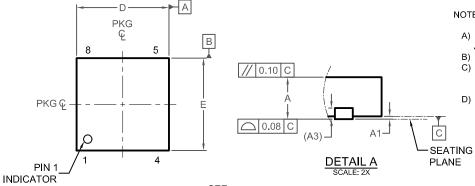
## **PQFN8 3.3X3.3, 0.65P**CASE 483AX ISSUE B

**DATE 24 JUN 2022** 

NOTES: UNLESS OTHERWISE SPECIFIED

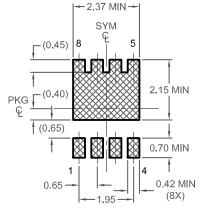
- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
Α	0.70	0.75	0.80
A1	0.00	ı	0.05
A3	(	).20 REF	
b	0.27	0.32	0.37
D	3,20	3,30	3.40
D2	2.17	2.27	2.37
E	3.20	3.30	3.40
E2	1.84	1.94	2.04
е	0.65 BSC		
e1	1.95 BSC		
L	0.40	0.50	0.60
L4	0.34 REF		
z	0.52 REF		



DETAIL A

<b>♦</b> 0.10 C A B	e1
b (8X) — 1	e 4
ΓΨ̈́	ΨΨΨ <u></u>
PKG Ç	
<u> </u>	
(L4)   8	_
_	—D2—



## LAND PATTERN RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRW/D.

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