

MOSFET – N-Channel, DUAL COOL[®] 33, POWERTRENCH[®]

30 V, 40 A, 2.2 mΩ

FDMC7660DC

General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process. Advancements in both silicon and DUAL COOL package technologies have been combined to offer the lowest $R_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

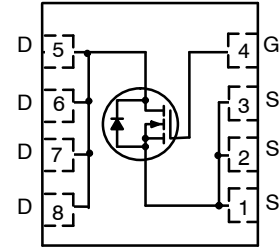
Features

- DUAL COOL Top Side Cooling PQFN Package
- Max $R_{DS(on)}$ = 2.2 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 22\text{ A}$
- Max $R_{DS(on)}$ = 3.3 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 18\text{ A}$
- High Performance Technology for Extremely Low $R_{DS(on)}$
- SyncFET™ Schottky Body Diode
- Pb-Free, Halide Free and RoHS Compliant

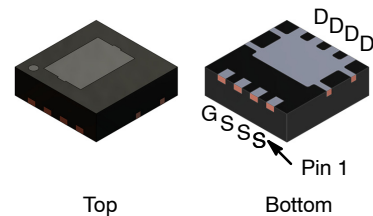
Applications

- Synchronous Rectifier for DC/DC Converters
- Telecom Secondary Side Rectification
- High End Server/Workstation

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
30 V	2.2 mΩ @ 10 V	40 A
	3.3 mΩ @ 4.5 V	



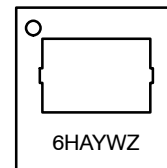
N-CHANNEL MOSFET



Top Bottom

PQFN8 3.3 × 3.3, 0.65P
(DUAL COOL 33)
CASE 483AL

MARKING DIAGRAM



- 6H = Specific Device Code
- A = Assembly Plant Code
- YW = Date Code (Year and Week)
- Z = Lot Code

ORDERING INFORMATION

Device	Package	Shipping†
FDMC7660DC	PQFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

FDMC7660DC

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit		
V_{DS}	Drain to Source Voltage	30	V		
V_{GS}	Gate to Source Voltage (Note 4)	± 20	V		
I_D	Drain Current	Continuous (Package limited)	$T_C = 25^\circ\text{C}$	A	
		Continuous (Silicon limited)	$T_C = 25^\circ\text{C}$		40
		Continuous (Note 1a)	$T_A = 25^\circ\text{C}$		150
		Pulsed			30
			200		
E_{AS}	Single Pulse Avalanche Energy (Note 3)	220	mJ		
dv/dt	Peak Diode Recovery dv/dt (Note 5)	1.0	V/ns		
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	78	W	
	Power Dissipation (Note 1a)	$T_A = 25^\circ\text{C}$	3.0		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Top Source)	4.3	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Bottom Drain)	1.6	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	42	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	105	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1i)	17	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1j)	26	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1k)	12	

FDMC7660DC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
--------	-----------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

B _V D _{SS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	30	–	–	V
ΔB _V D _{SS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	15	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	–	–	1	μA
I _{GSS}	Gate to Source Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V	–	–	100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1.2	2	2.5	V
ΔV _{GS(th)} / ΔT _J	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	–7	–	mV/°C
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 22 A	–	1.6	2.2	mΩ
		V _{GS} = 4.5 V, I _D = 18 A	–	2.5	3.3	
		V _{GS} = 10 V, I _D = 22 A, T _J = 125°C	–	2.2	3.3	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 22 A	–	147	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	–	3885	5170	pF
C _{oss}	Output Capacitance		–	1215	1620	pF
C _{rss}	Reverse Transfer Capacitance		–	100	150	pF
R _g	Gate Resistance		–	0.7	1.5	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 15 V, I _D = 22 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	17	31	ns
t _r	Rise Time		–	6.6	13	ns
t _{d(off)}	Turn-Off Delay Time		–	36	58	ns
t _f	Fall Time		–	5	10	ns
Q _g	Total Gate Charge	V _{GS} = 0 V to 10 V, V _{DD} = 15 V, I _D = 22 A	–	54	76	nC
		V _{GS} = 0 V to 4.5 V, V _{DD} = 15 V, I _D = 22 A	–	24	34	nC
Q _{gs}	Gate to Source Charge	V _{DD} = 15 V, I _D = 22 A	–	13	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	5.5	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source-Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 22 A (Note 2)	–	0.8	1.2	V
		V _{GS} = 0 V, I _S = 1.9 A (Note 2)	–	0.7	1.2	
t _{rr}	Reverse Recovery Time	I _F = 22 A, di/dt = 100 A/μs	–	43	69	ns
Q _{rr}	Reverse Recovery Charge		–	24	38	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

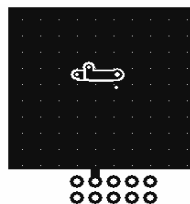
FDMC7660DC

THERMAL CHARACTERISTICS

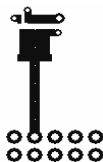
Symbol	Characteristic	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Top Source)	4.3	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Bottom Drain)	1.6	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	42	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	105	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1c)	29	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1d)	40	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1e)	19	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1f)	23	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1g)	30	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1h)	79	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1i)	17	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1j)	26	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1k)	12	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1l)	16	

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- a) 42°C/W when mounted on a 1 in² pad of 2 oz copper.



- b) 105°C/W when mounted on a minimum pad of 2 oz copper.

- Still air, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
 - Still air, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
 - Still air, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
 - Still air, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
 - 200FPM Airflow, No Heat Sink, 1 in² pad of 2 oz copper
 - 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
 - 200FPM Airflow, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
 - 200FPM Airflow, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
 - 200FPM Airflow, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
 - 200FPM Airflow, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
 - E_{AS} of 220 mJ is based on starting $T_J = 25^\circ\text{C}$, N-ch: $L = 1$ mH, $I_{AS} = 21$ A, $V_{DD} = 27$ V, $V_{GS} = 10$ V. 100% test at $L = 0.3$ mH, $I_{AS} = 33.5$ A.
 - As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
 - $I_{SD} \leq 22$ A, $di/dt \leq 100$ A/μs, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

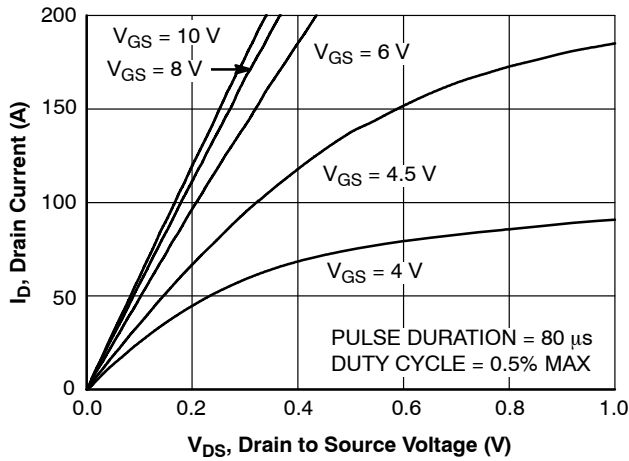


Figure 1. On-Region Characteristics

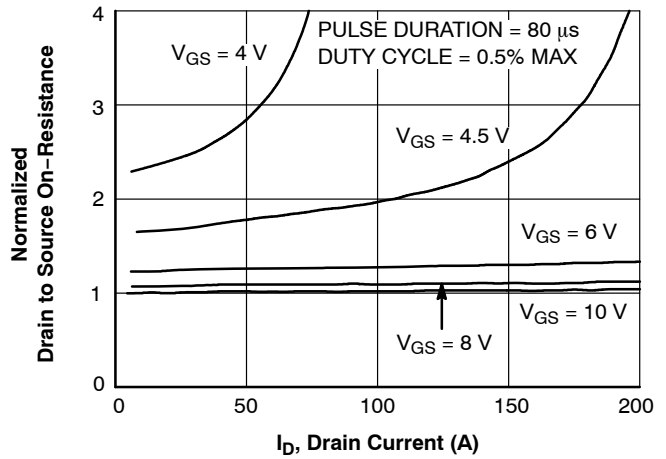


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

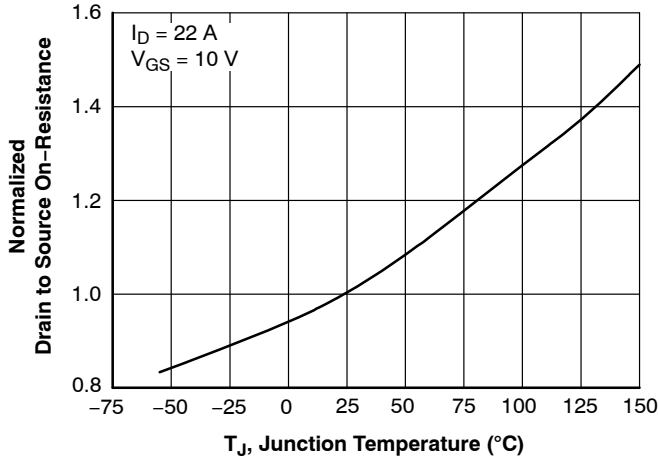


Figure 3. Normalized On-Resistance vs. Junction Temperature

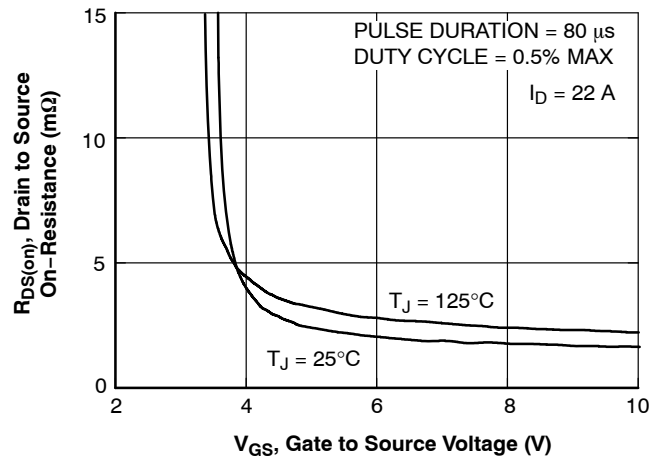


Figure 4. On-Resistance vs. Gate to Source Voltage

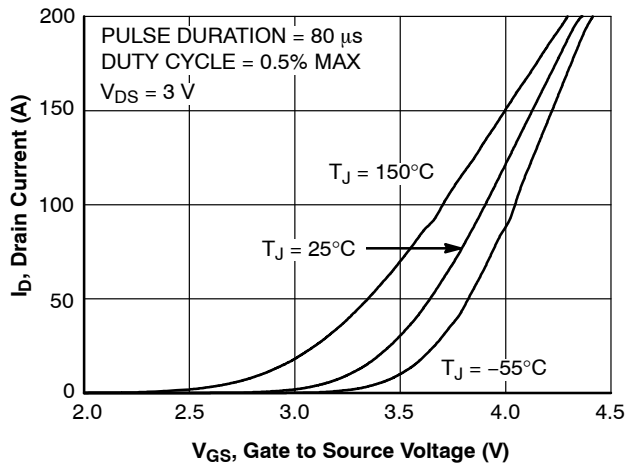


Figure 5. Transfer Characteristics

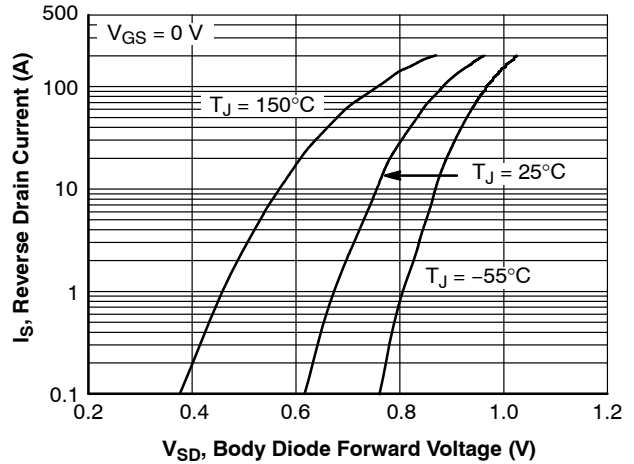


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

FDMC7660DC

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

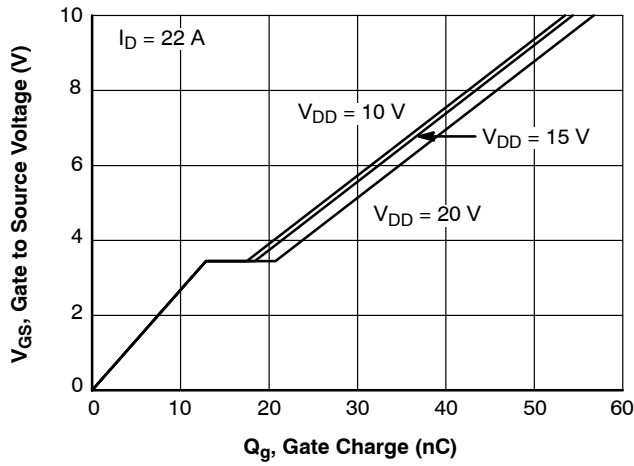


Figure 7. Gate Charge Characteristics

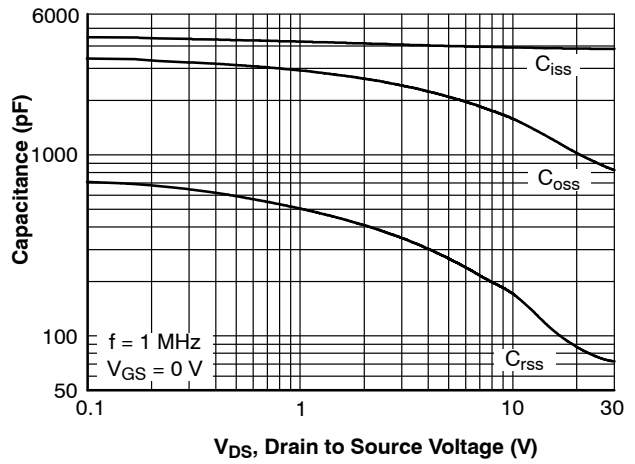


Figure 8. Capacitance vs. Drain to Source Voltage

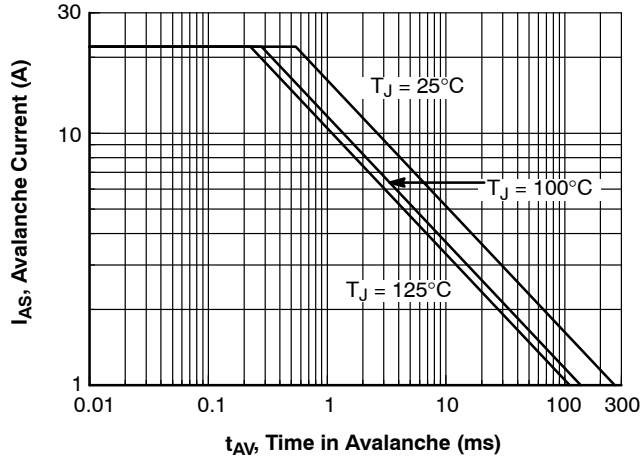


Figure 9. Unclamped Inductive Switching Capability

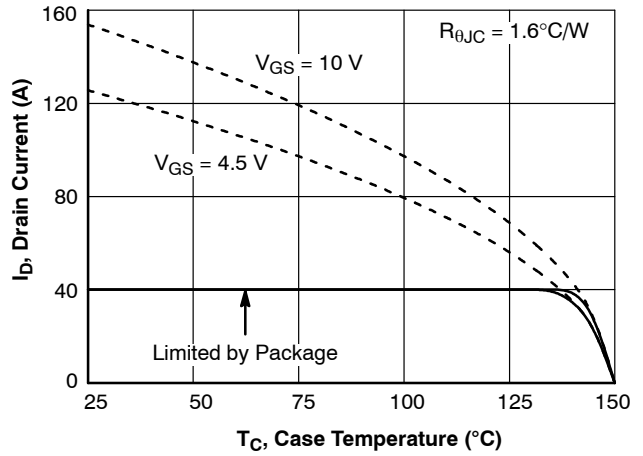


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

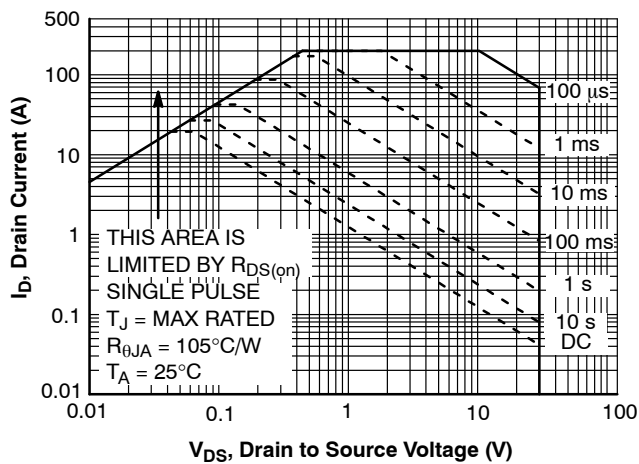


Figure 11. Forward Bias Safe Operating Area

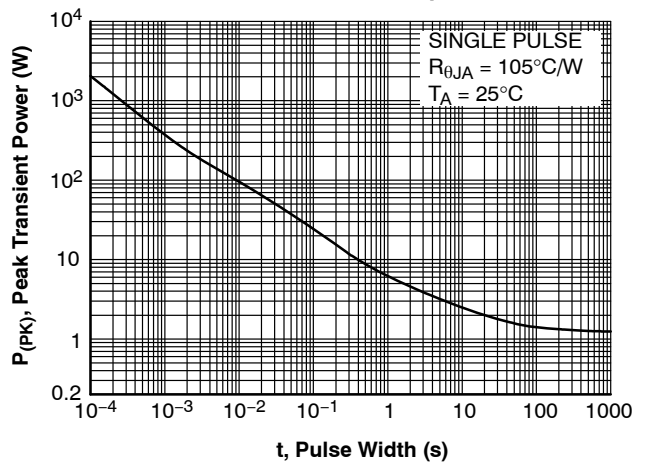


Figure 12. Single Pulse Maximum Power Dissipation

FDMC7660DC

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

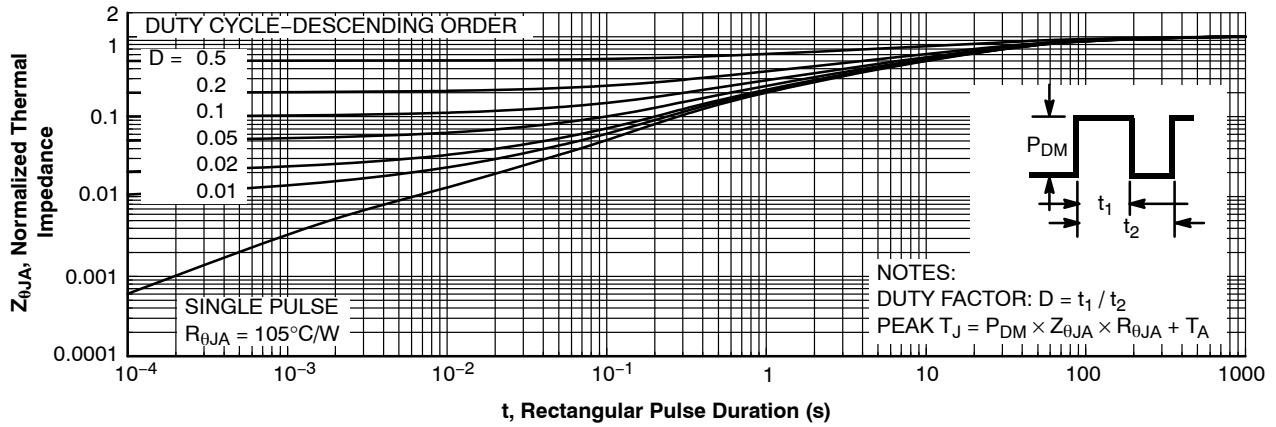
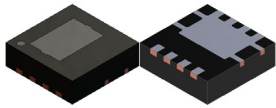


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

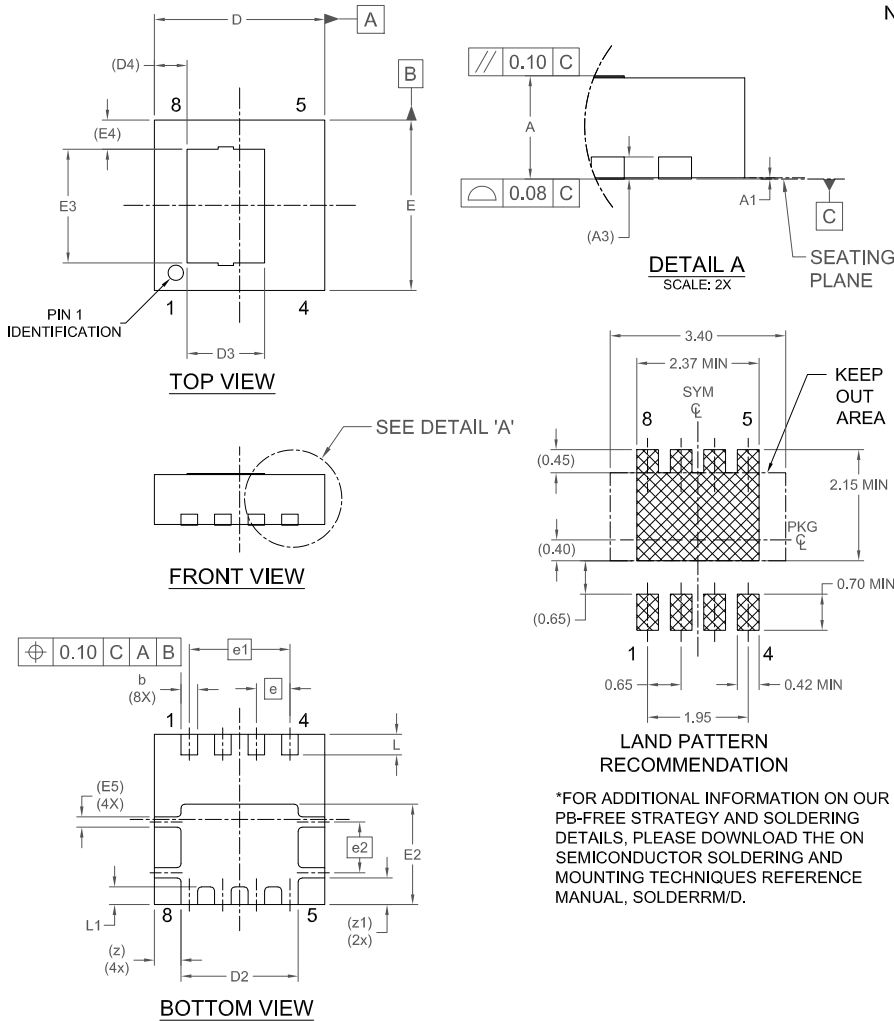
DUAL COOL and POWER TRENCH are registered trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

SyncFET is a trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.



**PQFN8 3.30x3.30x1.00, 0.65P
CASE 483AL
ISSUE B**

DATE 20 DEC 2023



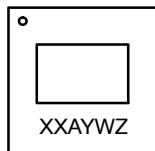
NOTES:

- A. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.27	0.32	0.37
A3	0.20 REF		
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
D3	1.40	1.55	1.70
D4	0.63 REF		
E	3.20	3.30	3.40
E2	1.90	2.00	2.10
E3	2.10	2.25	2.40
E4	0.56 REF		
E5	0.20 REF		
e	0.65 BSC		
e1	1.95 BSC		
e2	0.98 BSC		
L	0.30	0.40	0.50
L4	0.29	0.39	0.49
z	0.52 REF		
z1	0.52 REF		

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- Z = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "μ", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON13661G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PQFN8 3.30x3.30x1.00, 0.65P	PAGE 1 OF 1

onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

