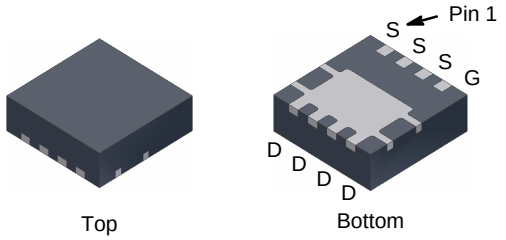
MOSFET – N-Channel, POWERTRENCH®, SyncFET™

30 V, 20 A, 2.2 mΩ

FDMC7660S

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
30 V	2.2 mΩ @ 10 V	20 A
	2.95 mΩ @4.5 V	



PQFN8 3.3X3.3, 0.65P
(Power 33)
CASE 483AK

General Description

The FDMC7660S has been designed to minimize losses in power conversion applications. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

Features

- Max $r_{DS(on)}$ = 2.2 mΩ at V_{GS} = 10 V, I_D = 20 A
- Max $r_{DS(on)}$ = 2.95 mΩ at V_{GS} = 4.5 V, I_D = 18 A
- High Performance Technology for Extremely Low $r_{DS(on)}$
- This Device is Pb−Free, Halide Free and is RoHS Compliant

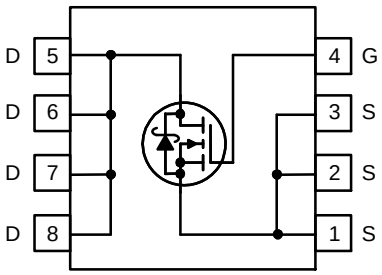
Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/GPU Low Side Switch
- Networking Point of Load Low Side Switch
- Telecom Secondary Side Rectification

MARKING DIAGRAM

&Z = Assembly Plant Code
&3 = 3−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
FDMC7660S = Device Code

PIN ASSIGNMENT



MOSFET MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 4)	±20	V
I_D	Drain Current − Continuous (Package Limited) T_C = 25°C − Continuous (Silicon Limited) T_C = 25°C − Continuous T_A = 25°C (Note 1a) − Pulsed	 40 100 20 200	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	128	mJ
P_D	Power Dissipation Power Dissipation (Note 1a)	41 2.3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

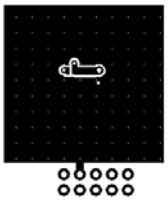
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, referenced to 25°C	–	13	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	–	–	500	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1 mA	1.2	1.6	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 1 mA, referenced to 25°C	–	−3	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 20 A	–	1.7	2.2	mΩ
		V_{GS} = 4.5 V, I_D = 18 A	–	2.5	2.95	
		V_{GS} = 10 V, I_D = 20 A,T_J = 125°C	–	2.2	3.1	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 20 A	–	129	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	–	3250	4325	pF
C_{oss}	Output Capacitance		–	1260	1680	pF
C_{rss}	Reverse Transfer Capacitance		–	105	160	pF
R_g	Gate Resistance		0.1	0.8	1.6	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 15 V, I_D = 20 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	14	25	ns
t_r	Rise Time		–	5	10	ns
$t_{d(off)}$	Turn−Off Delay Time		–	34	54	ns
t_f	Fall Time		–	3.9	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 15 V, I_D = 20 A	–	47	66	nC
		V_{GS} = 0 V to 4.5 V, V_{DD} = 15 V, I_D = 20 A	–	21	29	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 15 V, I_D = 20 A	–	9.5	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	5	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 20 A (Note 2)	–	0.8	1.2	V
		V_{GS} = 0 V, I_S = 1.9 A (Note 2)	–	0.4	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 20 A, di/dt = 300 A/μs	–	31	50	ns
Q_{rr}	Reverse Recovery Charge		–	39	62	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C, N−ch: L = 1 mH, I_{AS} = 16 A, V_{DD} = 27 V, V_{GS} = 10 V.
4. As an N−ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted)

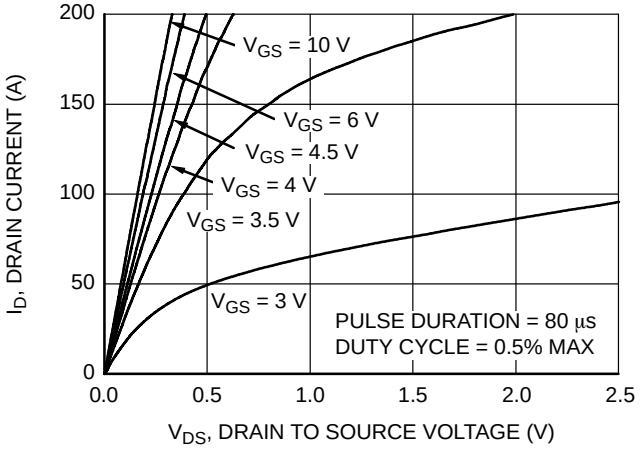


Figure 1. On Region Characteristics

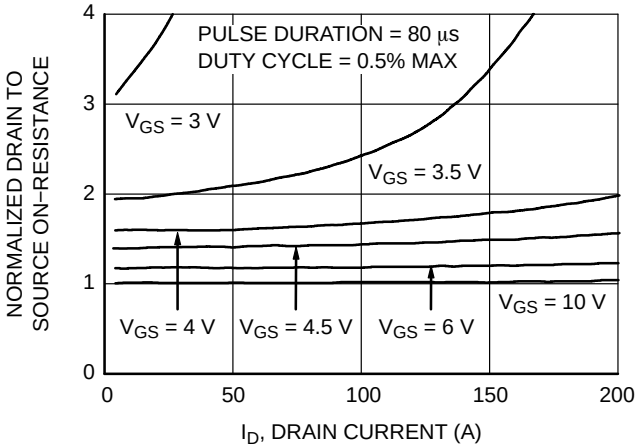


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

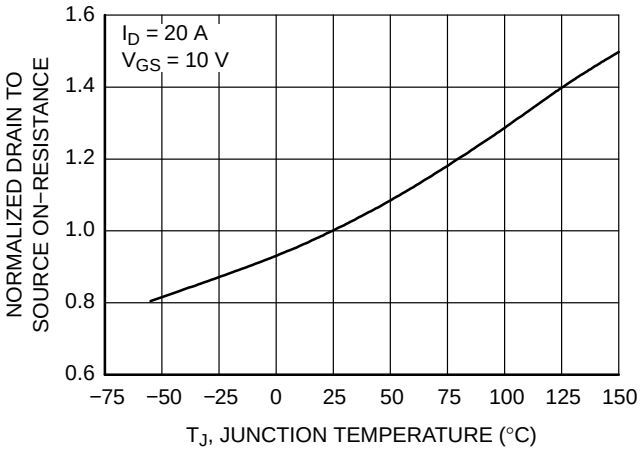


Figure 3. Normalized On Resistance vs. Junction Temperature

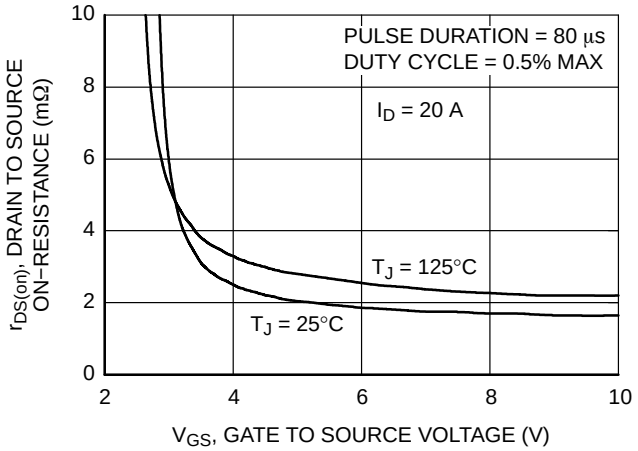


Figure 4. On−Resistance vs. Gate to Source Voltage

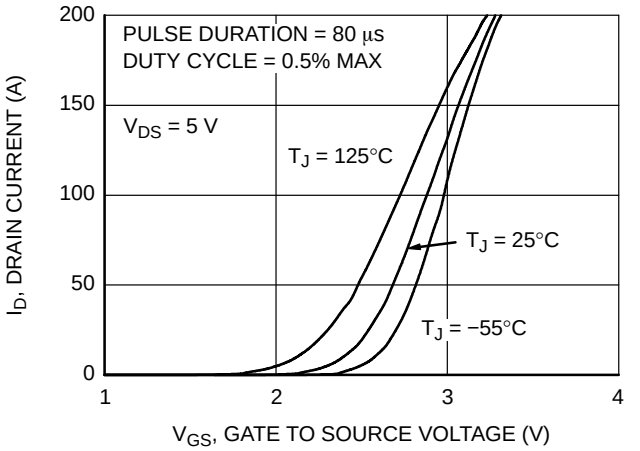


Figure 5. Transfer Characteristics

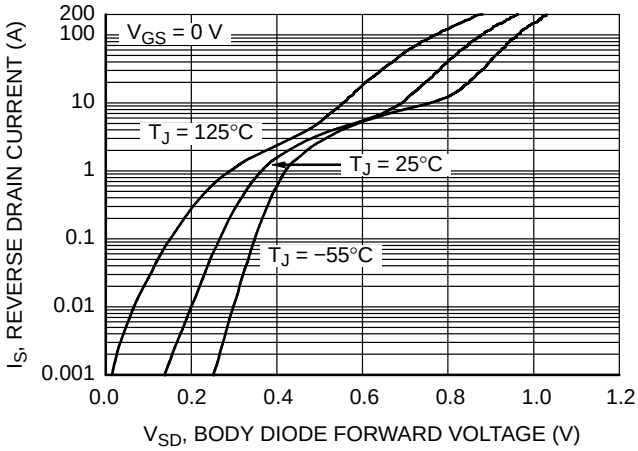


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted) (continued)

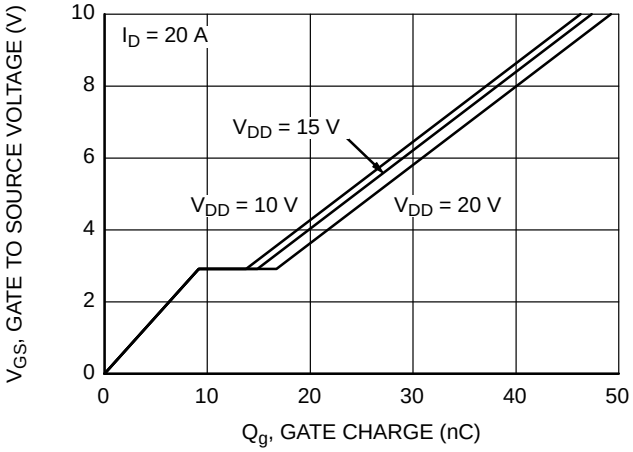


Figure 7. Gate Charge Characteristics

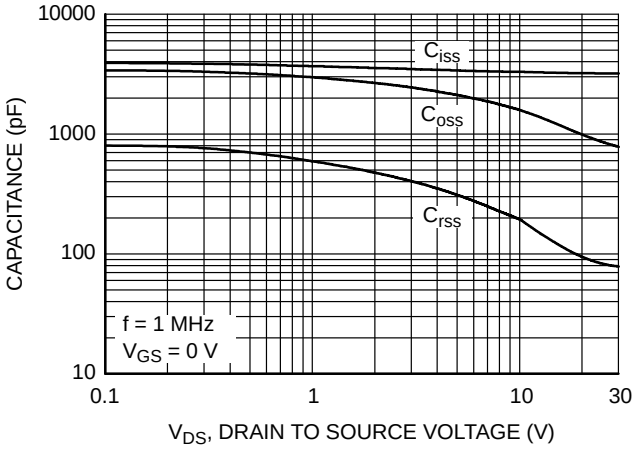


Figure 8. Capacitance vs. Drain to Source Voltage

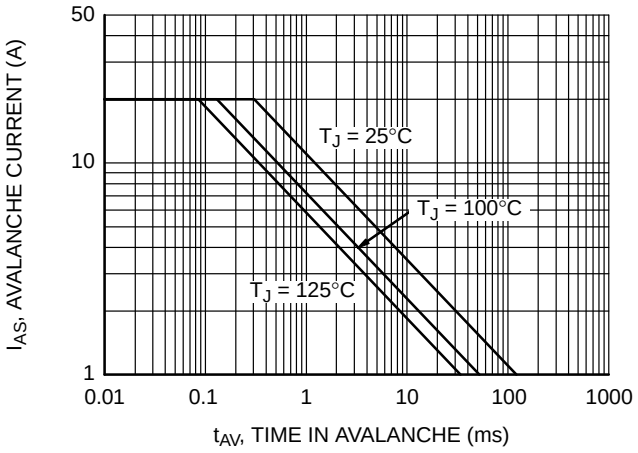


Figure 9. Unclamped Inductive Switching Capability

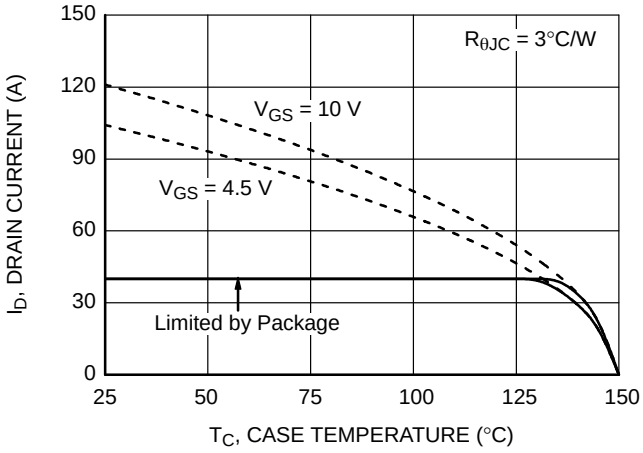


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

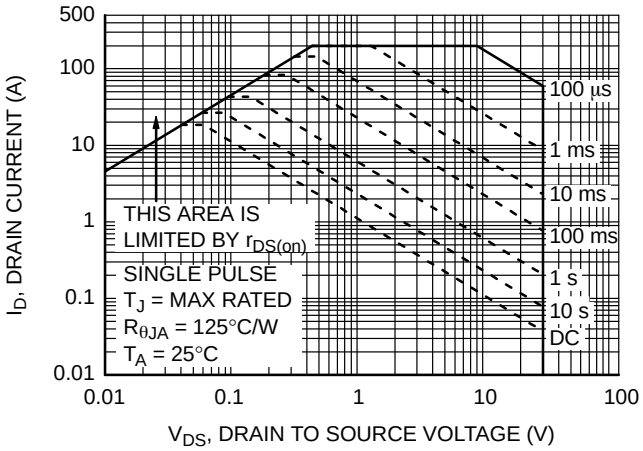


Figure 11. Forward Bias Safe Operating Area

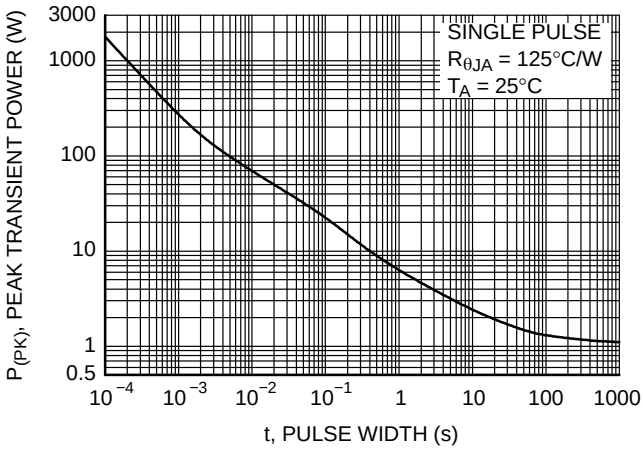


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted) (continued)

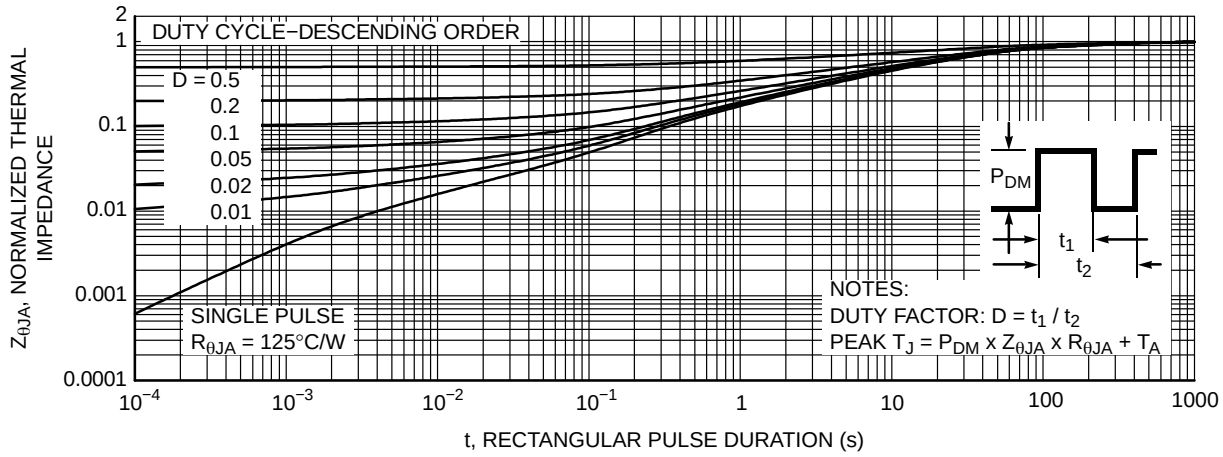
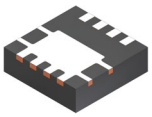


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

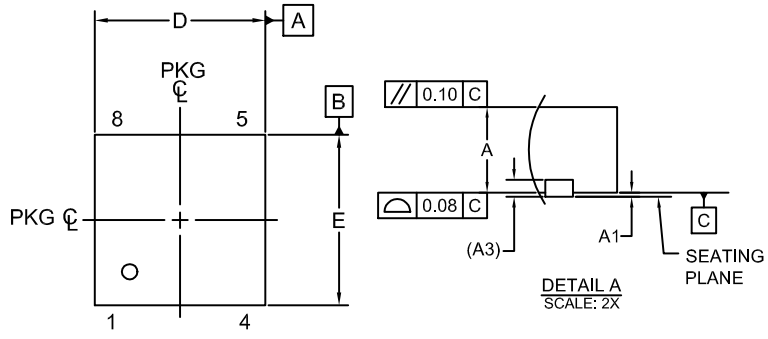
Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMC7660S	FDMC7660S	PQFN8 3.3X3.3, 0.65P (Power 33) (Pb−Free, Halide Free)	13”	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

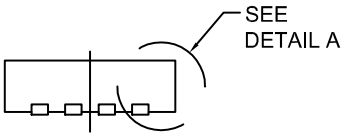


PQFN8 3.3X3.3, 0.65P
CASE 483AK
ISSUE B

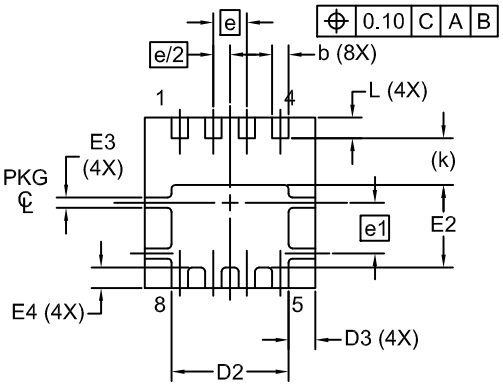
DATE 12 OCT 2021



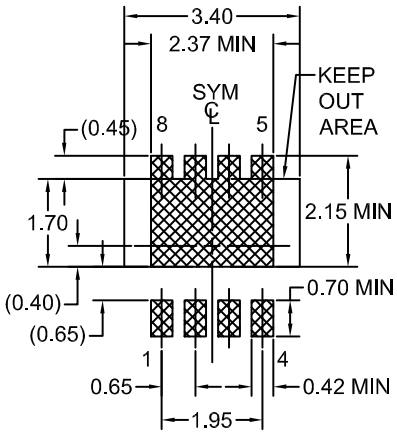
TOP VIEW



FRONT VIEW



BOTTOM VIEW



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
D3	0.42	0.52	0.62
E	3.20	3.30	3.40
E2	1.50	1.60	1.70
E3	0.10	0.20	0.30
E4	0.29	0.39	0.49
e	0.65 BSC		
e/2	0.325 BSC		
e1	0.98 BSC		
k	0.91 REF		
L	0.30	0.40	0.50

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DESCRIPTION:	**PQFN8 3.3X3.3, 0.65P**		**PAGE 1 OF 1**

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