

# MOSFET – N-Channel, POWERTRENCH®

**30 V, 75 A, 1.3 mΩ**

## FDMC8010

### General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance. This device is well suited for applications where ultra low  $R_{DS(on)}$  is required in small spaces such as High performance VRM, POL and Oring functions.

### Features

- Max  $R_{DS(on)}$  = 1.3 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 30\text{ A}$
- Max  $R_{DS(on)}$  = 1.8 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 25\text{ A}$
- High Performance Technology for Extremely Low  $R_{DS(on)}$
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- DC-DC Buck Converters
- Point of Load
- High Efficiency Load Switch and Low Side Switching
- Oring FET

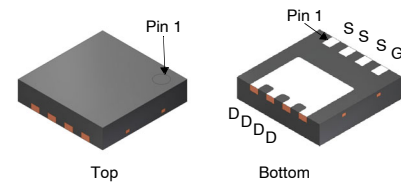
### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage (Note 4)	±20	V
$I_D$	Drain Current		A
	–Continuous (Package limited) $T_C = 25^\circ\text{C}$	75	
	–Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	166	
	–Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	30	
	–Pulsed	120	
EAS	Single Pulse Avalanche Energy (Note 3)	153	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	54	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.4	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	–55 to +150	$^\circ\text{C}$

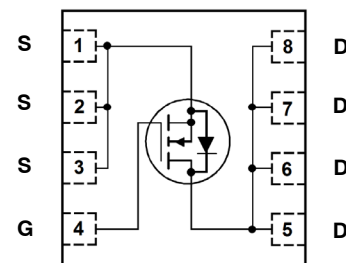
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

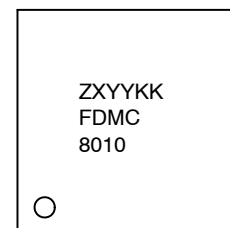
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	$^\circ\text{C}/\text{W}$



WDFN8 3.3x3.3, 0.65P  
(Power 33)  
CASE 483AW



### MARKING DIAGRAM



Z = Assembly Plant Code  
 XYY = Date Code (Year & Week)  
 KK = Lot Traceability Code  
 FDMC8010 = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping†
FDMC8010	WDFN8 (Power 33)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0 V	30			V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 1 mA, referenced to 25°C		15		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 1 mA	1.2	1.5	2.5	V
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 1 mA, referenced to 25°C		-5		mV/°C
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A		0.9	1.3	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 25 A		1.3	1.8	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A, T <sub>J</sub> = 125°C		1.3	2	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 30 A		188		S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		4405	5860	pF
C <sub>oss</sub>	Output Capacitance			1570	2090	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			167	250	pF
R <sub>g</sub>	Gate Resistance		0.1	0.5	1.25	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 30 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω		15	27	ns
t <sub>r</sub>	Rise Time			7.5	15	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			40	64	ns
t <sub>f</sub>	Fall Time			5.3	11	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	V <sub>DD</sub> = 15 V I <sub>D</sub> = 30 A	67	94	nC
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 4.5 V		32	45	nC
Q <sub>gs</sub>	Gate to Source Charge			10		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge			9.5		nC

### DRAIN-SOURCE DIODE CHARACTERISTICS

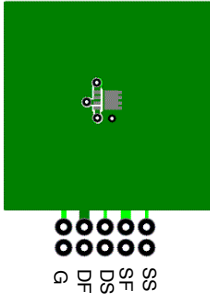
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2 A (Note 2)		0.6	1.2	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 30 A (Note 2)		0.7	1.2	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 30 A, di/dt = 100 A/μs		49	78	ns
Q <sub>rr</sub>	Reverse Recovery Charge			29	46	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

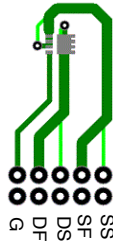
# FDMC8010

## NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0 %.
3.  $E_{AS}$  of 153 mJ is based on starting  $T_J = 25$  °C,  $L = 0.3$  mH,  $I_{AS} = 32$  A,  $V_{DD} = 27$  V,  $V_{GS} = 10$  V. 100% test at  $L = 0.1$  mH,  $I_{AS} = 47$  A.
4. As an N-ch device, the negative  $V_{GS}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS

$T_J = 25^\circ\text{C}$  Unless Otherwise Noted

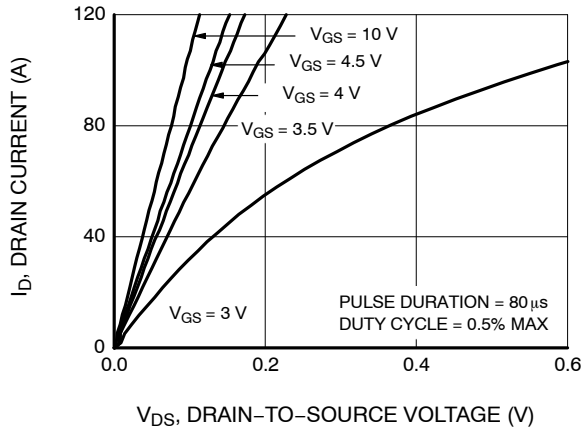


Figure 1. On-Region Characteristics

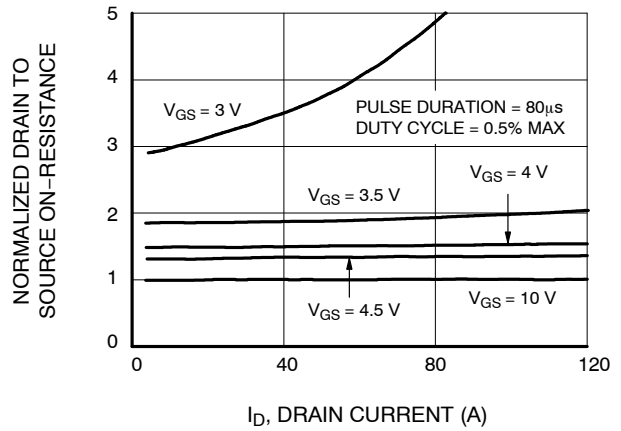


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

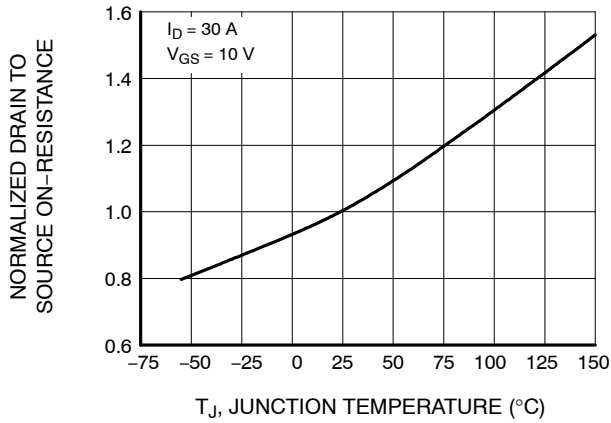


Figure 3. Normalized On Resistance vs Junction Temperature

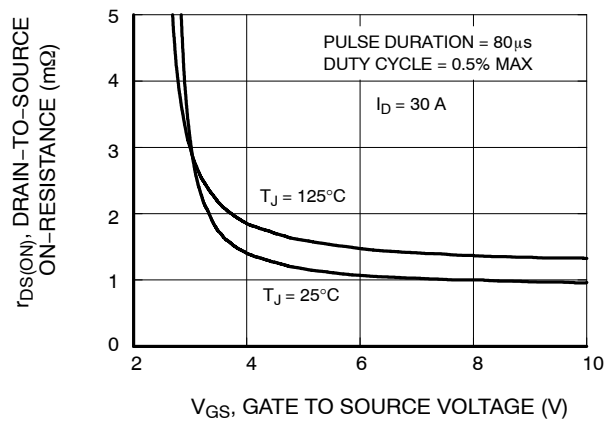


Figure 4. On-Resistance vs Gate to Source Voltage

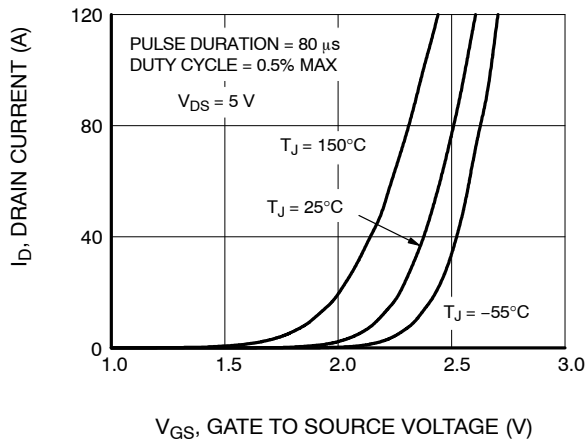


Figure 5. Transfer Characteristics

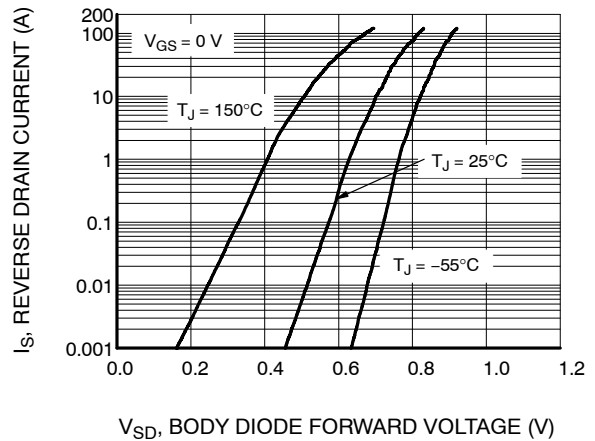


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (continued)

$T_J = 25^\circ\text{C}$  Unless Otherwise Noted

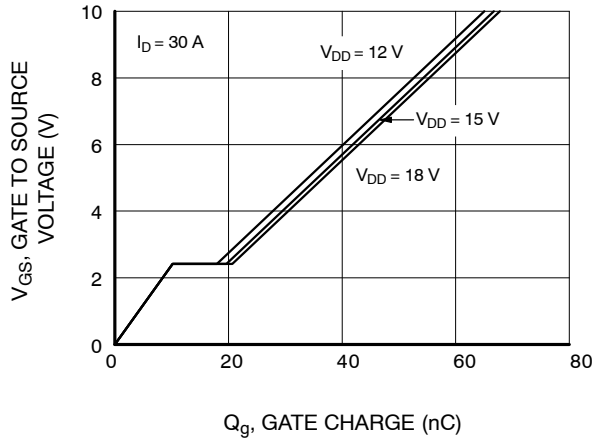


Figure 7. Gate Charge Characteristics

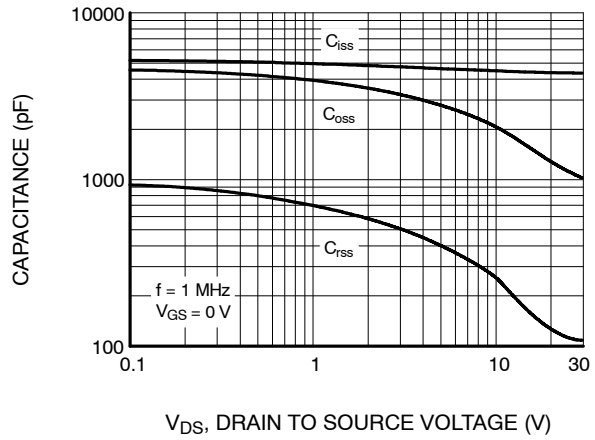


Figure 8. Capacitance vs Drain to Source Voltage

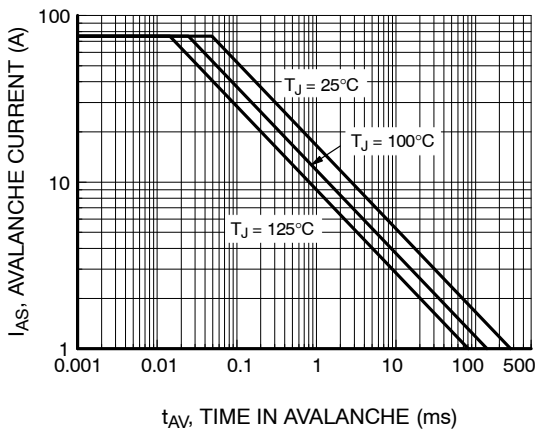


Figure 9. Unclamped Inductive Switching Capability

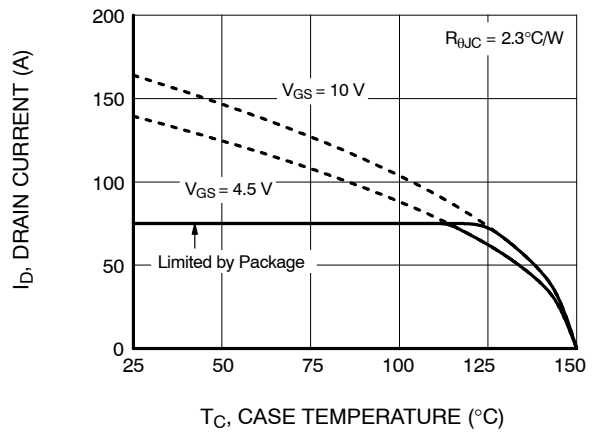


Figure 10. Maximum Continuous Drain Current vs Case Temperature

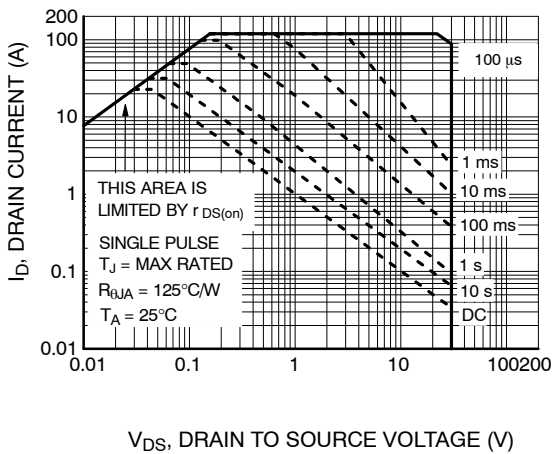


Figure 11. Forward Bias Safe Operating Area

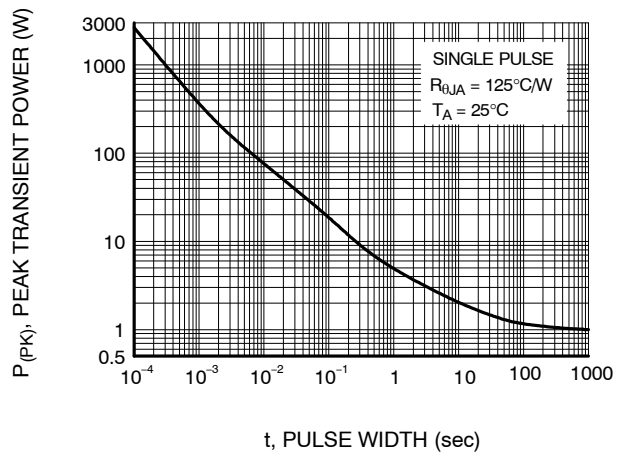
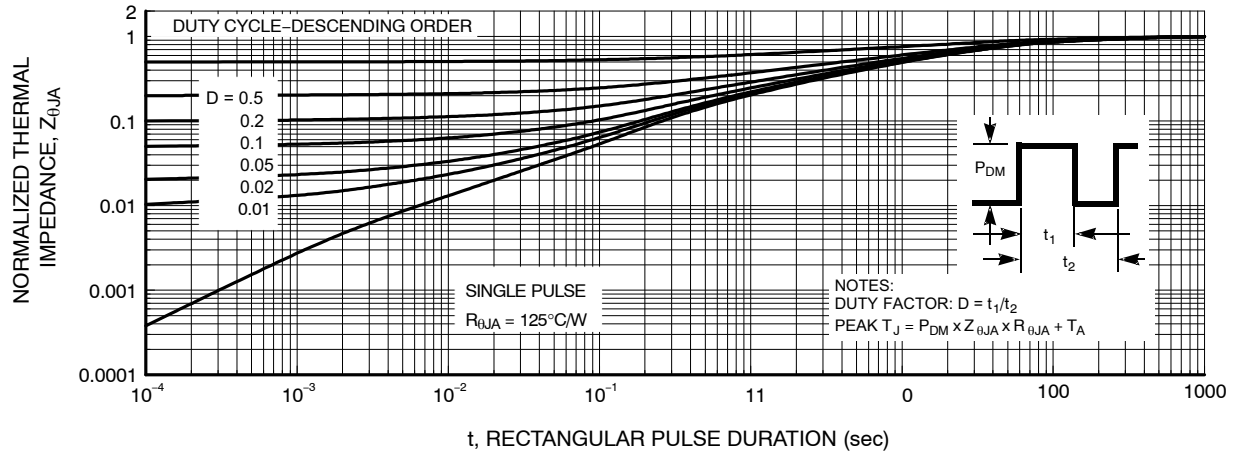


Figure 12. Single Pulse Maximum Power Dissipation

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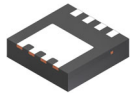
## TYPICAL CHARACTERISTICS (continued)

$T_J = 25^\circ\text{C}$  Unless Otherwise Noted



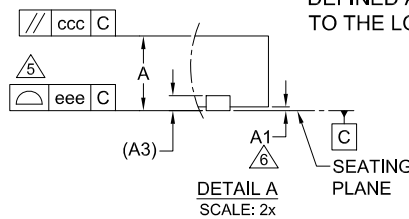
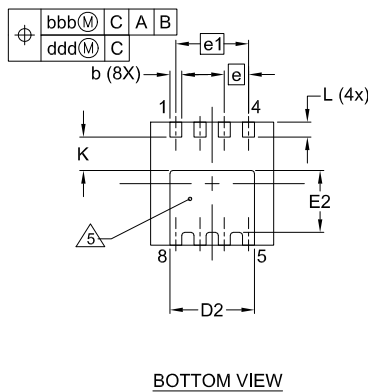
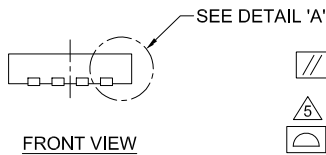
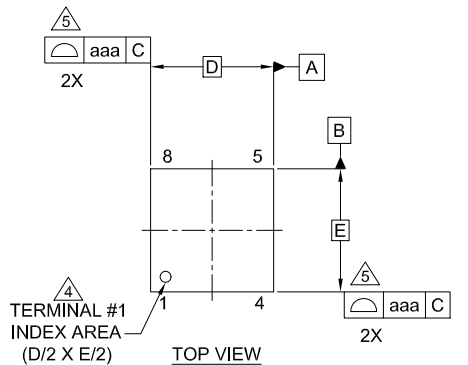
**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

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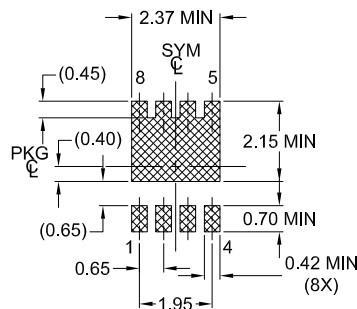


**WDFN8 3.30x3.30x0.75, 0.65P**  
**CASE 483AW**  
**ISSUE B**

DATE 22 MAR 2024



**LAND PATTERN RECOMMENDATION**



**NOTES:**

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP95 SEC. 3 SPP-12. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD, EMBEDDED METAL OR MARKED FEATURE.
5. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	--	--	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.30 BSC		
D2	2.17	2.27	2.37
E	3.30 BSC		
E2	1.56	1.66	1.76
e	0.65 BSC		
e1	1.95 BSC		
K	0.90	--	--
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC MARKING DIAGRAM\***



XXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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