

# MOSFET – N-Channel, Shielded Gate POWERTRENCH®

40 V, 141 A, 2.1 mΩ

## FDMC8360LET40

### General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that incorporates shielded gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

### Features

- Shielded Gate MOSFET Technology
- Max  $R_{DS(on)}$  = 2.1 mΩ at  $V_{GS} = 10$  V,  $I_D = 27$  A
- Max  $R_{DS(on)}$  = 3.1 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 22$  A
- High Performance Technology for Extremely Low  $R_{DS(on)}$
- Termination is Lead-Free
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is RoHS Compliant

### Application

- DC-DC Conversion

### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

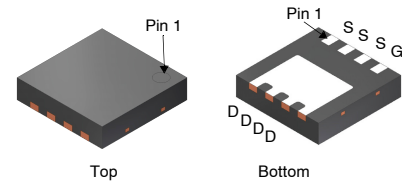
| Symbol         | Parameter  | Ratings     | Units |
|----------------|--|-------------|-------|
| $V_{DS}$       | Drain to Source Voltage                              | 40          | V     |
| $V_{GS}$       | Gate to Source Voltage                               | ±20         | V     |
| $I_D$          | Drain Current  |             | A     |
|                | -Continuous $T_C = 25^\circ\text{C}$ (Note 5)        | 141         |       |
|                | -Continuous $T_C = 100^\circ\text{C}$ (Note 5)       | 100         |       |
|                | -Continuous $T_A = 25^\circ\text{C}$ (Note 1a)       | 27          |       |
|                | -Pulsed (Note 4)                                     | 658         |       |
| EAS            | Single Pulse Avalanche Energy (Note 3)               | 253         | mJ    |
| $P_D$          | Power Dissipation $T_C = 25^\circ\text{C}$           | 75          | W     |
|                | Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a) | 2.8         |       |
| $T_J, T_{STG}$ | Operating and Storage Junction Temperature Range     | -55 to +175 | °C    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

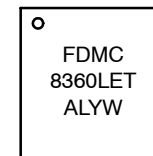
| Symbol          | Parameter   | Ratings | Unit |
|-----------------|---|---------|------|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case (Note 1)     | 2.0     | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1a) | 53      | °C/W |

| $V_{DS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX |
|----------|------------------|-----------|
| 40 V     | 2.1 mΩ @ 10 V    | 141 A     |
|          | 3.1 mΩ @ 4.5 V   |           |



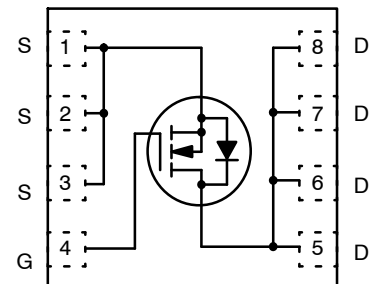
WDFN8 3.3x3.3, 0.65P  
CASE 483AW

### MARKING DIAGRAM



FDMC8360LET = Specific Device Code  
A = Assembly Site  
L = Wafer Lot Number  
YW = Assembly Start Week

### PIN ASSIGNMENT



N-Channel MOSFET

### ORDERING INFORMATION

| Device        | Package                      | Shipping†          |
|---------------|------------------------------|--------------------|
| FDMC8360LET40 | WDFN8 (Pb-Free, Halide Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# FDMC8360LET40

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

| Symbol                               | Parameter                                 | Test Condition                                 | Min | Typ | Max  | Unit  |
|--------------------------------------|---|--|-----|-----|------|-------|
| ΔBV <sub>DSS</sub>                   | Drain to Source Breakdown Voltage         | I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V | 40  | -   | -    | V     |
| ΔBV <sub>DSS</sub> / ΔT <sub>J</sub> | Breakdown Voltage Temperature Coefficient | I <sub>D</sub> = 250 μA, referenced to 25°C    | -   | 20  | -    | mV/°C |
| I <sub>DSS</sub>                     | Zero Gate Voltage Drain Current           | V <sub>DS</sub> = 32 V, V <sub>GS</sub> = 0 V  | -   | -   | 1    | μA    |
| I <sub>GSS</sub>                     | Gate to Source Leakage Current            | V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V | -   | -   | ±100 | nA    |

## ON CHARACTERISTICS

|  |  |   |     |     |     |       |
|--|--|---|-----|-----|-----|-------|
| V <sub>GS(th)</sub>                    | Gate to Source Threshold Voltage                         | V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA           | 1.0 | 1.7 | 3.0 | V     |
| ΔV <sub>GS(th)</sub> / ΔT <sub>J</sub> | Gate to Source Threshold Voltage Temperature Coefficient | I <sub>D</sub> = 250 μA, referenced to 25°C                           | -   | -6  | -   | mV/°C |
| R <sub>DS(on)</sub>                    | Static Drain to Source On Resistance                     | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 27 A                         | -   | 1.4 | 2.1 | mΩ    |
|  |  | V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 22 A                        | -   | 2.1 | 3.1 |       |
|  |  | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 27 A, T <sub>J</sub> = 150°C | -   | 2.3 | 3.5 |       |
| g <sub>FS</sub>                        | Forward Transconductance                                 | V <sub>DS</sub> = 5 V, I <sub>D</sub> = 27 A                          | -   | 138 | -   | S     |

## DYNAMIC CHARACTERISTICS

|                  |                              |   |     |      |      |    |
|------------------|------------------------------|---|-----|------|------|----|
| C <sub>iss</sub> | Input Capacitance            | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V,<br>f = 1 MHz | -   | 3785 | 5300 | pF |
| C <sub>oss</sub> | Output Capacitance           |   | -   | 1220 | 1710 | pF |
| C <sub>rss</sub> | Reverse Transfer Capacitance |   | -   | 57   | 80   | pF |
| R <sub>g</sub>   | Gate Resistance              |   | 0.1 | 0.8  | 1.6  | Ω  |

## SWITCHING CHARACTERISTICS

|                     |                               |  |   |    |     |    |    |
|---------------------|-------------------------------|--|---|----|-----|----|----|
| t <sub>d(on)</sub>  | Turn-On Delay Time            | V <sub>DD</sub> = 20 V, I <sub>D</sub> = 27 A,<br>V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω | -   | 14 | 26  | ns |    |
| t <sub>r</sub>      | Rise Time                     |  | -   | 8  | 16  | ns |    |
| t <sub>d(off)</sub> | Turn-Off Delay Time           |  | -   | 35 | 57  | ns |    |
| t <sub>f</sub>      | Fall Time                     |  | -   | 7  | 14  | ns |    |
| Q <sub>g(TOT)</sub> | Total Gate Charge             | V <sub>GS</sub> = 0 V to 10 V  | V <sub>DD</sub> = 20 V<br>I <sub>D</sub> = 27 A | -  | 57  | 80 | nC |
| Q <sub>g(TOT)</sub> | Total Gate Charge             | V <sub>GS</sub> = 0 V to 4.5 V   |   | -  | 27  | 38 | nC |
| Q <sub>gs</sub>     | Gate to Source Charge         |  |   | -  | 9.9 | -  | nC |
| Q <sub>gd</sub>     | Gate to Drain "Miller" Charge |  |   | -  | 8.1 | -  | nC |

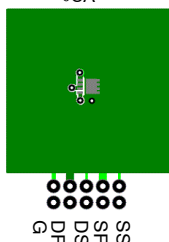
## DRAIN-SOURCE DIODE CHARACTERISTICS

|                 |                                       |  |   |     |     |    |
|-----------------|---------------------------------------|--|---|-----|-----|----|
| V <sub>SD</sub> | Source to Drain Diode Forward Voltage | V <sub>GS</sub> = 0 V, I <sub>S</sub> = 27 A (Note 2)  | - | 0.8 | 1.3 | V  |
|                 |                                       | V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.9 A (Note 2) | - | 0.7 | 1.2 |    |
| t <sub>rr</sub> | Reverse Recovery Time                 | I <sub>F</sub> = 27 A, di/dt = 100 A/μs                | - | 47  | 76  | ns |
| Q <sub>rr</sub> | Reverse Recovery Charge               |  | - | 30  | 48  | nC |

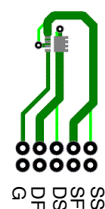
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTES:

- R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



a. 53°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
- E<sub>AS</sub> of 253 mJ is based on starting T<sub>J</sub> = 25 °C, L = 3 mH, I<sub>AS</sub> = 13 A, V<sub>DD</sub> = 40 V, V<sub>GS</sub> = 10 V. 100% test at L = 0.1 mH, I<sub>AS</sub> = 42 A.
- Pulsed I<sub>d</sub> please refer to Figure 11 SOA graph for more details
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

# FDMC8360LET40

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

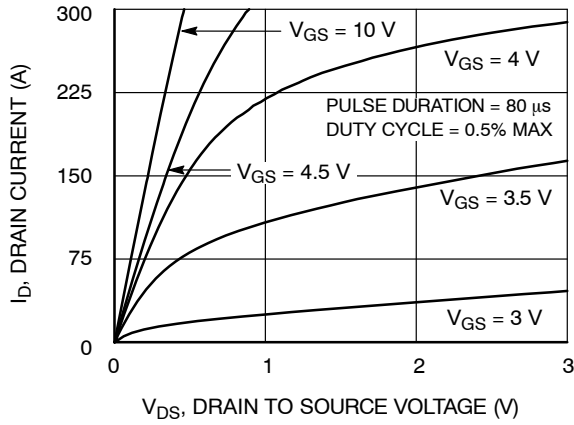


Figure 1. On Region Characteristics

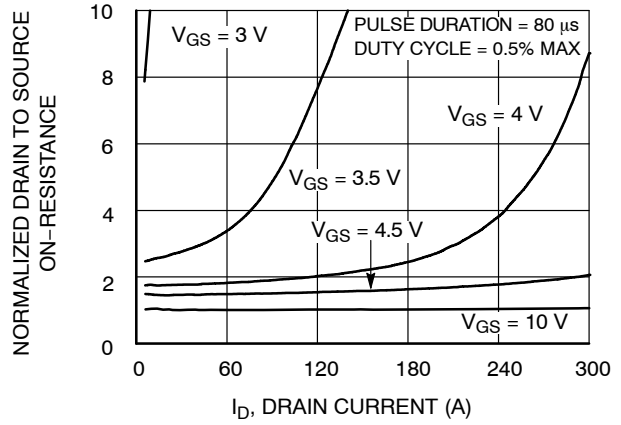


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

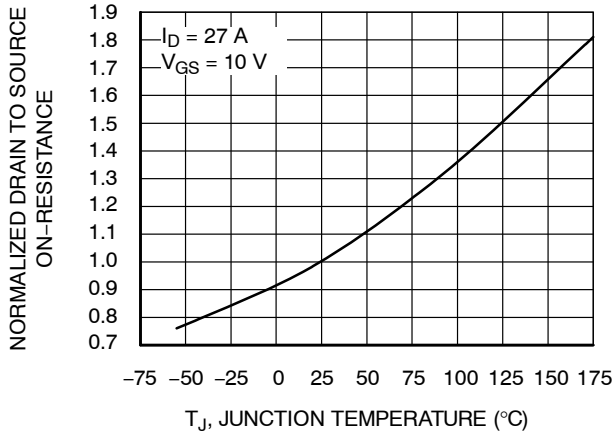


Figure 3. Normalized On Resistance vs. Junction Temperature

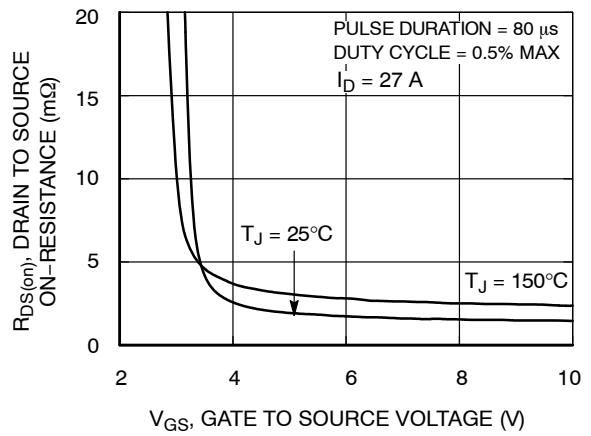


Figure 4. On-Resistance vs. Gate to Source Voltage

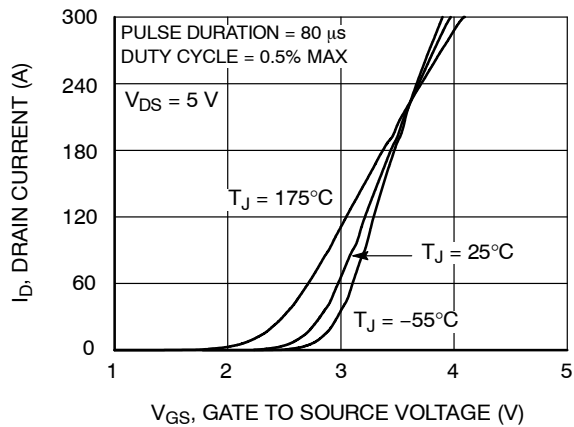


Figure 5. Transfer Characteristics

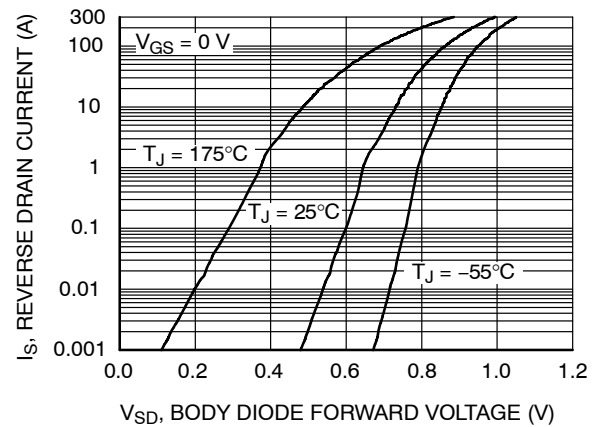
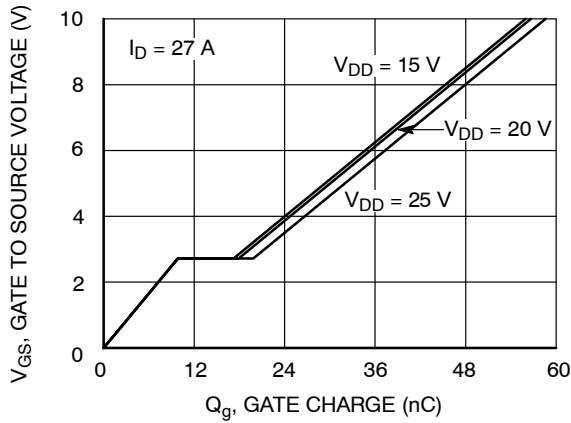


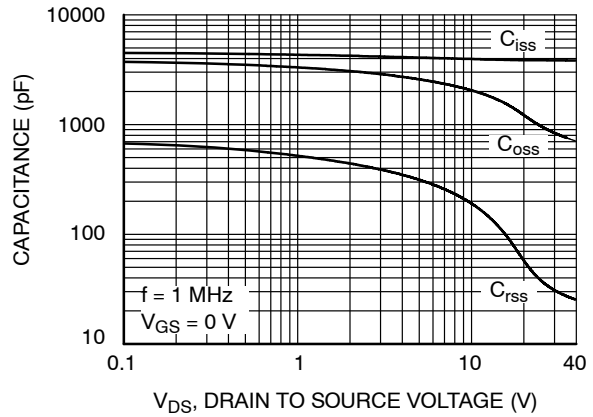
Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# FDMC8360LET40

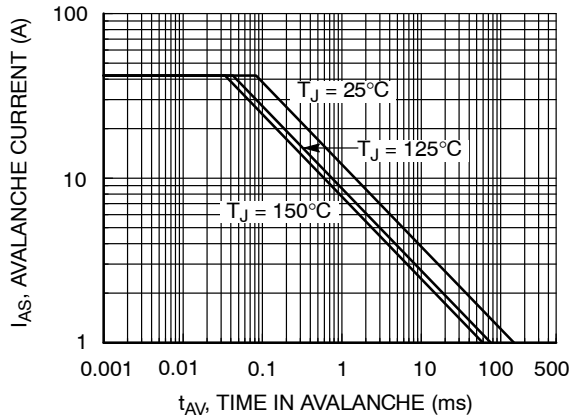
## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)



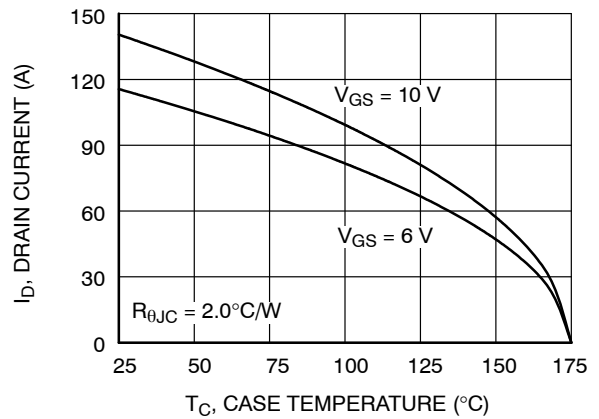
**Figure 7. Gate Charge Characteristics**



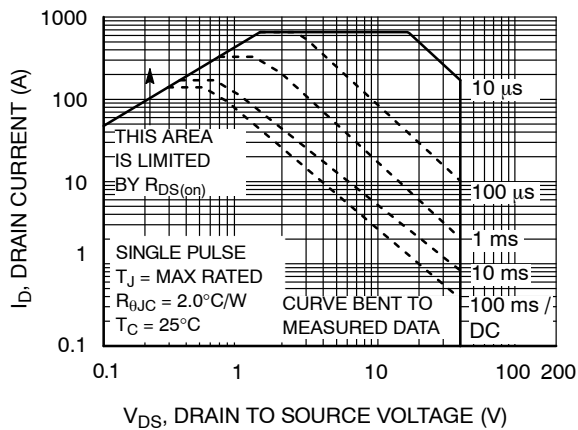
**Figure 8. Capacitance vs. Drain to Source Voltage**



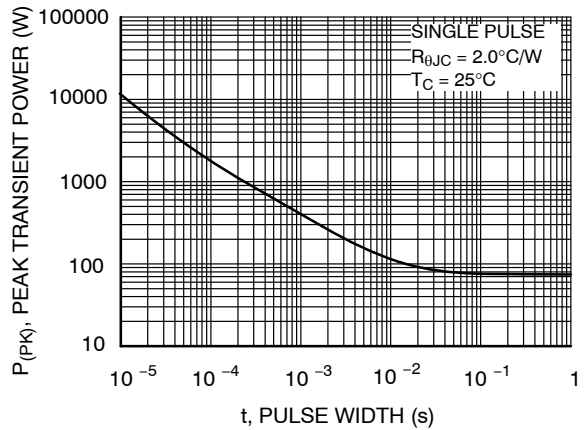
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**



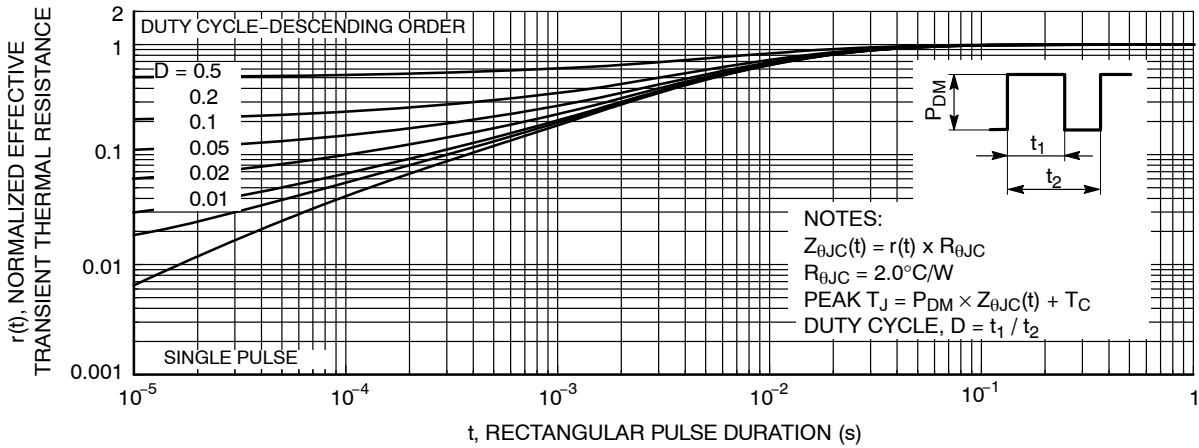
**Figure 11. Forward Bias Safe Operating Area**



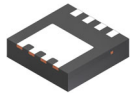
**Figure 12. Single Pulse Maximum Power Dissipation**

# FDMC8360LET40

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

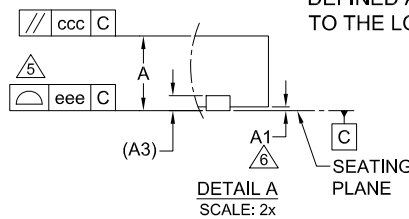
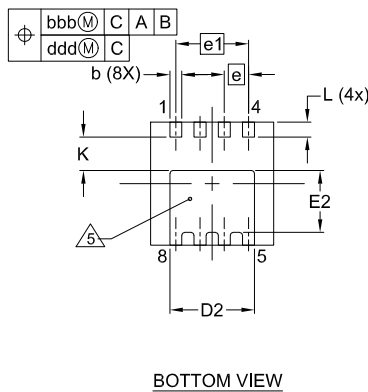
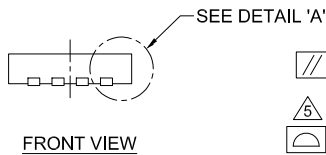
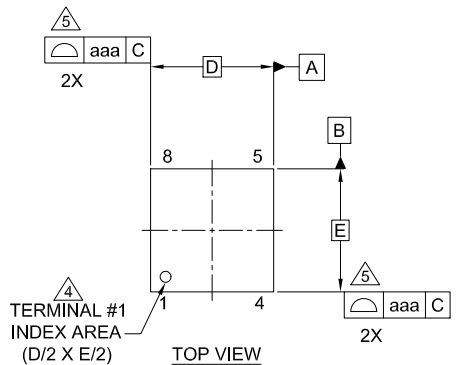


**Figure 13. Junction-to-Case Transient Thermal Response Curve**

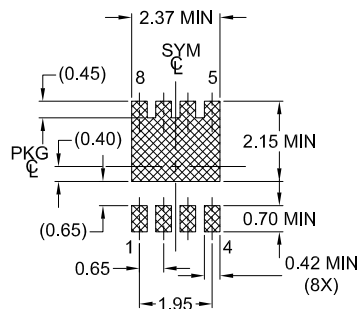


**WDFN8 3.30x3.30x0.75, 0.65P  
CASE 483AW  
ISSUE B**

DATE 22 MAR 2024



**LAND PATTERN  
RECOMMENDATION**



**NOTES:**

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP95 SEC. 3 SPP-12. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD, EMBEDDED METAL OR MARKED FEATURE.
5. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN         | NOM  | MAX  |
| A   | 0.70        | 0.75 | 0.80 |
| A1  | --          | --   | 0.05 |
| A3  | 0.20 REF    |      |      |
| b   | 0.27        | 0.32 | 0.37 |
| D   | 3.30 BSC    |      |      |
| D2  | 2.17        | 2.27 | 2.37 |
| E   | 3.30 BSC    |      |      |
| E2  | 1.56        | 1.66 | 1.76 |
| e   | 0.65 BSC    |      |      |
| e1  | 1.95 BSC    |      |      |
| K   | 0.90        | --   | --   |
| L   | 0.30        | 0.40 | 0.50 |
| aaa | 0.10        |      |      |
| bbb | 0.10        |      |      |
| ccc | 0.10        |      |      |
| ddd | 0.05        |      |      |
| eee | 0.05        |      |      |

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC  
MARKING DIAGRAM\***



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

|                         |                                    |  |
|-------------------------|------------------------------------|--|
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| <b>DESCRIPTION:</b>     | <b>WDFN8 3.30x3.30x0.75, 0.65P</b> | <b>PAGE 1 OF 1</b>   |

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