

# MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

60 V, 87 A, 4.3 mΩ

## FDMC86570LET60

### General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

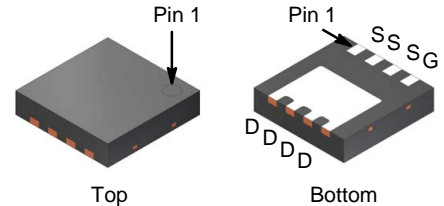
### Features

- Extended T<sub>J</sub> Rating to 175°C
- Shielded Gate MOSFET Technology
- Max r<sub>DS(on)</sub> = 4.3 mΩ at V<sub>GS</sub> = 10 V, I<sub>D</sub> = 18 A
- Max r<sub>DS(on)</sub> = 6.5 mΩ at V<sub>GS</sub> = 4.5 V, I<sub>D</sub> = 15 A
- High Performance Technology for Extremely Low r<sub>DS(on)</sub>
- Termination is Lead-free
- RoHS Compliant

### Applications

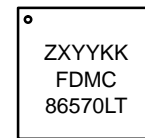
- DC-DC Conversion

V <sub>DS</sub>	r <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX
60 V	4.3 mΩ @ 10 V	87 A
	6.5 mΩ @ 4.5 V	



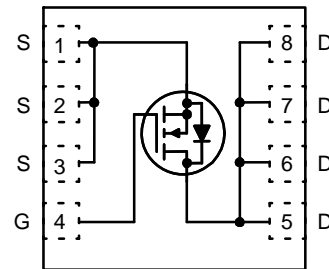
WDFN8 3.3x3.3, 0.65P  
(Power 33)  
CASE 483 AW

### MARKING DIAGRAM



Z = Assembly Plant Code  
 XYY = 3-Digit Date Code Format  
 KK = 2-Alphanumeric Lot Run Traceability Code  
 FDMC86570LT = Device Code

### PIN ASSIGNMENT



### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# FDMC86570LET60

## MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	60	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous	$T_C = 25^\circ\text{C}$ (Note 5)	87
	– Continuous	$T_C = 100^\circ\text{C}$ (Note 5)	62
	– Continuous	$T_A = 25^\circ\text{C}$ (Note 1a)	18
	– Pulsed	(Note 4)	436
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	253
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	65
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	2.8
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	$-55$ to $+175$	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	2.3
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	60	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	–	30	–	$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$	–	–	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	–	–	$\pm 100$	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	–	–7	–	$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 18 \text{ A}$	–	3.1	4.3	$\text{m}\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}$	–	4.7	6.5	
		$V_{GS} = 10 \text{ V}, I_D = 18 \text{ A}, T_J = 125^\circ\text{C}$	–	5.0	6.9	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5 \text{ V}, I_D = 18 \text{ A}$	–	75	–	S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	–	4790	–	pF
$C_{oss}$	Output Capacitance		–	821	–	pF
$C_{rss}$	Reverse Transfer Capacitance		–	19	–	pF
$R_g$	Gate Resistance		0.1	0.9	2.7	$\Omega$

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30 \text{ V}, I_D = 18 \text{ A}, V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	–	19	34	ns
$t_r$	Rise Time		–	6.2	12	ns
$t_{d(off)}$	Turn-Off Delay Time		–	38	61	ns
$t_f$	Fall Time		–	3.9	10	ns

# FDMC86570LET60

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### SWITCHING CHARACTERISTICS

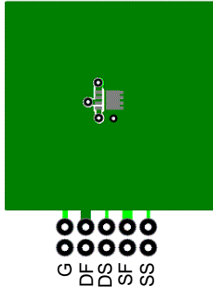
$Q_{g(\text{TOT})}$	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}, V_{DD} = 30\text{ V}, I_D = 18\text{ A}$	–	63	88	nC
$Q_{g(\text{TOT})}$	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}, V_{DD} = 30\text{ V}, I_D = 18\text{ A}$	–	29	41	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 30\text{ V}, I_D = 18\text{ A}$	–	14	–	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		–	6.3	–	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS

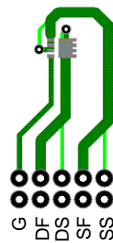
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 18\text{ A}$ (Note 2)	–	0.8	1.3	V
		$V_{GS} = 0\text{ V}, I_S = 1.9\text{ A}$ (Note 2)	–	0.7	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 18\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	–	43	69	ns
$Q_{rr}$	Reverse Recovery Charge		–	26	42	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a.  $53^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.
- $E_{AS}$  of 253 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 13\text{ A}$ ,  $V_{DD} = 60\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 43\text{ A}$ .
- Pulsed  $I_d$  please refer to Figure 11 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

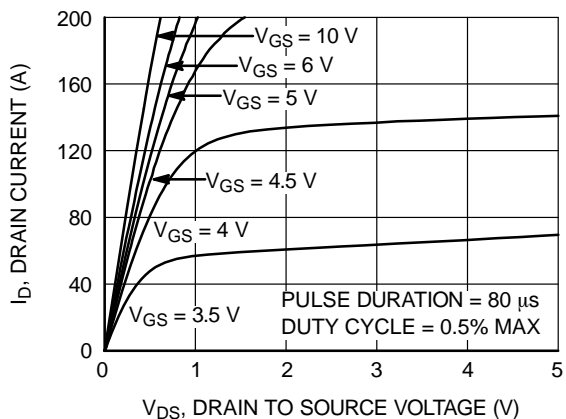


Figure 1. On-Region Characteristics

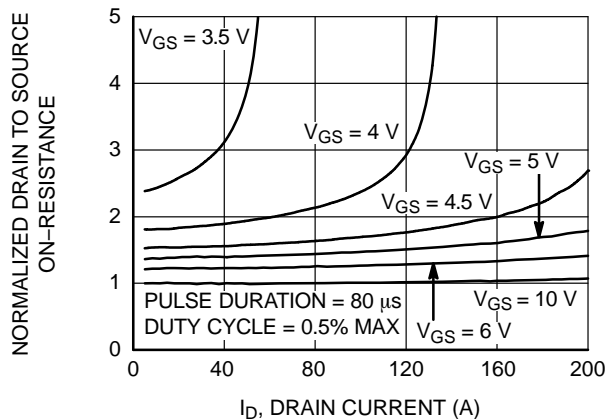


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

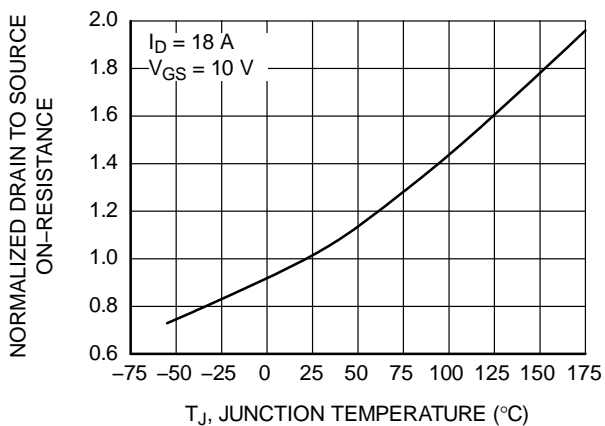


Figure 3. Normalized On-Resistance vs. Junction Temperature

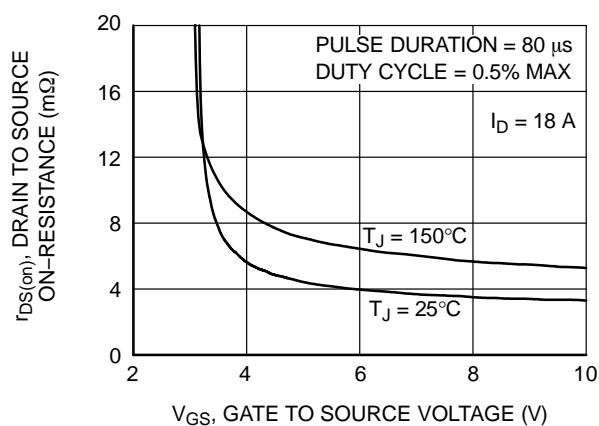


Figure 4. On-Resistance vs. Gate to Source Voltage

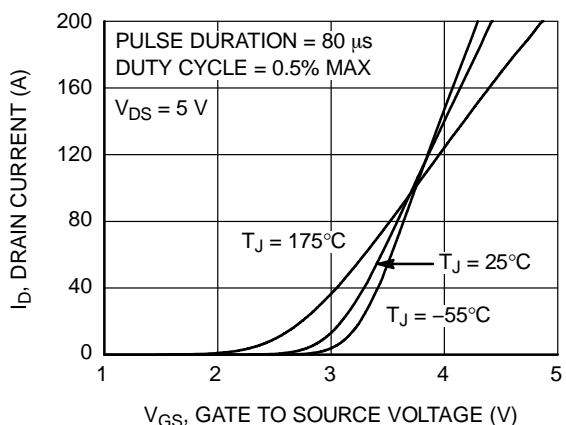


Figure 5. Transfer Characteristics

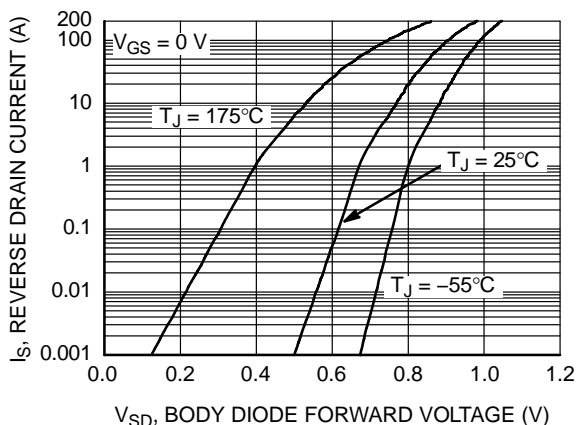


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# FDMC86570LET60

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

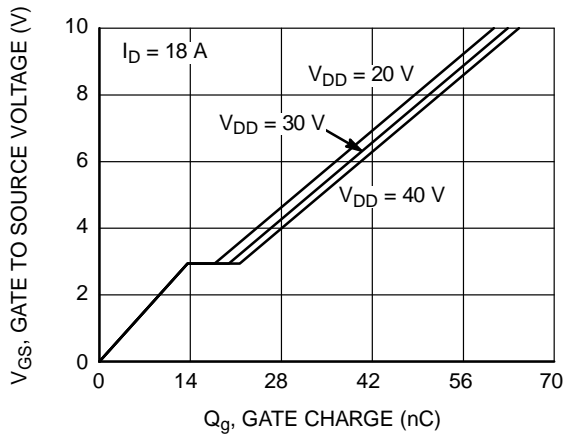


Figure 7. Gate Charge Characteristics

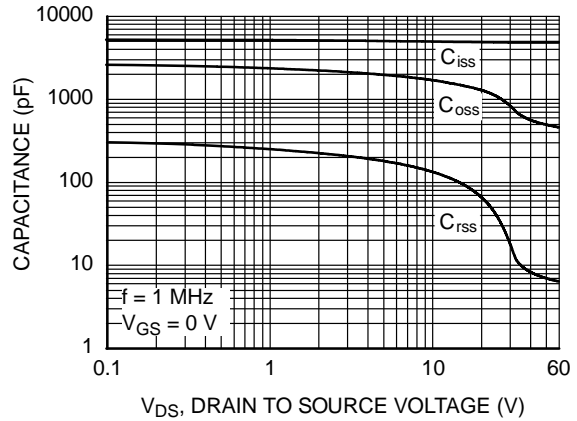


Figure 8. Capacitance vs. Drain to Source Voltage

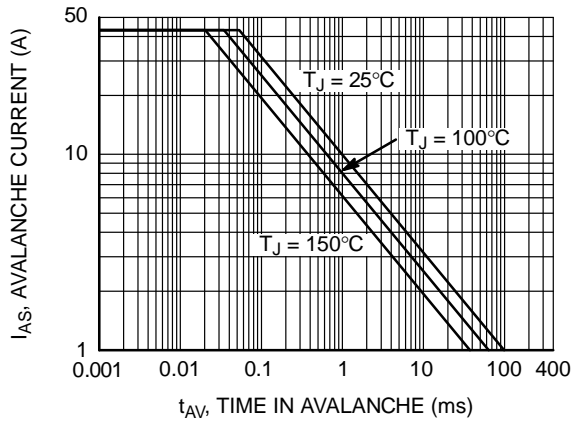


Figure 9. Unclamped Inductive Switching Capability

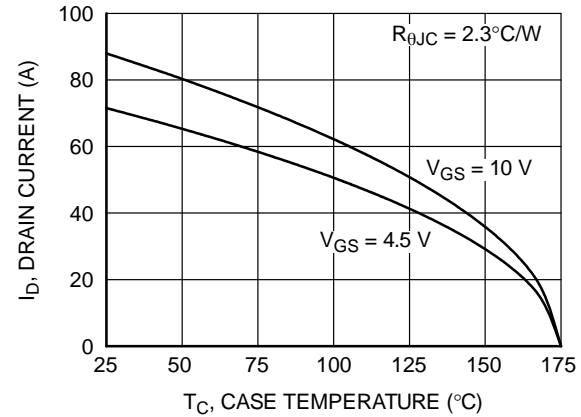


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

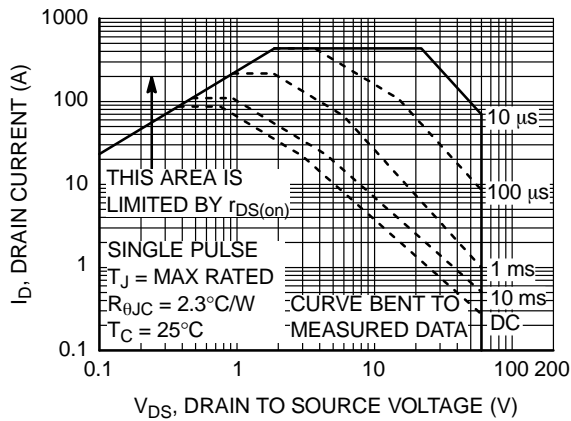


Figure 11. Forward Bias Safe Operating Area

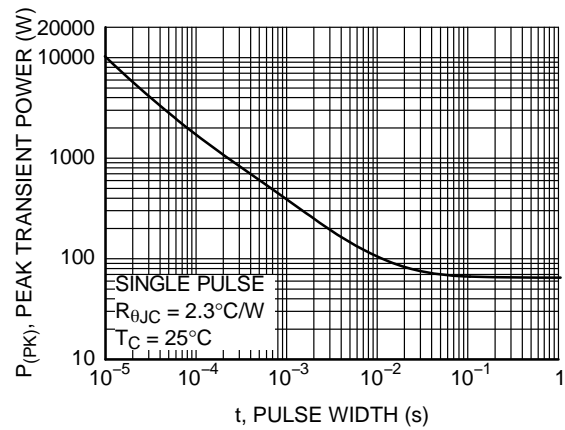


Figure 12. Single Pulse Maximum Power Dissipation

# FDMC86570LET60

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

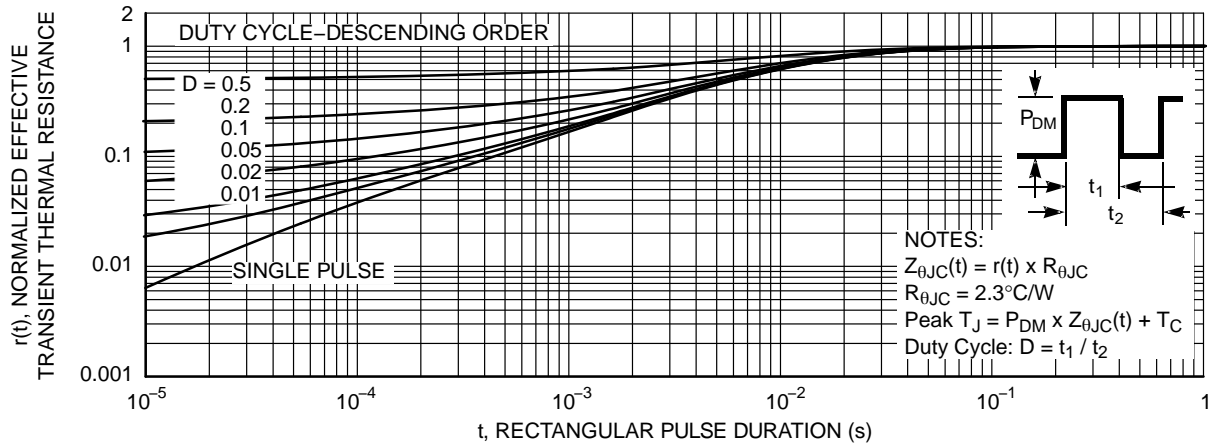
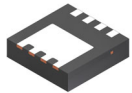


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

### PACKAGE MARKING AND ORDERING INFORMATION

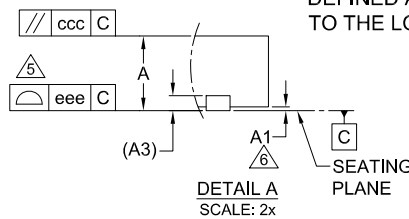
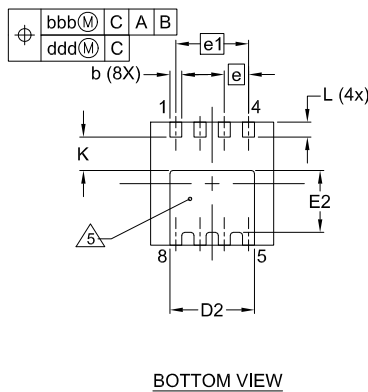
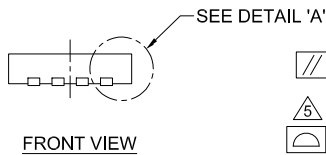
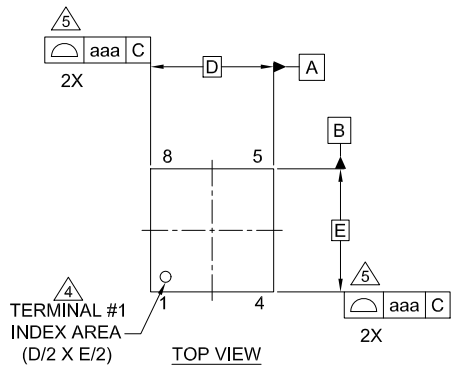
Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping <sup>†</sup>
FDMC86570LET60	FDMC86570LT	WDFN8 3.3x3.3, 0.65P Power 33	13"	12 mm	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

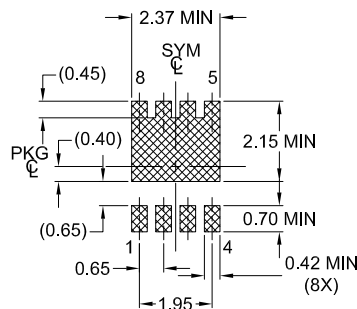


**WDFN8 3.30x3.30x0.75, 0.65P**  
**CASE 483AW**  
**ISSUE B**

DATE 22 MAR 2024



**LAND PATTERN RECOMMENDATION**



**NOTES:**

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP95 SEC. 3 SPP-12. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD, EMBEDDED METAL OR MARKED FEATURE.
5. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	--	--	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.30 BSC		
D2	2.17	2.27	2.37
E	3.30 BSC		
E2	1.56	1.66	1.76
e	0.65 BSC		
e1	1.95 BSC		
K	0.90	--	--
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC MARKING DIAGRAM\***



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>WDFN8 3.30x3.30x0.75, 0.65P</b>	<b>PAGE 1 OF 1</b>

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