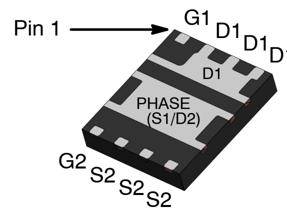
MOSFET – Dual, N-Channel, Asymmetric, POWERTRENCH®, Power Stage

FDMS3664S



PQFN8 5 × 6, 1.27P
(Power 56)
CASE 483AJ

General Description

This device includes two specialized N–Channel MOSFETs in a dual PQFN package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

Features

Q1: N–Channel

- Max $R_{DS(on)}$ = 8 mΩ at V_{GS} = 10 V, I_D = 13 A
- Max $R_{DS(on)}$ = 11 mΩ at V_{GS} = 4.5 V, I_D = 11 A

Q2: N–Channel

- Max $R_{DS(on)}$ = 2.6 mΩ at V_{GS} = 10 V, I_D = 25 A
- Max $R_{DS(on)}$ = 3.2 mΩ at V_{GS} = 4.5 V, I_D = 22 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- This Device is Pb–Free, Halide Free and is RoHS Compliant

Applications

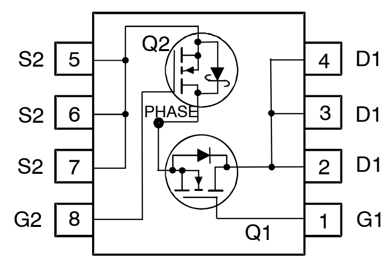
- Computing
- Communications
- General Purpose Point of Load
- Notebook VCORE

MARKING DIAGRAM

&Z&3&K
22CF
10OD

&Z	=	Assembly Plant Code
&3	=	3–Digit Date Code
&K	=	2–Digit Lot Run Traceability Code
22CF10OD	=	Specific Device Code

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
FDMS3664S	PQFN8 (Pb–Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter			Q1	Q2	Unit
V_{DS}	Drain to Source Voltage			30	30	V
V_{DSt}	Drain to Source Transient Voltage ($t_{Transient}$ < 100 ns)			33	33	V
V_{GS}	Gate to Source Voltage (Note 3)			±20	±12	V
I_D	Drain Current	Continuous (Package limited)	T_C = 25°C	30	60	A
		Continuous (Silicon limited)	T_C = 25°C	60	118	
		Continuous	T_A = 25°C	13 (Note 1a)	25 (Note 1b)	
		Pulsed		40	100	
E_{AS}	Single Pulse Avalanche Energy			33 (Note 4)	48 (Note 5)	mJ
P_D	Power Dissipation for Single Operation		T_A = 25°C	2.2 (Note 1a)	2.5 (Note 1b)	W
			T_A = 25°C	1 (Note 1c)	1 (Note 1d)	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	57 (Note 1a)	50 (Note 1b)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125 (Note 1c)	120 (Note 1d)	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.9	2.3	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	30 30	– –	– –	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C I_D = 10 mA, referenced to 25°C	Q1 Q2	– –	16 18	– –	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2	– –	– –	1 500	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 20 V, V_{DS} = 0 V V_{GS} = 12 V, V_{DS} = 0 V	Q1 Q2	– –	– –	100 100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA V_{GS} = V_{DS}, I_D = 1 mA	Q1 Q2	1.1 1.1	1.9 1.6	2.7 2.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C I_D = 10 mA, referenced to 25°C	Q1 Q2	– –	–6 –3	– –	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 13 A V_{GS} = 4.5 V, I_D = 11 A V_{GS} = 10 V, I_D = 13 A, T_J = 125°C	Q1	– – –	4 6 5.7	8 11 8.7	mΩ
		V_{GS} = 10 V, I_D = 25 A V_{GS} = 4.5 V, I_D = 22 A V_{GS} = 10 V, I_D = 25 A, T_J = 125°C	Q2	– – –	2.0 2.5 2.9	2.6 3.2 4.5	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 13 A V_{DS} = 5 V, I_D = 25 A	Q1 Q2	– –	62 179	– –	S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	Q1: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz Q2: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Q1 Q2	– –	1325 2515	1765 3345	pF
C_{oss}	Output Capacitance		Q1 Q2	– –	466 645	620 860	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2	– –	46 74	70 115	pF
R_g	Gate Resistance		Q1 Q2	0.2 0.2	0.6 0.9	2 3	Ω
SWITCHING CHARACTERISTICS							
$t_{d(on)}$	Turn-On Delay Time	Q1: V_{DD} = 15 V, I_D = 13 A, R_{GEN} = 6 Ω Q2: V_{DD} = 15 V, I_D = 25 A, R_{GEN} = 6 Ω	Q1 Q2	– –	7.7 9.2	15 18	ns
t_r	Rise Time		Q1 Q2	– –	2.2 3.4	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2	– –	19 28	34 46	ns
t_f	Fall Time		Q1 Q2	– –	1.8 2.4	10 10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V (Q1: V_{DD} = 15 V, I_D = 13 A; Q2: V_{DD} = 15 V, I_D = 25 A)	Q1 Q2	– –	21 37	29 52	nC
		V_{GS} = 0 V to 4.5 V (Q1: V_{DD} = 15 V, I_D = 13 A; Q2: V_{DD} = 15 V, I_D = 25 A)	Q1 Q2	– –	9.5 17	13 24	nC
Q_{gs}	Gate to Source Charge	Q1: V_{DD} = 15 V, I_D = 13 A Q2: V_{DD} = 15 V, I_D = 25 A	Q1 Q2	– –	3.9 5.9	– –	nC
Q_{gd}	Gate to Drain “Miller” Charge		Q1 Q2	– –	2.6 4	– –	nC

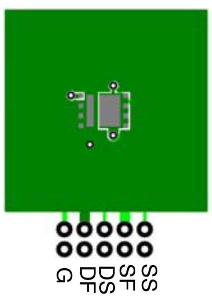
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source−Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 13 A (Note 2) V_{GS} = 0 V, I_S = 2 A (Note 2)	Q1 Q1	– –	0.8 0.7	1.2 1.2	V
		V_{GS} = 0 V, I_S = 25 A (Note 2) V_{GS} = 0 V, I_S = 2 A (Note 2)	Q2 Q2	– –	0.8 0.6	1.2 1.2	
t_{rr}	Reverse Recovery Time	Q1: I_F = 13 A, di/dt = 100 A/μs Q2: I_F = 25 A, di/dt = 300 A/μs	Q1 Q2	– –	26 24	42 38	ns
Q_{rr}	Reverse Recovery Charge		Q1 Q2	– –	10 22	20 34	nC

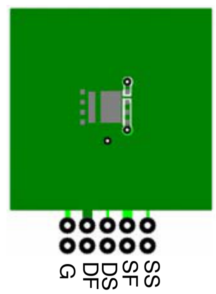
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

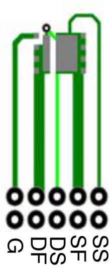
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 57°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper.



a) 125°C/W when mounted on a minimum pad of 2 oz copper.

b) 120°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. As an N−ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied with the negative Vgs rating.
4. E_{AS} of 33 mJ is based on starting T_J = 25°C, N−ch: L = 1.9 mH, I_{AS} = 6 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 16 A.
5. E_{AS} of 48 mJ is based on starting T_J = 25°C, N−ch: L = 0.6 mH, I_{AS} = 13 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 23 A.

TYPICAL CHARACTERISTICS (Q1 N−Channel)

(T_J = 25°C unless otherwise noted)

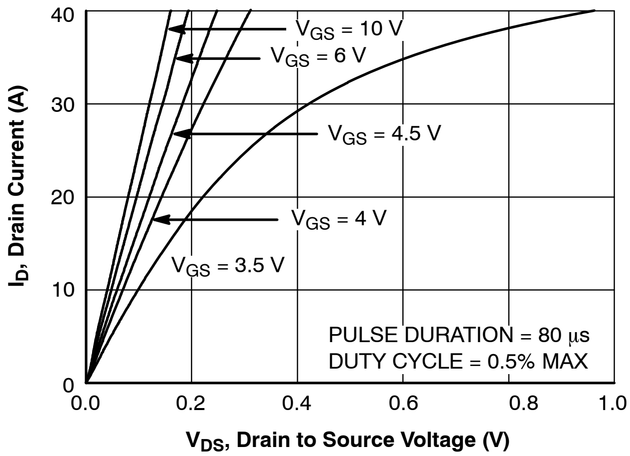


Figure 1. On Region Characteristics

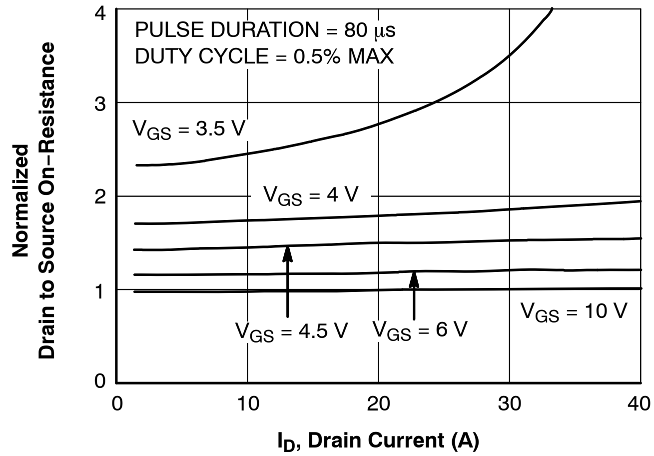


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

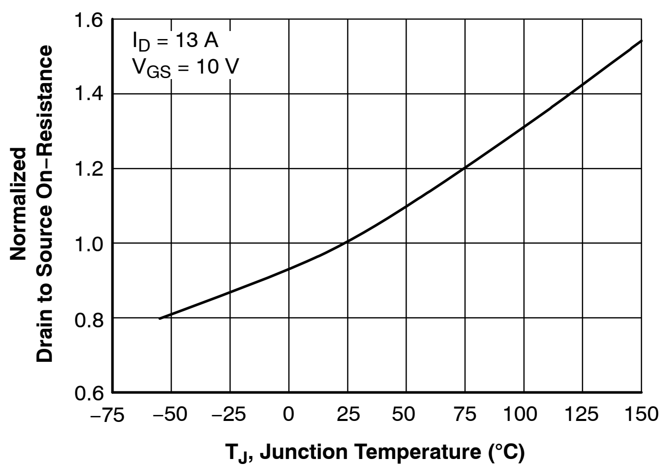


Figure 3. Normalized On Resistance vs. Junction Temperature

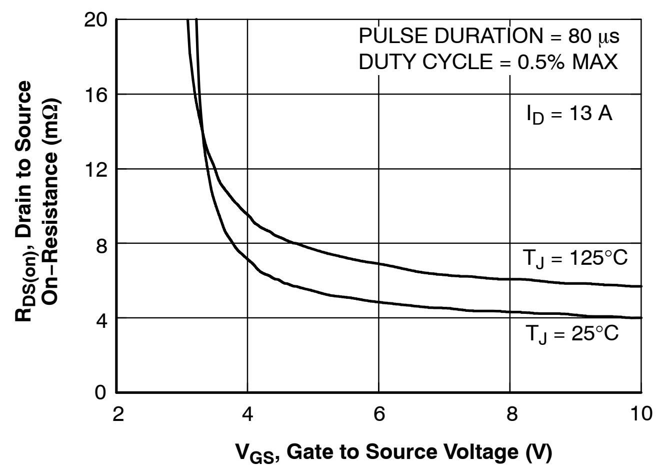


Figure 4. On−Resistance vs. Gate to Source Voltage

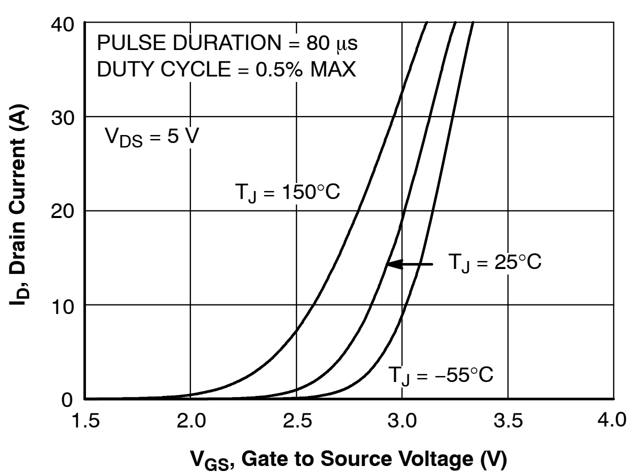


Figure 5. Transfer Characteristics

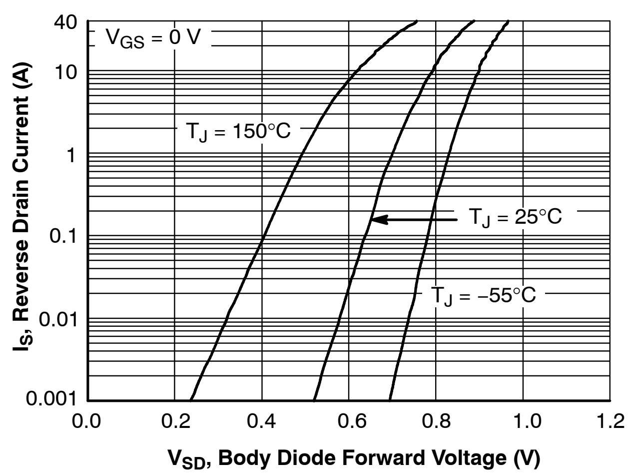


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1 N−Channel) (continued)

(T_J = 25°C unless otherwise noted)

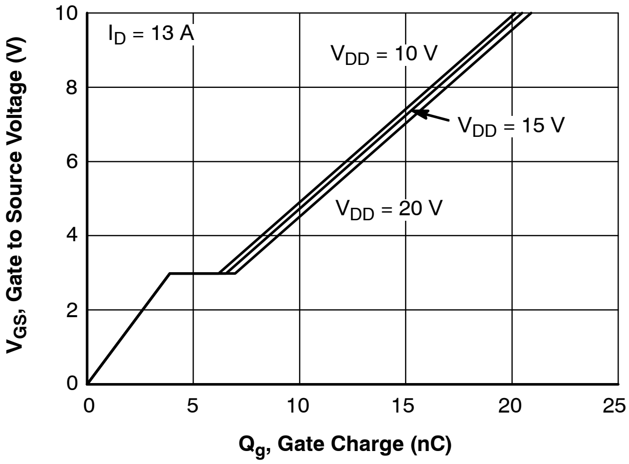


Figure 7. Gate Charge Characteristics

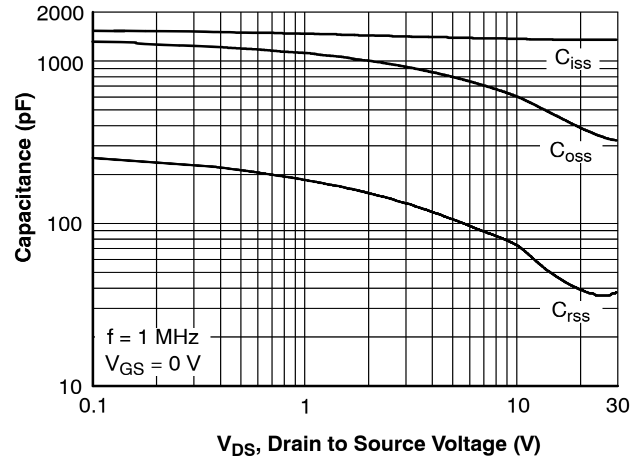


Figure 8. Capacitance vs. Drain to Source Voltage

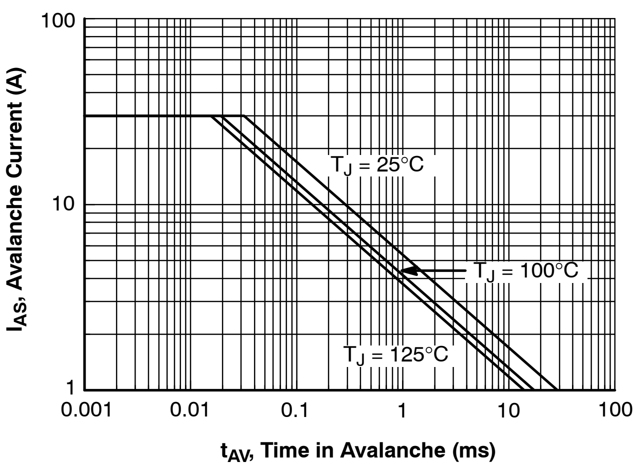


Figure 9. Unclamped Inductive Switching Capability

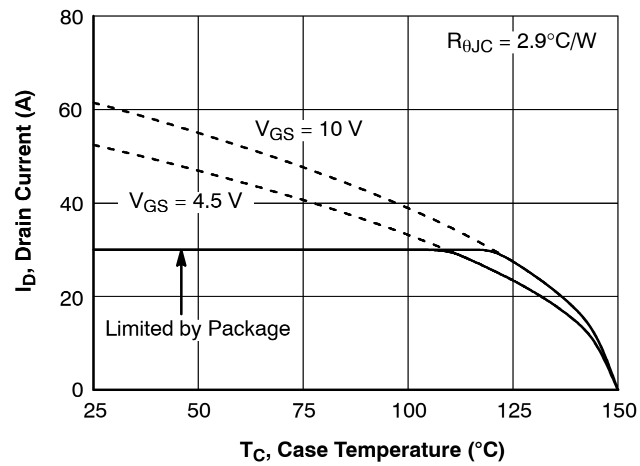


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

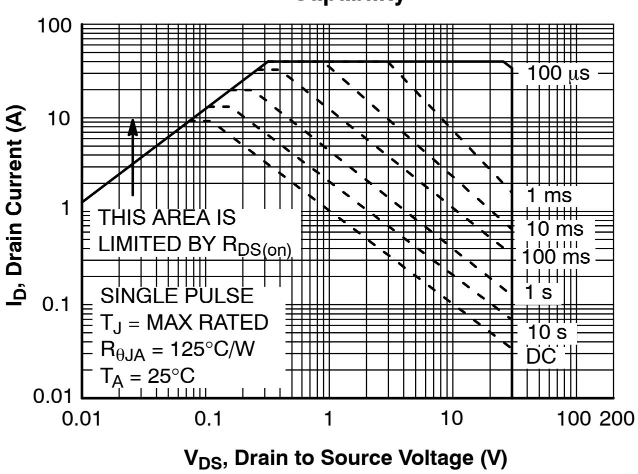


Figure 11. Forward Bias Safe Operating Area

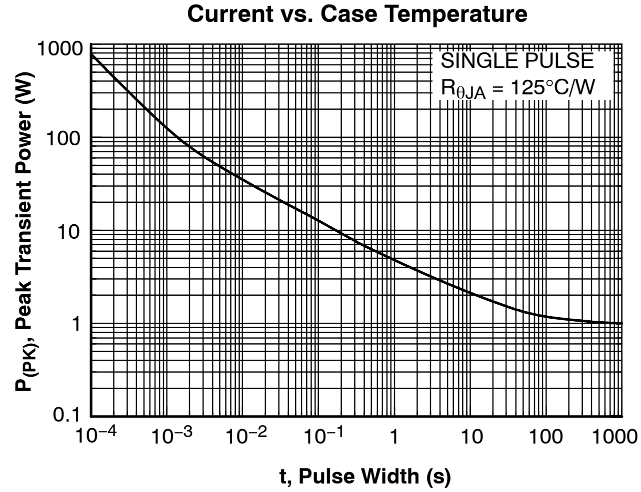


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q1 N−Channel) (continued)

(T_J = 25°C unless otherwise noted)

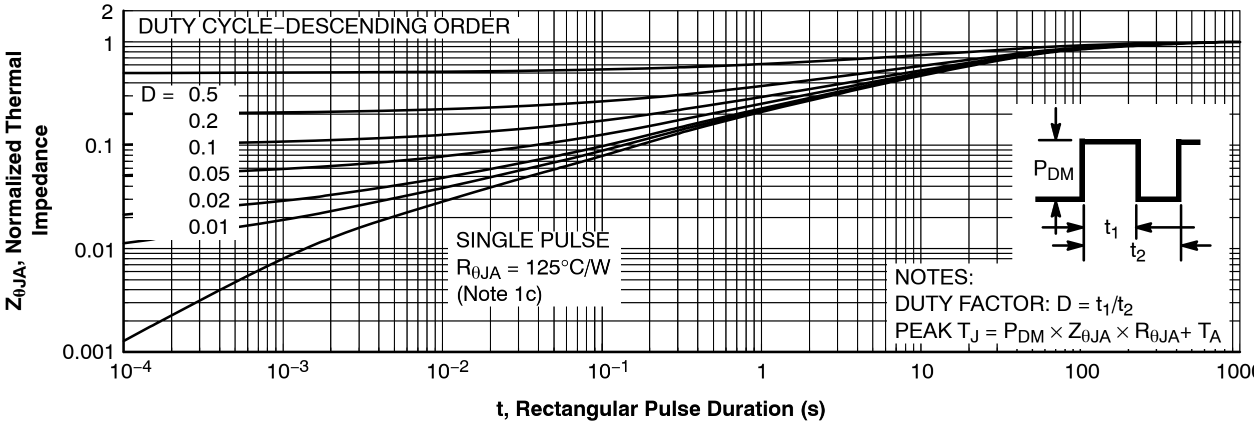


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N−Channel)

(T_J = 25°C unless otherwise noted)

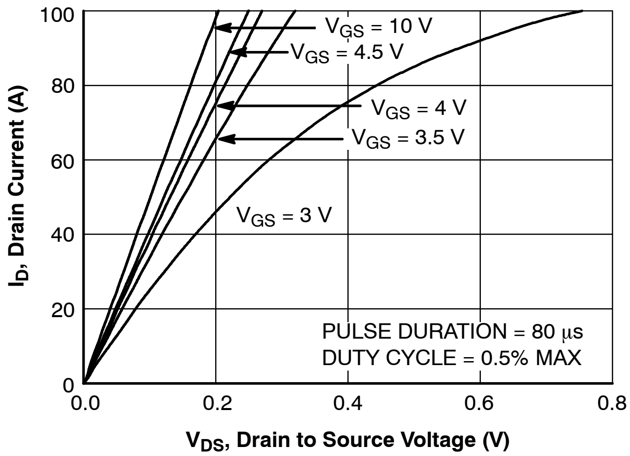


Figure 14. On Region Characteristics

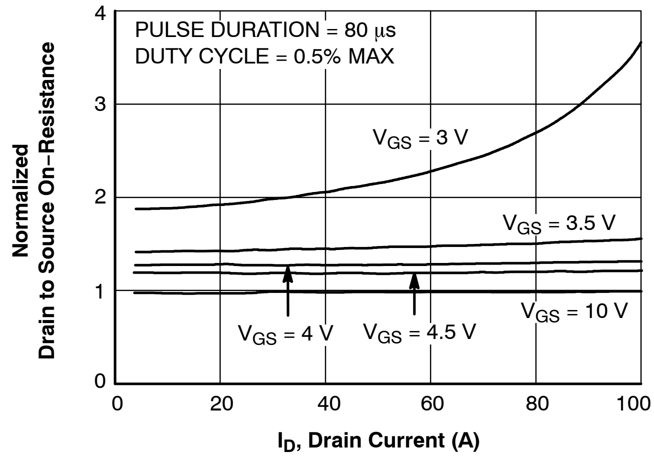


Figure 15. Normalized On−Resistance vs. Drain Current and Gate Voltage

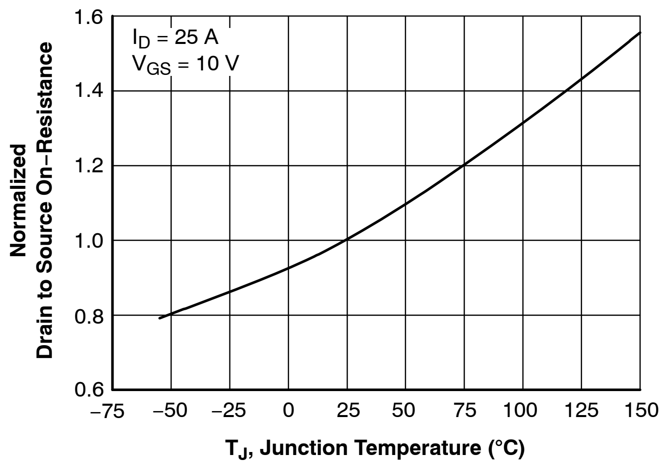


Figure 16. Normalized On−Resistance vs. Junction Temperature

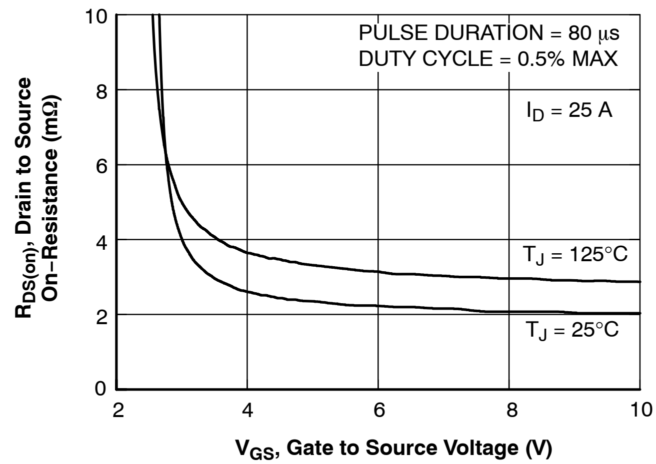


Figure 17. On−Resistance vs. Gate to Source Voltage

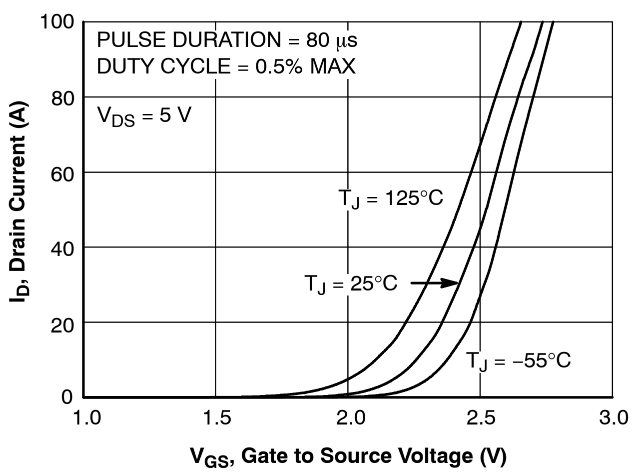


Figure 18. Transfer Characteristics

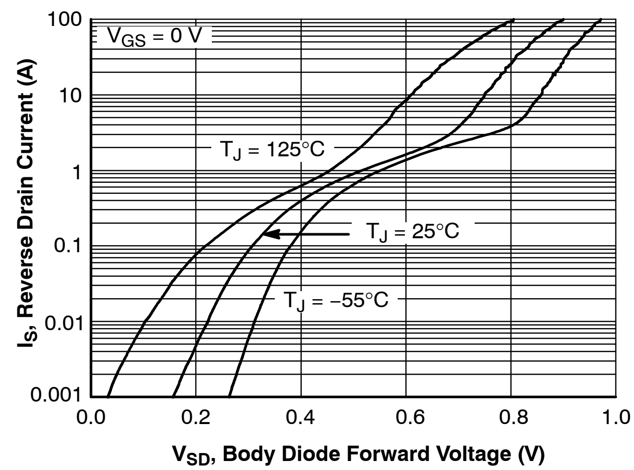


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2 N−Channel) (continued)

(T_J = 25°C unless otherwise noted)

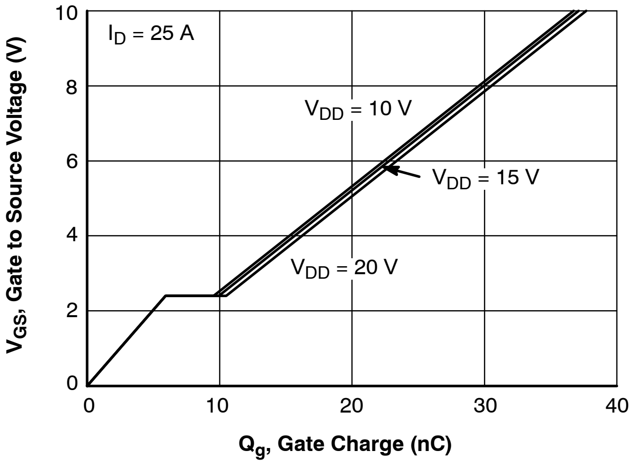


Figure 20. Gate Charge Characteristics

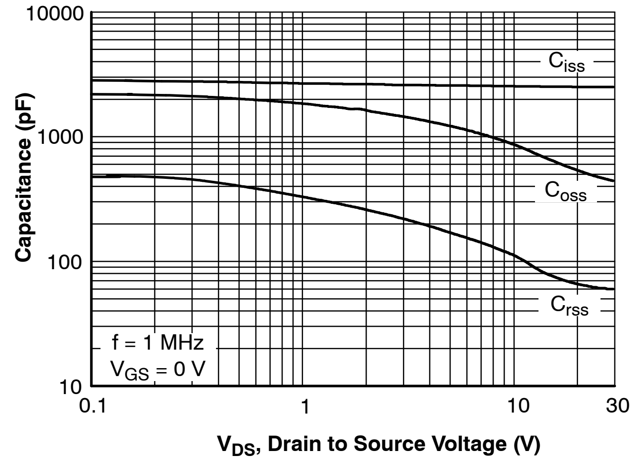


Figure 21. Capacitance vs. Drain to Source Voltage

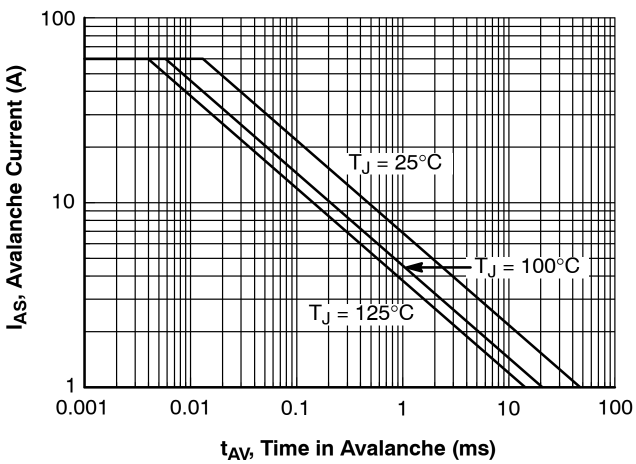


Figure 22. Unclamped Inductive Switching Capability

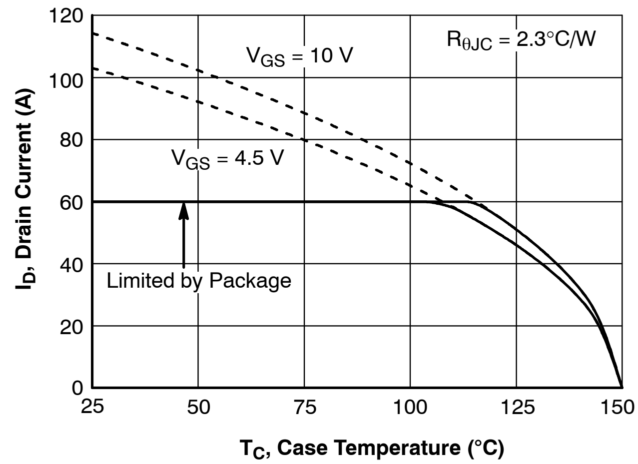


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

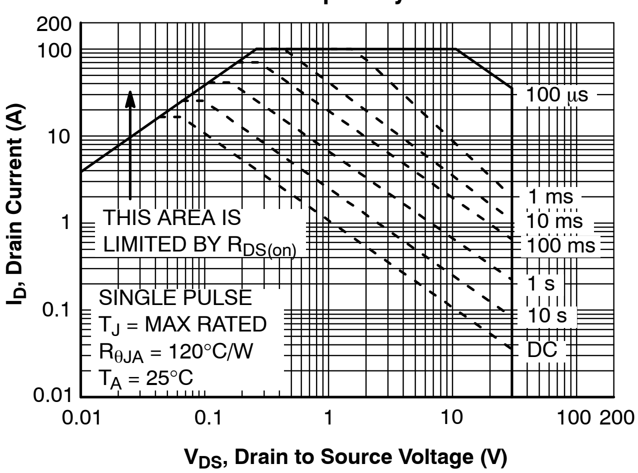


Figure 24. Forward Bias Safe Operating Area

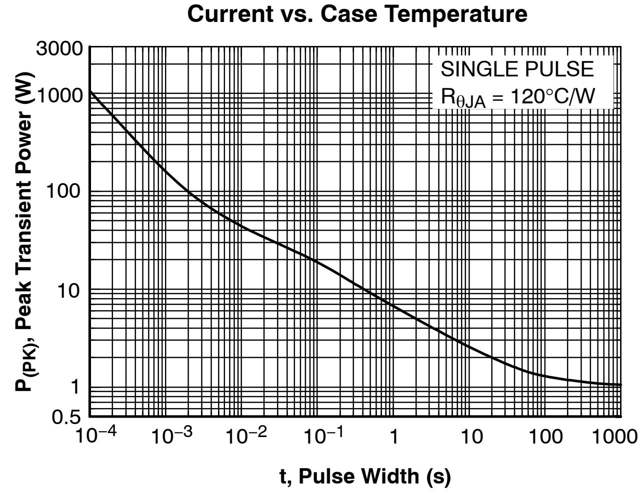


Figure 25. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q2 N−Channel) (continued)

(T_J = 25°C unless otherwise noted)

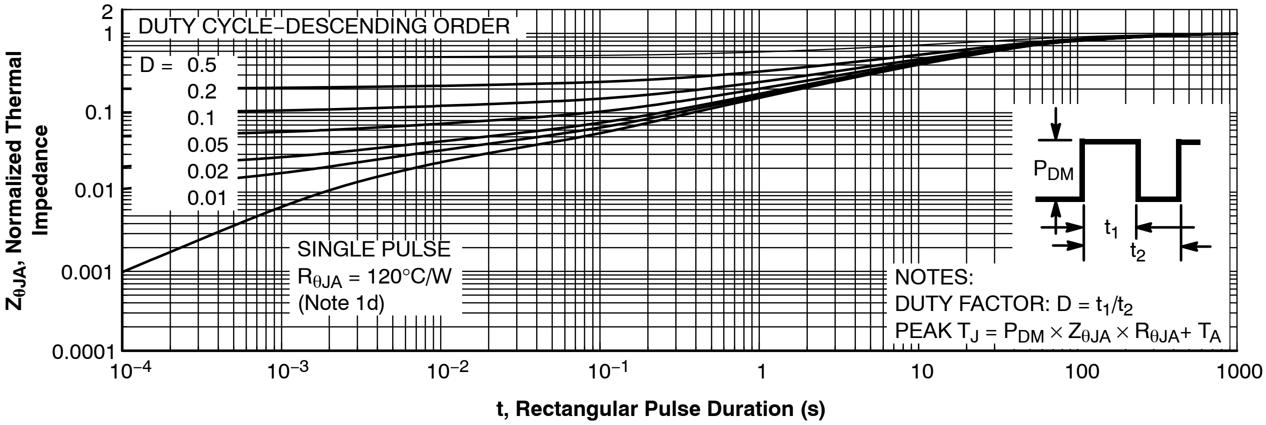


Figure 26. Junction−to−Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (continued)

SyncFET Schottky Body Diode Characteristics

onsemi's SyncFET process embeds a Schottky diode in parallel with POWERTRENCH MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMS3664S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

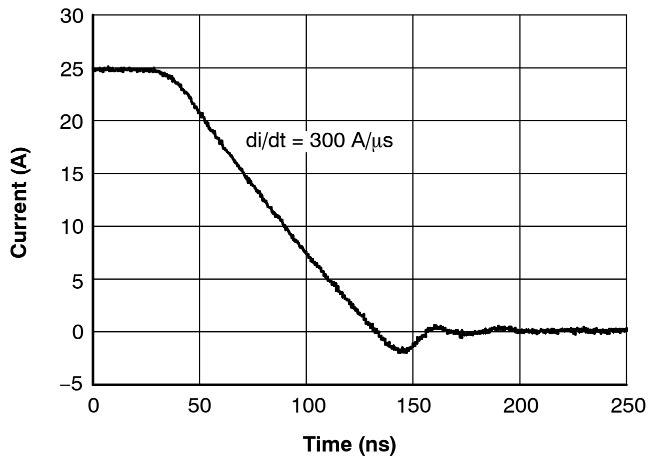


Figure 27. FDMS3664S SyncFET Body Diode Reverse Recovery Characteristic

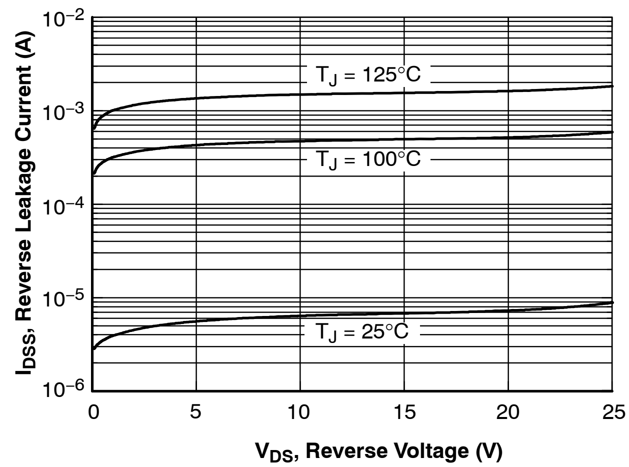
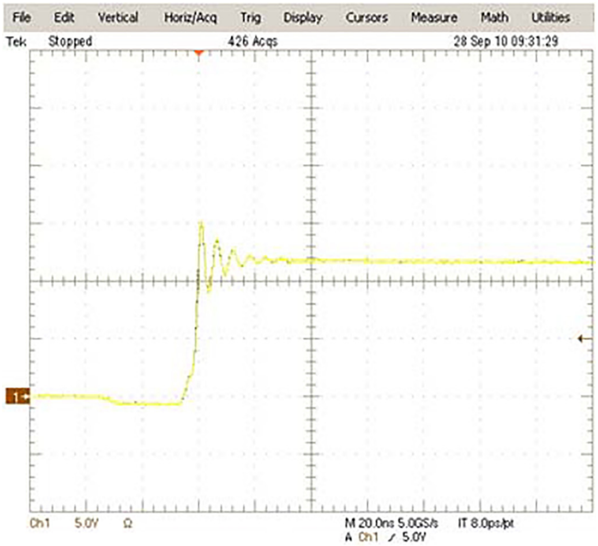


Figure 28. SyncFET Body Diode Reverse Leakage vs. Drain−Source Voltage

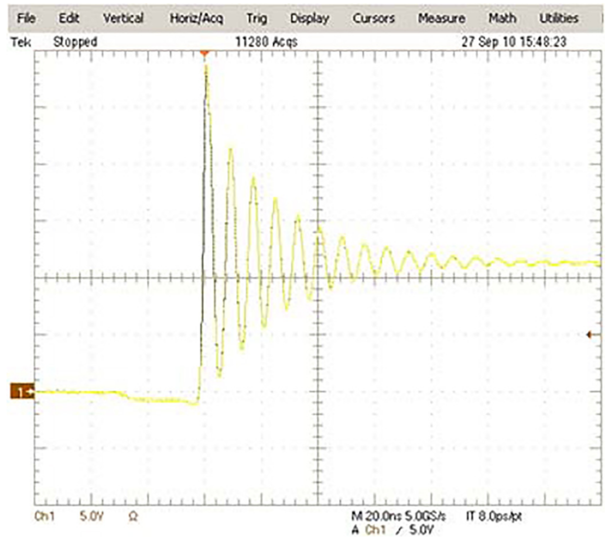
APPLICATIONS INFORMATION

Switch Node Ringing Suppression

onsemi's Power Stage products incorporate a proprietary design* that minimizes the peak overshoot, ringing voltage on the switch node (PHASE) without the need of any external snubbing components in a buck converter. As shown in the Figure 29, the Power Stage solution rings significantly less than competitor solutions under the same set of test conditions.



Power Stage Device



Competitors Solution

Figure 29. Power Stage Phase Node Rising Edge, High Side Turn On

* Patent Pending

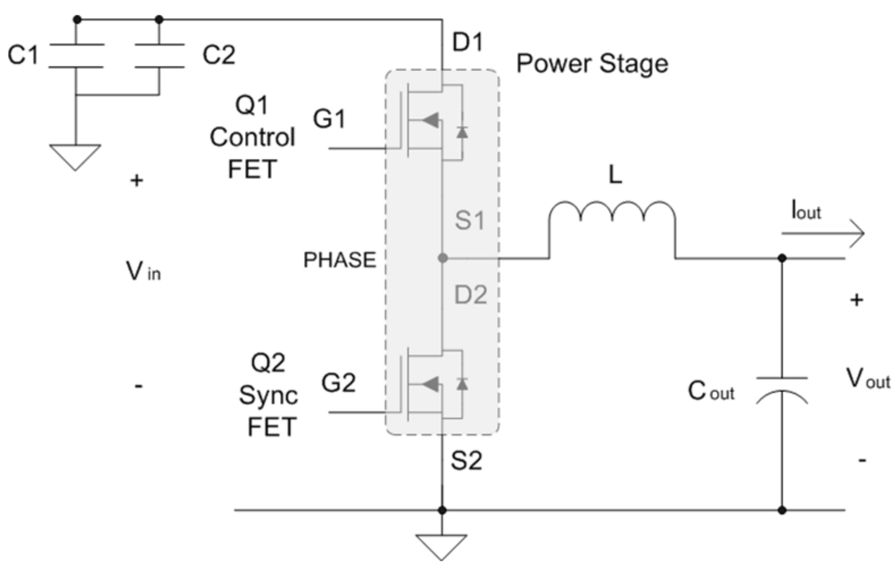
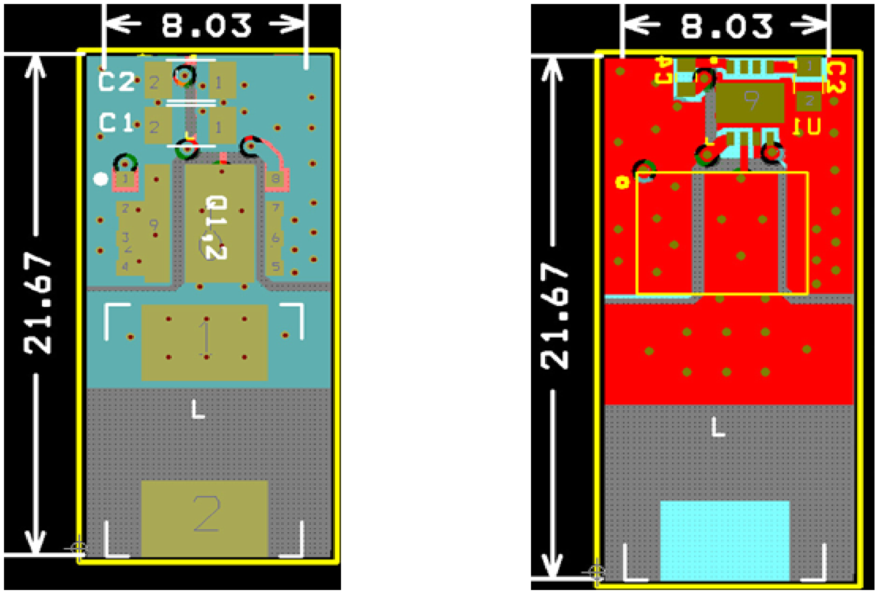


Figure 30. Shows the Power Stage in a Buck Converter Topology

Recommended PCB Layout Guidelines

As a PCB designer, it is necessary to address critical issues in layout to minimize losses and optimize the performance of the power train. Power Stage is a high power density solution and all high current flow paths, such as VIN (D1), PHASE (S1/D2) and GND (S2), should be short and wide for better and stable current flow, heat radiation and system performance. A recommended layout procedure is discussed below to maximize the electrical and thermal performance of the part.



Top Layer **Bottom Layer**

Figure 31. Recommended PCB Layout

Following is a guideline, not a requirement which the PCB designer should consider:

1. Input ceramic bypass capacitors C1 and C2 must be placed close to the D1 and S2 pins of Power Stage to help reduce parasitic inductance and high frequency conduction loss induced by switching operation. C1 and C2 show the bypass capacitors placed close to the part between D1 and S2. Input capacitors should be connected in parallel close to the part. Multiple input caps can be connected depending upon the application.

2. The PHASE copper trace serves two purposes; In addition to being the current path from the Power Stage package to the output inductor (L), it also serves as heat sink for the lower FET in the Power Stage package. The trace should be short and wide enough to present a low resistance path for the high current flow between the Power Stage and the inductor. This is done to minimize conduction losses and limit temperature rise. Please note that the PHASE node is a high voltage and high frequency switching node with high noise potential. Care should be taken to minimize coupling to adjacent traces. The reference layout in Figure 31 shows a good balance between the thermal and electrical performance of Power Stage.

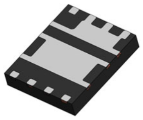
3. Output inductor location should be as close as possible to the Power Stage device for lower power loss due to copper trace resistance. A shorter and wider PHASE trace to the inductor reduces the conduction loss. Preferably the Power Stage should be directly in line (as shown in Figure 31) with the inductor for space savings and compactness.

4. The POWERTRENCH Technology MOSFETs used in the Power Stage are effective at minimizing phase node ringing. It allows the part to operate well within the breakdown voltage limits. This eliminates the need to have an external snubber circuit in most cases. If the designer chooses to use an RC snubber, it should be placed close to the part between the PHASE pad and S2 pins to dampen the high−frequency ringing.

5. The driver IC should be placed close to the Power Stage part with the shortest possible paths for the High Side gate and Low Side gates through a wide trace connection. This eliminates the effect of parasitic inductance and resistance between the driver and the MOSFET and turns the devices on and off as efficiently as possible. At higher−frequency operation this impedance can limit the gate current trying to charge the MOSFET input capacitance. This will result in slower rise and fall times and additional switching losses. Power Stage has both the gate pins on the same side of the package which allows for back mounting of the driver IC to the board. This provides a very compact path for the drive signals and improves efficiency of the part.

6. S2 pins should be connected to the GND plane with multiple vias for a low impedance grounding. Poor grounding can create a noise transient offset voltage level between S2 and driver ground. This could lead to faulty operation of the gate driver and MOSFET.

7. Use multiple vias on each copper area to interconnect top, inner and bottom layers to help smooth current flow and heat conduction. Vias should be relatively large, around 8 mils to 10 mils, and of reasonable inductance. Critical high frequency components such as ceramic bypass caps should be located close to the part and on the same side of the PCB. If not feasible, they should be connected from the backside via a network of low inductance vias.



PQFN8 5X6, 1.27P (SAWN TYPE)
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ISSUE A

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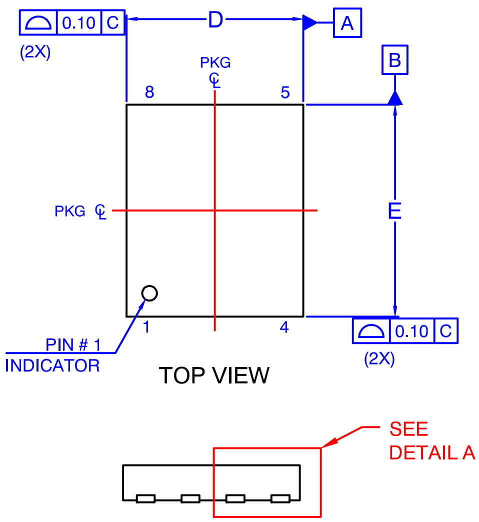
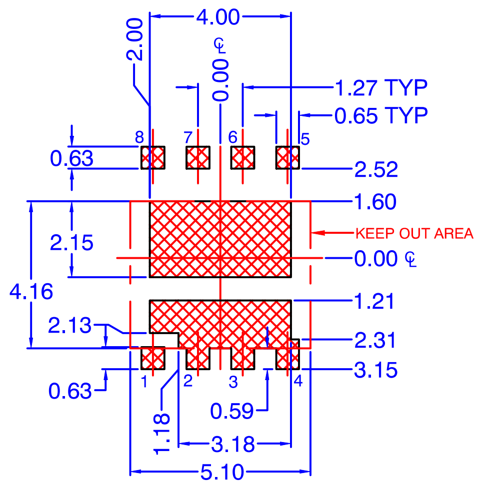
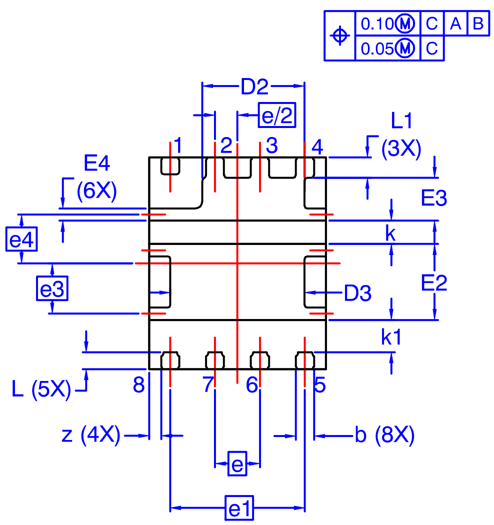




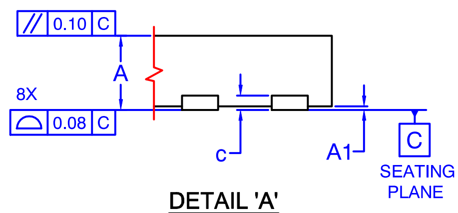
LAND PATTERN
RECOMMENDATION
FOR SAWN / PUNCHED TYPE

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.31	0.51	0.61
c	0.10	0.20	0.30
D	4.90	5.00	5.10
D2	2.80	2.90	3.16
D3	3.70	3.80	4.08
E	5.90	6.00	6.25
E2	2.05	2.15	2.25
E3	1.12	1.22	1.34
E4	0.25	0.35	0.45
e	1.27 BSC		
e1	3.81 BSC		
e/2	0.635 BSC		
e3	1.43 BSC		
e4	1.38 BSC		
k	0.61	0.66	0.71
k1	0.82	0.92	1.02
L	0.38	0.48	0.65
L1	0.48	0.58	0.68
z	0.34 REF		



BOTTOM VIEW
OPTION - A (SAWN TYPE)



DETAIL 'A'
(SCALE: 2X)

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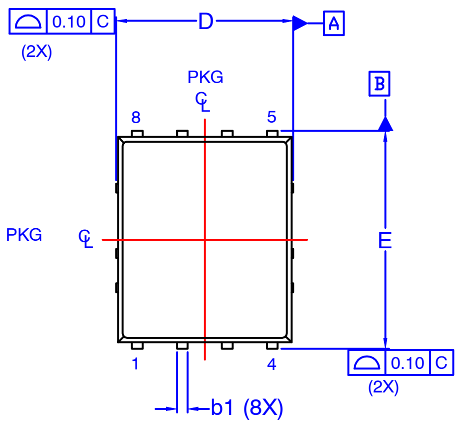
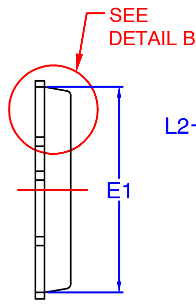
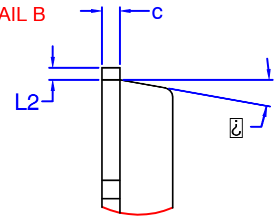
PQFN8 5X6, 1.27P (PUNCHED TYPE)
CASE 483AJ
ISSUE A

DATE 08 FEB 2021

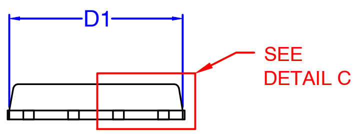


TOP VIEW

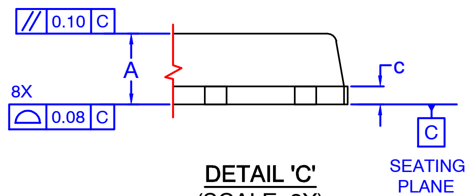




DETAIL 'B'
(SCALE: 2X)

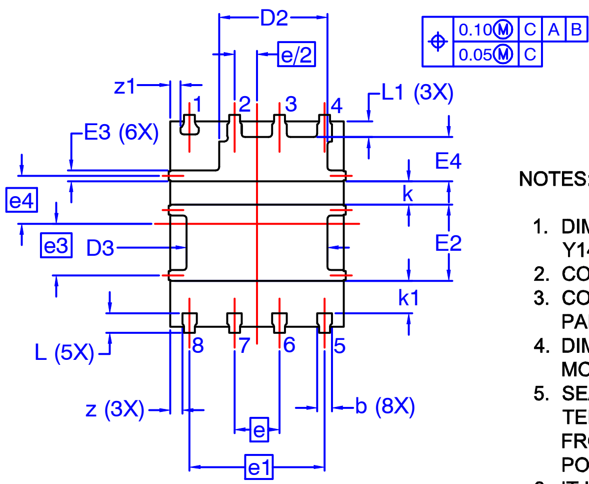


SIDE VIEW



DETAIL 'C'
(SCALE: 2X)

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.31	0.51	0.61
b1	0.21	0.31	0.41
c	0.15	0.25	0.35
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	2.80	3.06	3.16
D3	3.70	3.98	4.08
E	5.90	6.00	6.25
E1	5.70	5.80	5.90
E2	2.05	2.15	2.25
E3	0.25	0.33	0.45
E4	1.12	1.24	1.34
e	1.27 BSC		
e1	3.81 BSC		
e/2	0.635 BSC		
e3	1.45 BSC		
e4	1.36 BSC		
k	0.61	0.66	0.71
k1	0.82	0.92	1.02
L	0.38	0.55	0.65
L1	0.35	0.45	0.55
L2	0.08	0.18	0.28
z	0.34 REF		
z1	0.28 REF		
θ	0°	-	10°



BOTTOM VIEW

OPTION - B (PUNCHED TYPE)

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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