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FDP054N10

N-Channel PowerTrench® MOSFET

100 V, 144 A, 5.5 mΩ

Features

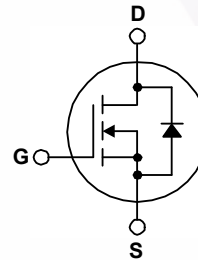
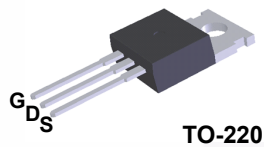
- $R_{DS(on)} = 4.6 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 75 \text{ A}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDP054N10	Unit
V_{DSS}	Drain to Source Voltage	100	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$, Silicon Limited)	144
		- Continuous ($T_C = 100^\circ\text{C}$, Silicon Limited)	102
		- Continuous ($T_C = 25^\circ\text{C}$, Package Limited)	120
I_{DM}	Drain Current	- Pulsed (Note 1)	576
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	1153
dv/dt	Peak Diode Avalanche Energy	(Note 3)	6
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	263
		- Derate Above 25°C	1.75
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDP054N10	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.57	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP054N10	FDP054N10	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}, T_C = 25^\circ\text{C}$	100	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.01	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μA
		$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, T_C = 150^\circ\text{C}$	-	-	500	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 75 \text{ A}$	-	4.6	5.5	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{GS} = 10 \text{ V}, I_D = 75 \text{ A}$	-	192	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	9985	13280	pF
C_{oss}	Output Capacitance		-	935	1245	pF
C_{rss}	Reverse Transfer Capacitance		-	390	585	pF
$Q_g(\text{tot})$	Total Gate Charge at 10V	$V_{DS} = 80 \text{ V}, I_D = 75 \text{ A}, V_{GS} = 10 \text{ V}$	-	156	203	nC
Q_{gs}	Gate to Source Gate Charge		-	53	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	48	-

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, I_D = 75 \text{ A}, V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	-	44	98	ns
t_r	Turn-On Rise Time		-	92	194	ns
$t_{d(off)}$	Turn-Off Delay Time		-	80	170	ns
t_f	Turn-Off Fall Time		(Note 4)	-	39	88

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	144	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	576	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 75 \text{ A}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{SD} = 75 \text{ A}, dI_F/dt = 100 \text{ A}/\mu\text{s}$	-	57	-	ns
Q_{rr}	Reverse Recovery Charge		-	121	-	nC

Notes:

- 1: Repetitive rating: pulse-width limited by maximum junction temperature.
- 2: $L = 0.41 \text{ mH}, I_{AS} = 75 \text{ A}, V_{DD} = 50 \text{ V}, R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
- 3: $I_{SD} \leq 75 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
- 4: Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

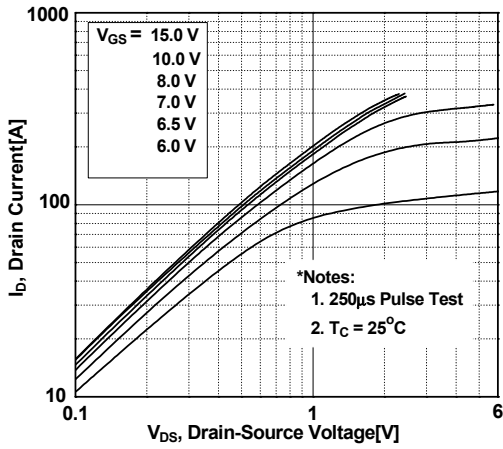


Figure 2. Transfer Characteristics

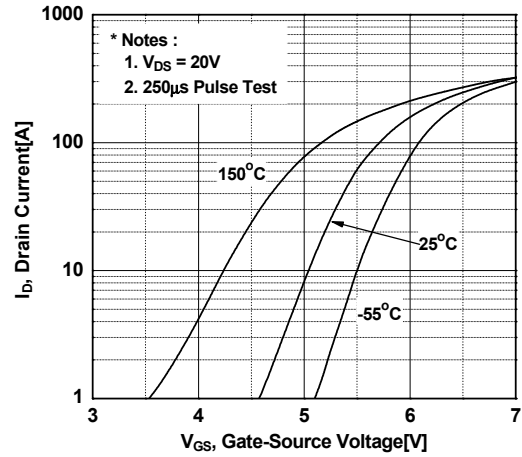


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

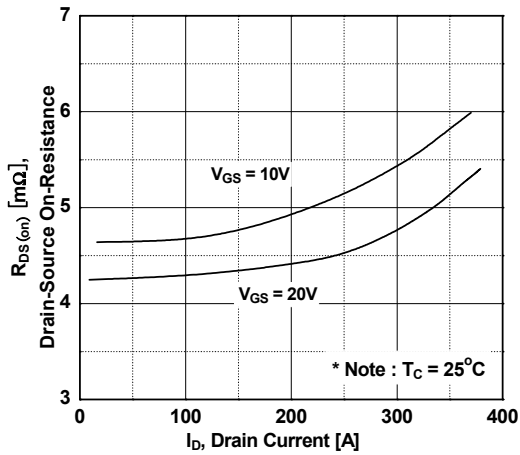


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

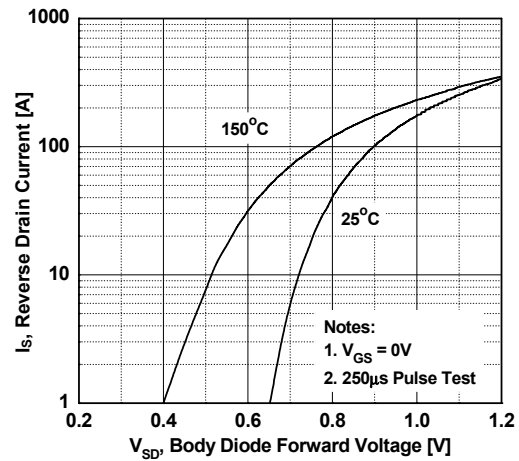


Figure 5. Capacitance Characteristics

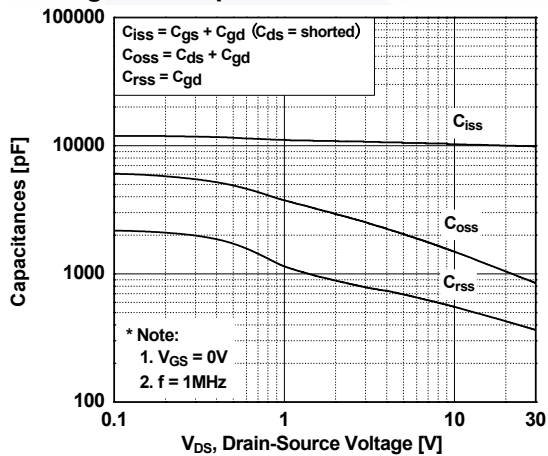
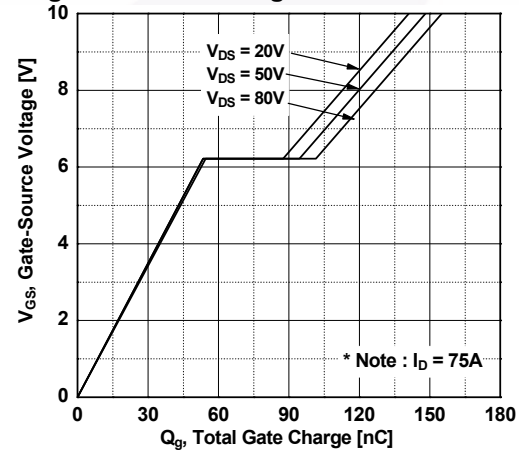


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

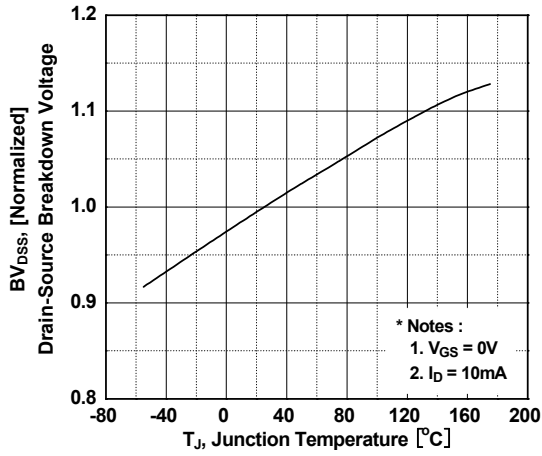


Figure 8. On-Resistance Variation vs. Temperature

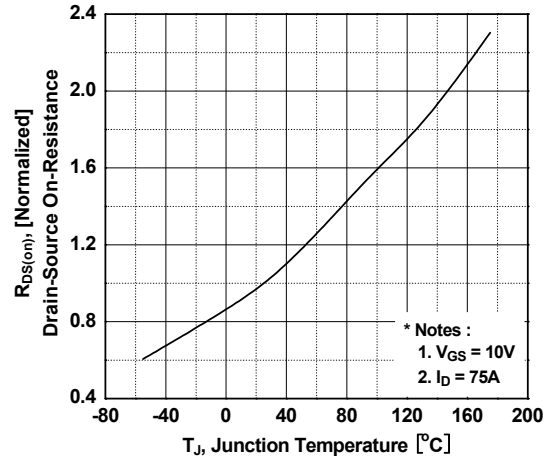


Figure 9. Maximum Safe Operating Area

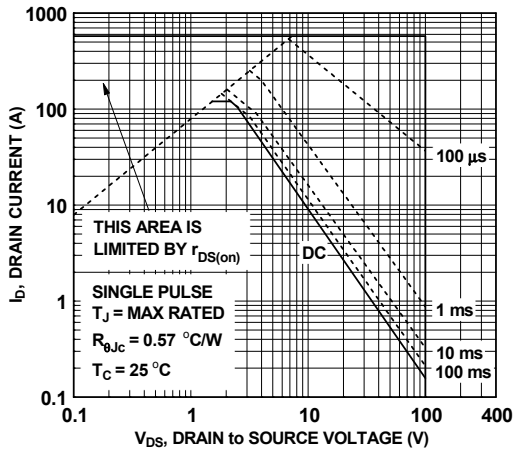


Figure 10. Maximum Drain Current vs. Case Temperature

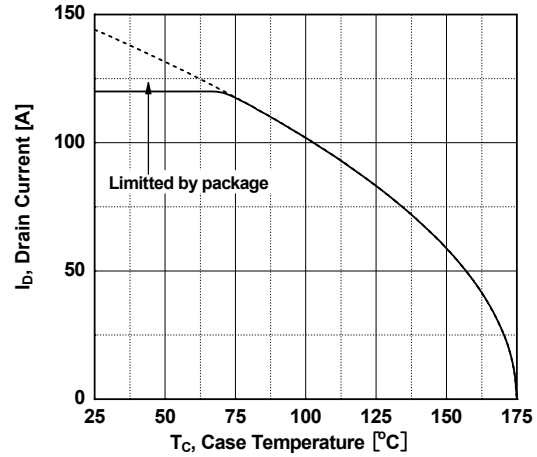


Figure 11. Transient Thermal Response Curve

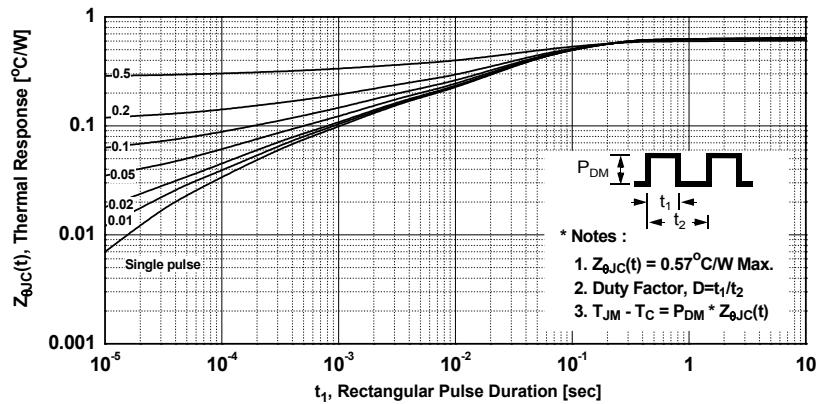




Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms

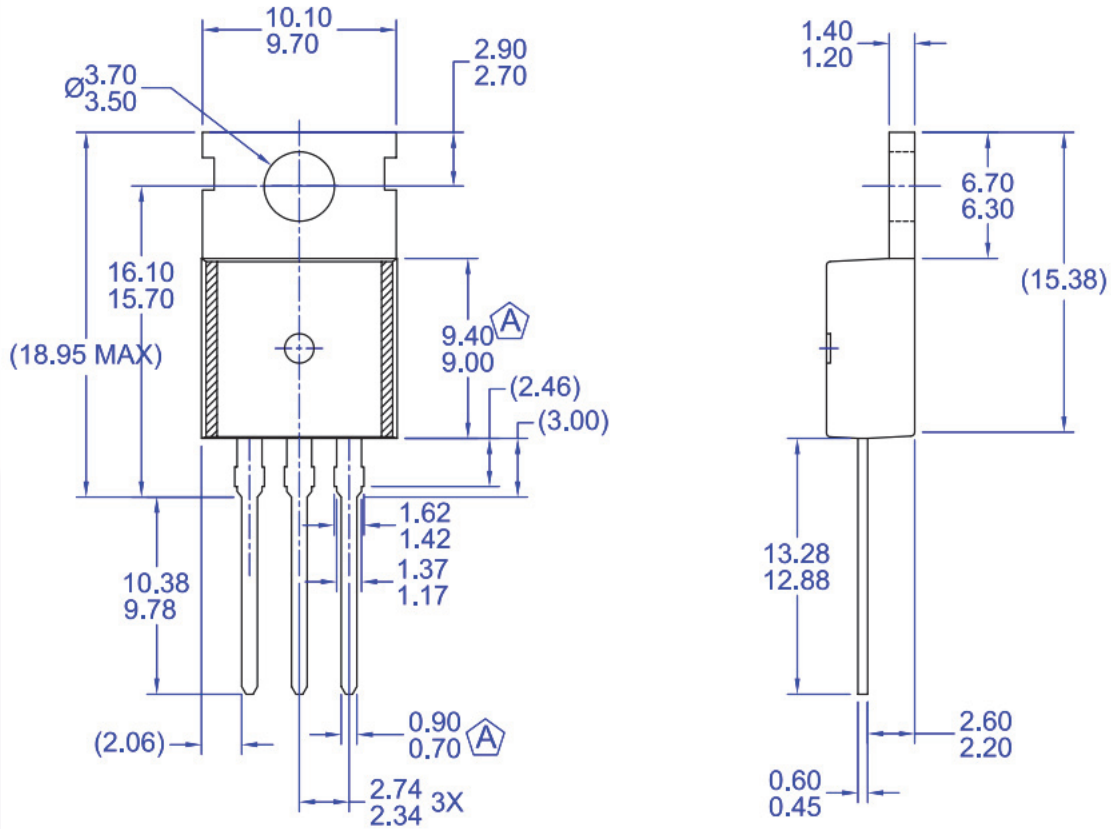


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES:

- A) CONFORMS TO JEDEC TO-220 VARIATION AB EXCEPT WHERE NOTED
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

Figure 16. TO220, Molded, 3-Lead, Non Jedec Variation AB

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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