onsemi

MOSFET – N-Channel, POWERTRENCH[®]

V _{DSS}	R _{DS(on)} MAX	I _D MAX				
100 V	15.0 m Ω @ 10 V	50 A				

100 V, 50 A, 15 m Ω

FDP150N10A

Description

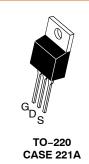
This N-Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Features

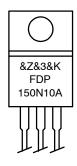
- $R_{DS(on)} = 12.5 \text{ m}\Omega \text{ (Typ.)} @ V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$
- Fast Switching Speed
- Low Gate Charge, $Q_G = 16.2 \text{ nC}$ (Typ.)
- High Performance Trench Technology for Extremely Low RDS(on)
- High Power and Current Handling Capability
- RoHS Compliant

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter



MARKING DIAGRAM

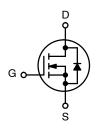


 &Z
 = Assembly Plant Code

 &3
 = 3-Digit Date Code Format

 &K
 = 2-Digits Lot Run Traceability Code

 FDP150N10A
 = Device Code



N-Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25° C unless otherwise noted)

Symbol	Parameter	FDP150N10A_F102	Unit		
V _{DSS}	Drain to Source Voltage	100	V		
V _{GSS}	Gate to Source Voltage	±20	V		
I _D	Drain Current	Drain Current – Continuous (T _C = 25° C)		А	
		– Continuous (T _C = 100°C)	36		
I _{DM}	Drain Current	– Pulsed (Note 1)			
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	84.6	mJ		
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns		
PD	Power Dissipation $(T_C = 25^{\circ}C)$		91	W	
		- Derate Above 25°C	0.61	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range	–55 to +175	°C		
ΤL	Maximum Lead Temperature for Soldering, 1/8" from Cas	300	°C		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. Repetitive rating: pulse-width limited by maximum junction temperature. 2. L = 2 mH, I_{AS} = 9.2 A, R_G = 25 Ω , starting T_J = 25°C. 3. I_{SD} ≤ 100 A, di/dt ≤ 200 A/µs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP150N10A_F102	Unit
R_{\thetaJC}	Thermal Resistance, Junction to Case, Max.	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
OFF CHARA	ACTERISTICS	-			•	
BV _{DSS}	Drain to Source Breakdown Voltage $I_D = 250 \ \mu$ A, $V_{GS} = 0 \ V$			-	-	V
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta \text{T}_{\text{J}}}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C	-	0.08	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μΑ
		$V_{DS} = 80 \text{ V}, \text{ T}_{C} = 150^{\circ}\text{C}$	-	-	500	
I _{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±100	nA
ON CHARAG	CTERISTICS					
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \ \mu A$	2.0	-	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 50 \text{ A}$	-	12.5	15.0	mΩ
9 _{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 50 \text{ A}$	-	40	-	S
DYNAMIC C	HARACTERISTICS	-			•	
C _{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$	-	1080	1440	pF
C _{oss}	Output Capacitance		-	267	355	pF
C _{rss}	Reverse Transfer Capacitance		-	11	-	pF
C _{oss(er)}	Energy Related Output Capacitance	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	436	-	pF
Q _{g(tot)}	Total Gate Charge at 10 V	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 50 \text{ A},$	-	16.2	21.0	nC
Q _{gs}	Gate to Source Gate Charge	(Note 4)	-	5.3	-	nC
Q _{gs2}	Gate Charge Threshold to Plateau		-	2.6	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	3.7	-	nC
ESR	Equivalent Series Resistance (G-S)	f = 1 MHz	-	1.3	-	Ω
SWITCHING	CHARACTERISTICS			-	•	
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, \text{ I}_{D} = 50 \text{ A}, \text{ V}_{GS} = 10 \text{ V},$	-	13	36	ns
t _r	Turn–On Rise Time	- R _G = 4.7 Ω (Note 4)	-	16	42	ns
t _{d(off)}	Turn-Off Delay Time		-	21	52	ns
t _f	Turn–Off Fall Time		-	5	20	ns
DRAIN-SOU	IRCE DIODE CHARACTERISTICS		•	•		
۱ _S	Maximum Continuous Drain to Source Diode Forward Current			-	50	А
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current			-	200	А
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 50 A	-	-	1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, V _{DD} = 50 V, I _{SD} = 50 A,	-	50	-	ns
Q _{rr}	Reverse Recovery Charge	dl _F /dt = 100 A/μs	_	55	_	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

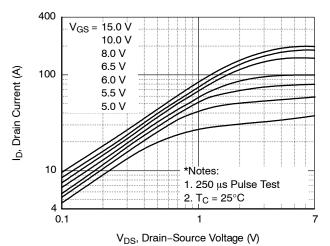


Figure 1. On-Region Characteristics

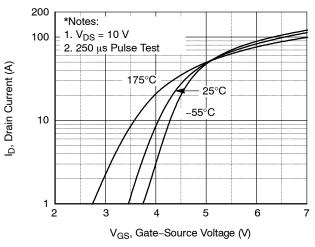


Figure 2. Transfer Characteristics

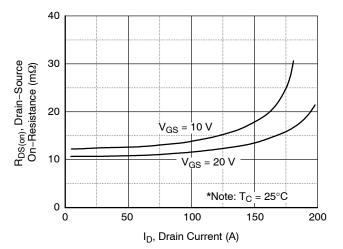


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

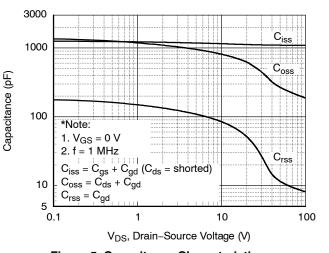


Figure 5. Capacitance Characteristics

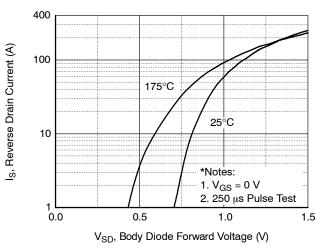


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

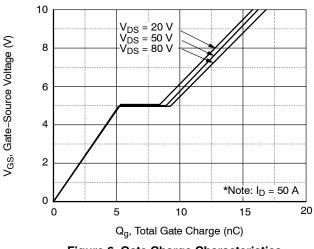
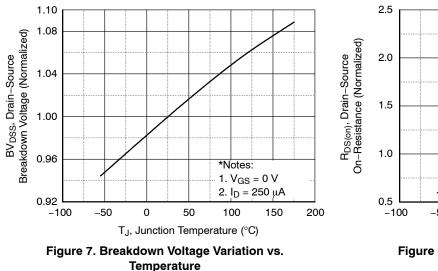
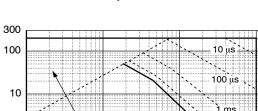


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)





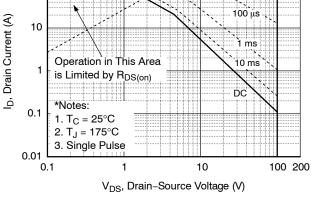
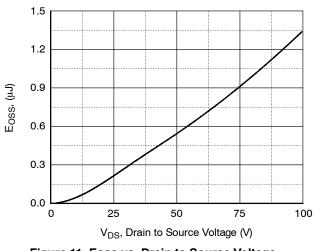


Figure 9. Maximum Safe Operating Area





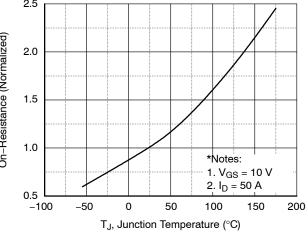


Figure 8. On-Resistance Variation vs. Temperature

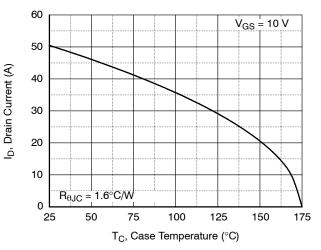
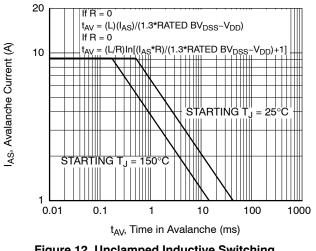
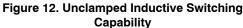


Figure 10. Maximum Drain Current vs. Case Temperature





TYPICAL PERFORMANCE CHARACTERISTICS (continued)

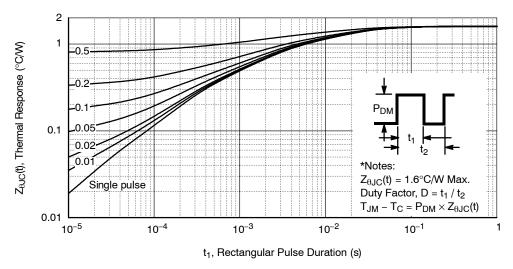


Figure 13. Transient Thermal Response Curve

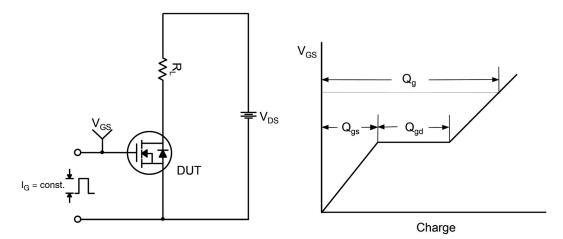


Figure 14. Gate Charge Test Circuit & Waveform

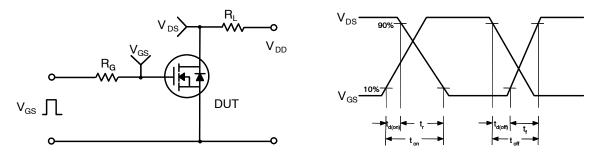


Figure 15. Resistive Switching Test Circuit & Waveforms

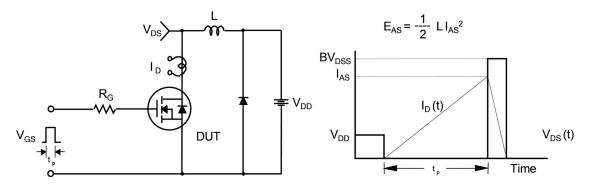


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

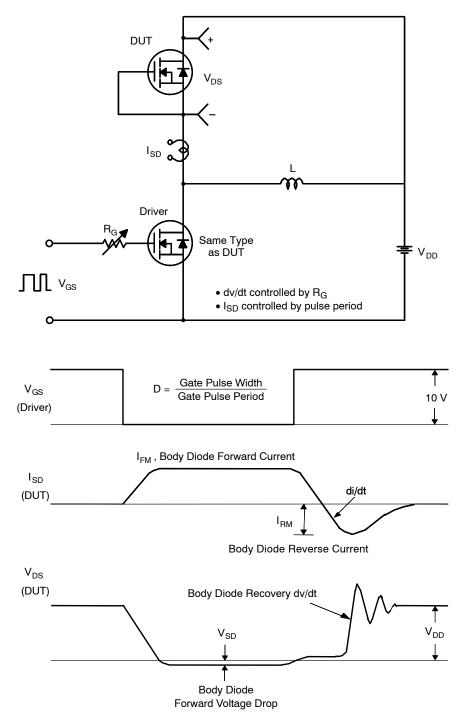


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

ORDERING INFORMATION

Part Number	Part Number Device Marking		Reel Size	Tape Width	Shipping	
FDP150N10A-F102	FDP150N10A	TO-220	N/A	N/A	800 Units / Tube	

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A A				INC	1	MILLIM		
	Ŭ		DIM	MIN.	MAX.	MIN.	MAX.	
1 2 3			A	0.570	0.620	14.48	15.75	
			B	0.380	0.415	9.66	10.53	
<u>╄</u> <u></u>			C D	0.160	0.190	4.07	4.83	
			F	0.025	0.038	0.64 3.60	0.96 4.09	
Z-J K			G	0.095	0.101	2.42	2.66	
			н	0.110	0.161	2.42	4.10	
				0.014	0.024	0.36	0.61	
			ĸ	0.500	0.562	12.70	14.27	
∨4	R —		L	0.045	0.060	1.15	1.52	
G	J → →		N	0.190	0.210	4.83	5.33	
_ → → D			Q	0.100	0.120	2.54	3.04	
N			R	0.080	0.110	2.04	2.79	
			s	0.045	0.055	1.15	1.41	
			т	0.235	0.255	5.97	6.47	
			U	0.000	0.050	0.00	1.27	
			V	0.045		1.15		
			Z		0.080		2.04	
STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. BASE 2. EMITTER 3. COLLECTOR 4. EMITTER	3. 0	CATHODI NODE GATE NODE		2. MA 3. GA	in terminal In terminal Te In terminal	.2	
STYLE 5: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 6: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE	3. 0	Cathodi Node Cathodi Node	E	STYLE 8: PIN 1. CA 2. AN 3. EX 4. AN	ode Ternal Trip	/DELAY	
STYLE 9: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 10: PIN 1. GATE 2. SOURCE 3. DRAIN 4. SOURCE	3. 0	OURCE		2. MA 3. GA	NIN TERMINAL NIN TERMINAL TE DT CONNECTI	.2	

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