

MOSFET – Dual, N-Channel, POWERTRENCH[®], Power Clip, Asymmetric 25 V

FDPC8014AS

General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

Features

- Q1: N-Channel
 - ◆ Max $r_{DS(on)}$ = 3.8 mΩ at $V_{GS} = 10$ V, $I_D = 20$ A
 - ◆ Max $r_{DS(on)}$ = 4.7 mΩ at $V_{GS} = 4.5$ V, $I_D = 18$ A
- Q2: N-Channel
 - ◆ Max $r_{DS(on)}$ = 1.0 mΩ at $V_{GS} = 10$ V, $I_D = 40$ A
 - ◆ Max $r_{DS(on)}$ = 1.2 mΩ at $V_{GS} = 4.5$ V, $I_D = 37$ A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Computing
- Communications
- General Purpose Point of Load

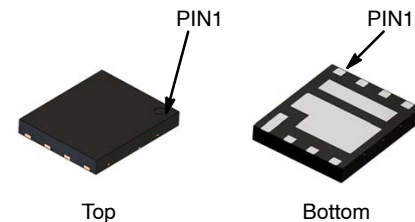
PIN DESCRIPTION

Pin	Name	Description
1	HSG	High Side Gate
2	GR	Gate Return
3, 4, 9	V+ (HSD)	High Side Drain
5, 6, 7	SW	Switching Node, Low Side Drain
8	LSG	Low Side Gate
10	GND (LSS)	Low Side Source



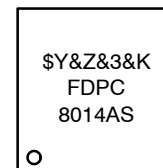
ON Semiconductor[®]

www.onsemi.com

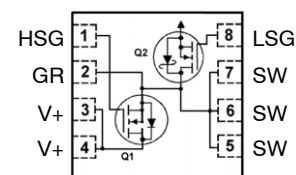
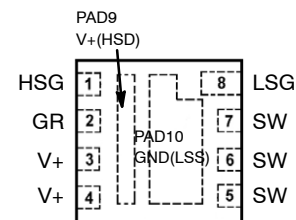


Power Clip 5x6
PDFN8 5x6, 1.27P,
CASE 483AR

MARKING DIAGRAM



FDPC8014AS = Specific Device Code
 \$Y = ON semiconductor Logo
 &Z = Assembly Plant Code
 &3 = 3-Digit Date Code
 &K = 2-Digits Lot Run Traceability Code



N-Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

FDPC8014AS

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

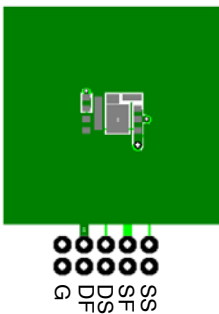
Symbol	Parameter		Q1	Q2	Unit	
V_{DS}	Drain to Source Voltage		25 (Note 4)	25	V	
V_{GS}	Gate to Source Voltage		± 12	± 12	V	
I_D	Drain Current	-Continuous	$T_C = 25^\circ\text{C}$ (Note 5)	59	159	A
		-Continuous	$T_C = 100^\circ\text{C}$ (Note 5)	37	100	
	-Continuous	$T_A = 25^\circ\text{C}$	20 (Note 1a)	40 (Note 1b)		
	-Pulsed	(Note 3)	266	1116		
E_{AS}	Single Pulse Avalanche Energy		(Note 2)	73	294	mJ
P_D	Power Dissipation for Single Operation		$T_C = 25^\circ\text{C}$	21	37	W
	Power Dissipation for Single Operation		$T_A = 25^\circ\text{C}$	2.1 (Note 1a)	2.3 (Note 1b)	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

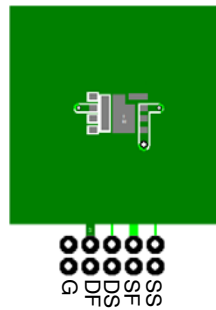
THERMAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.0	3.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	60 (Note 1a)	55 (Note 1b)	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	130 (Note 1c)	120 (Note 1d)	

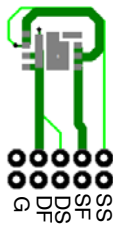
- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



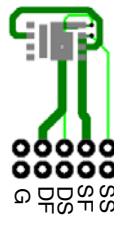
a. $60^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. $55^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



c. $130^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper



d. $120^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

- Q1: E_{AS} of 73 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3$ mH, $I_{AS} = 7$ A, $V_{DD} = 30$ V, $V_{GS} = 10$ V. 100% test at $L = 0.1$ mH, $I_{AS} = 24$ A.
- Q2: E_{AS} of 294 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3$ mH, $I_{AS} = 14$ A, $V_{DD} = 25$ V, $V_{GS} = 10$ V. 100% test at $L = 0.1$ mH, $I_{AS} = 46$ A.
- Pulsed I_D please refer to Figure 11 and Figure 24 SOA graph for more details.
- The continuous V_{DS} rating is 25 V; However, a pulse of 30 V peak voltage for no longer than 100 ns duration at 600 kHz frequency can be applied.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V I _D = 1 mA, V _{GS} = 0 V	Q1 Q2	25 25	– –	– –	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C I _D = 10 mA, referenced to 25°C	Q1 Q2	– –	24 25	– –	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 20 V, V _{GS} = 0 V V _{DS} = 20 V, V _{GS} = 0 V	Q1 Q2	– –	– –	1 500	μA μA
I _{GSS}	Gate to Source Leakage Current, Forward	V _{GS} = 12 V / –8 V, V _{DS} = 0 V V _{GS} = 12 V / –8 V, V _{DS} = 0 V	Q1 Q2	– –	– –	±100 ±100	nA nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA V _{GS} = V _{DS} , I _D = 1 mA	Q1 Q2	0.8 1.0	1.3 1.5	2.5 3.0	V
ΔV _{GS(th)} / ΔT _J	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C I _D = 10 mA, referenced to 25°C	Q1 Q2	– –	–4 –3	– –	mV/°C
r _{DS(on)}	Drain to Source On Resistance	V _{GS} = 10 V, I _D = 20 A V _{GS} = 4.5 V, I _D = 18 A V _{GS} = 10 V, I _D = 20 A, T _J = 125°C	Q1	– – –	2.9 3.6 3.9	3.8 4.7 5.3	mΩ
		V _{GS} = 10 V, I _D = 40 A V _{GS} = 4.5 V, I _D = 37 A V _{GS} = 10 V, I _D = 40 A, T _J = 125°C	Q2	– – –	0.75 0.9 1.0	1.0 1.2 1.5	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 20 A V _{DS} = 5 V, I _D = 40 A	Q1 Q2	– –	182 296	– –	S

DYNAMIC CHARACTERISTICS

C _{ISS}	Input Capacitance	Q1: V _{DS} = 13 V, V _{GS} = 0 V, f = 1 MHz Q2: V _{DS} = 13 V, V _{GS} = 0 V, f = 1 MHz	Q1 Q2	– –	1695 6985	2375 9780	pF
C _{OSS}	Output Capacitance		Q1 Q2	– –	495 2170	710 3040	pF
C _{RSS}	Reverse Transfer Capacitance		Q1 Q2	– –	54 172	100 245	pF
R _g	Gate Resistance		Q1 Q2	0.1 0.1	0.4 0.4	1.2 1.2	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	Q1: V _{DD} = 13 V, I _D = 20 A, R _{GEN} = 6 Ω Q2: V _{DD} = 13 V, I _D = 40 A, R _{GEN} = 6 Ω	Q1 Q2	– –	8 16	16 29	ns
t _r	Rise Time		Q1 Q2	– –	2 6	10 12	ns
t _{d(off)}	Turn-Off Delay Time		Q1 Q2	– –	24 48	38 76	ns
t _f	Fall Time		Q1 Q2	– –	2 5	10 10	ns
Q _g	Total Gate Charge		V _{GS} = 0 V to 10 V Q1: V _{DD} = 13 V, I _D = 20 A Q2: V _{DD} = 13 V, I _D = 40 A	Q1 Q2	– –	25 97	35 135
Q _g	Total Gate Charge	V _{GS} = 0 V to 4.5 V Q1: V _{DD} = 13 V, I _D = 20 A Q2: V _{DD} = 13 V, I _D = 40 A	Q1 Q2	– –	11 44	16 62	nC
Q _{gs}	Gate to Source Gate Charge	Q1: V _{DD} = 13 V, I _D = 20 A Q2: V _{DD} = 13 V, I _D = 40 A	Q1 Q2	– –	3.4 14	– –	nC
Q _{gd}	Gate to Drain "Miller" Charge		Q1 Q2	– –	2.2 9	– –	nC

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 20\text{ A}$ (Note 6) $V_{GS} = 0\text{ V}, I_S = 40\text{ A}$ (Note 6)	Q1 Q2	- -	0.8 0.8	1.2 1.2	V
I_S	Diode Continuous Forward Current	$T_C = 25^\circ\text{C}$	Q1 Q2	- -	59 159	- -	A
$I_{S,Pulse}$	Diode Pulse Current		Q1 Q2	- -	266 1116	- -	A
t_{rr}	Reverse Recovery Time	Q1: $I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ Q2: $I_F = 40\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$	Q1 Q2	- -	25 44	40 70	ns
Q_{rr}	Reverse Recovery Charge		Q1 Q2	- -	10 78	20 125	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

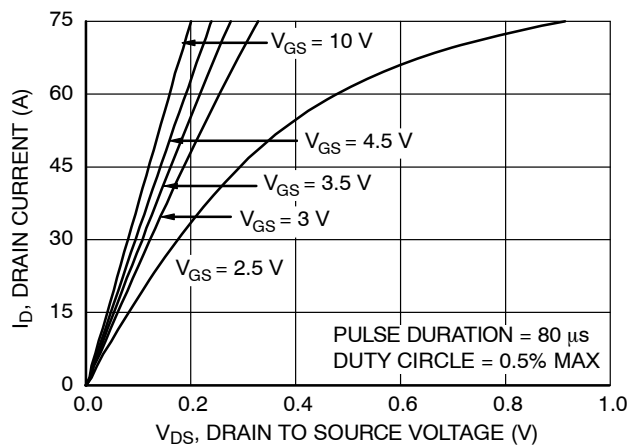


Figure 1. On Region Characteristics

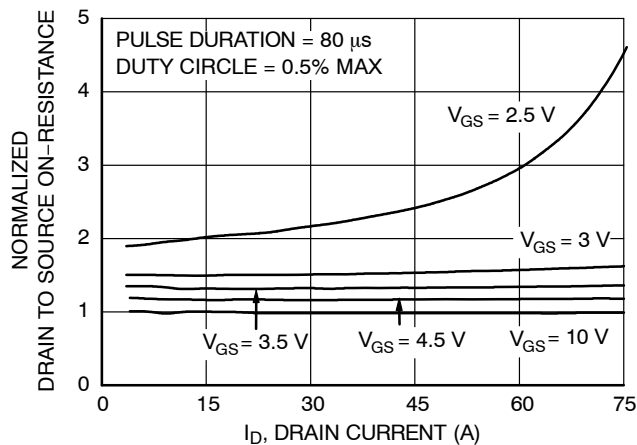


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

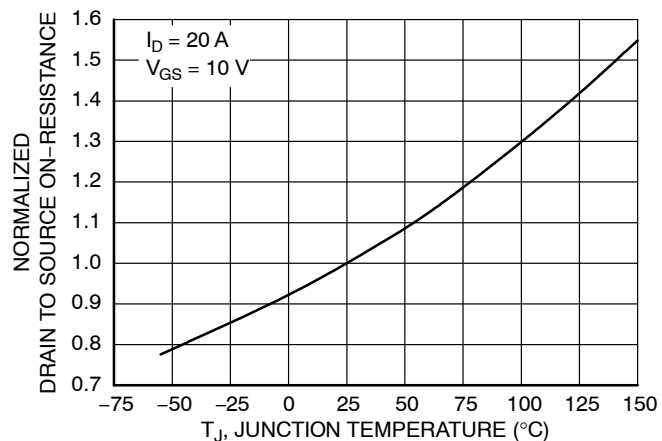


Figure 3. Normalized On Resistance vs. Junction Temperature

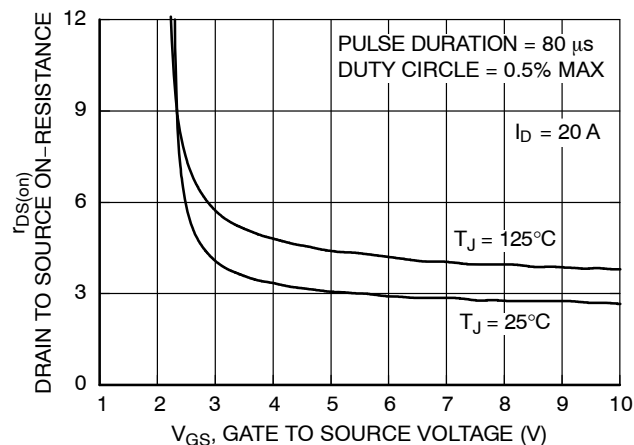


Figure 4. On-Resistance vs. Gate to Source Voltage

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TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

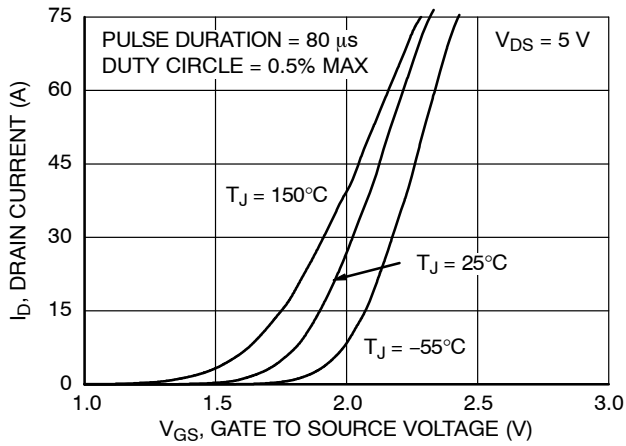


Figure 5. Transfer Characteristics

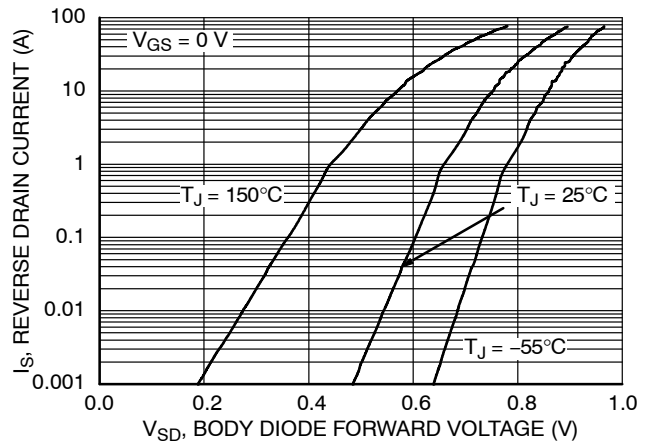


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

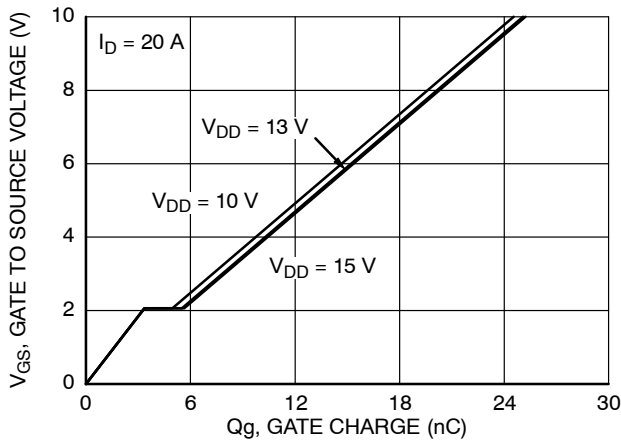


Figure 7. Gate Charge Characteristics

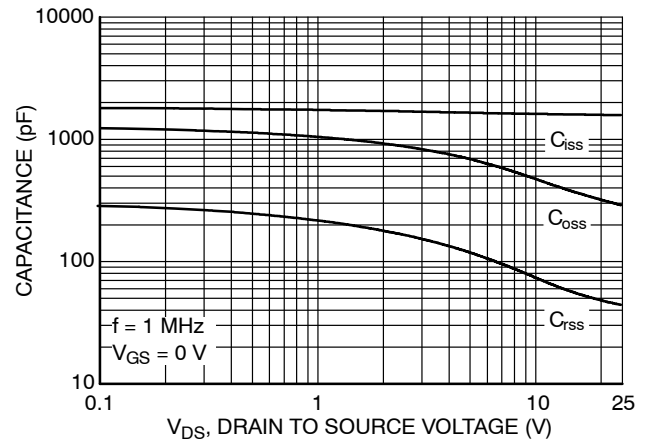


Figure 8. Capacitance vs. Drain to Source Voltage

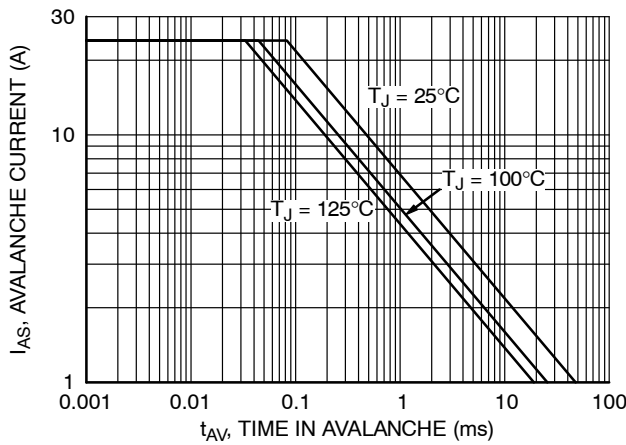


Figure 9. Unclamped Inductive Switching Capability

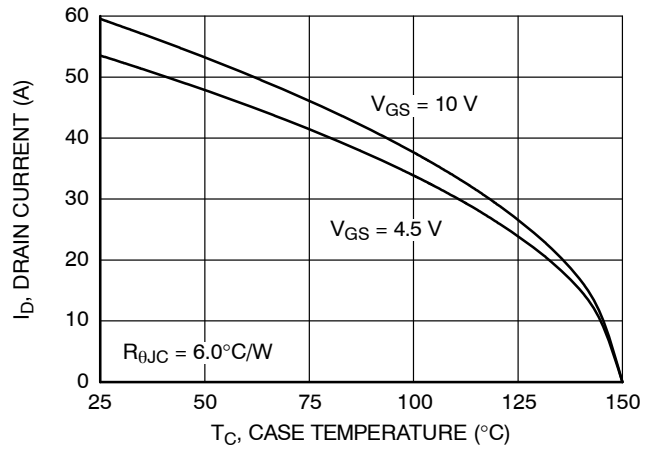


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

FDPC8014AS

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

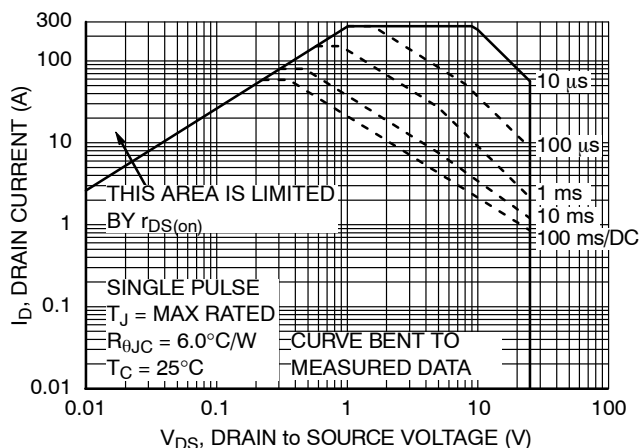


Figure 11. Forward Bias Safe Operating Area

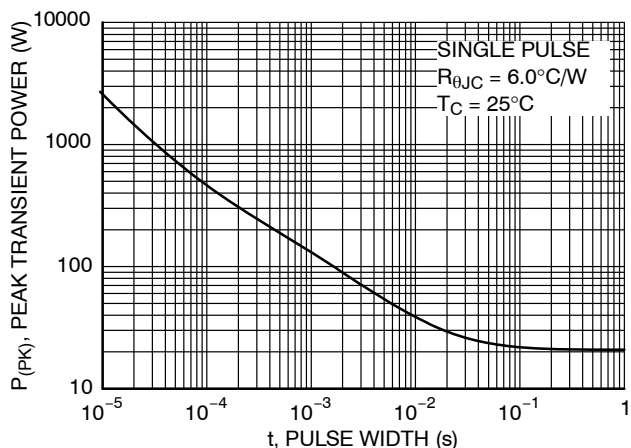


Figure 12. Single Pulse Maximum Power Dissipation

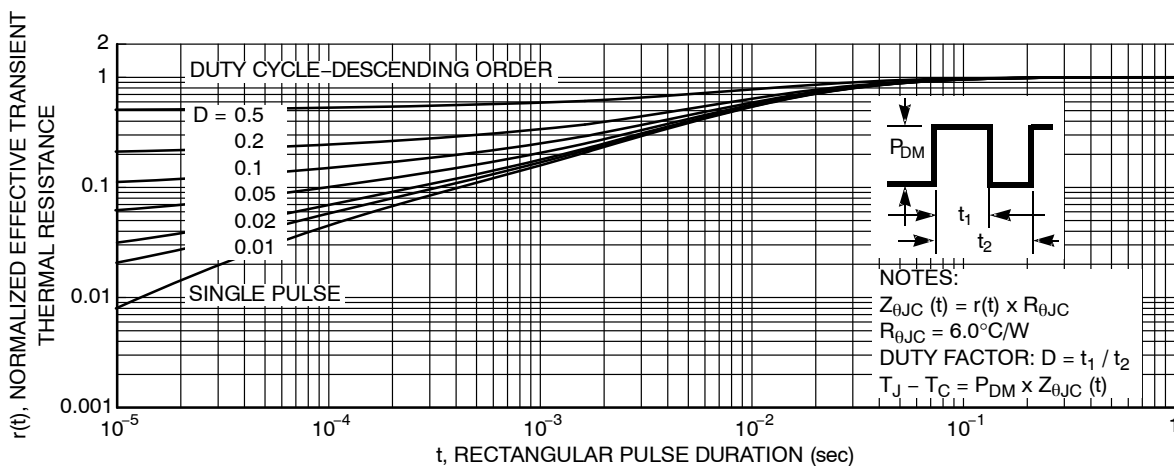


Figure 13. Junction-to-Case Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

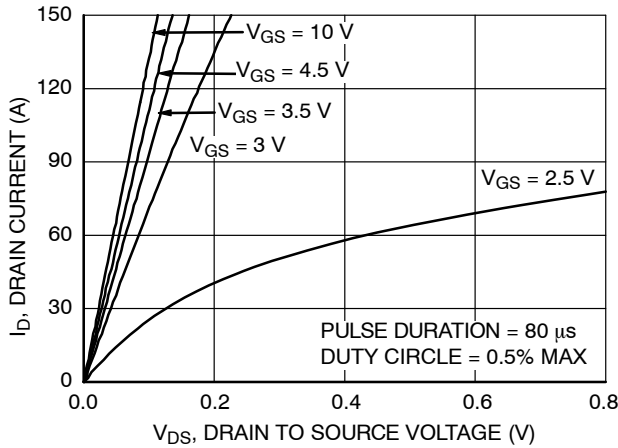


Figure 14. On-Region Characteristics

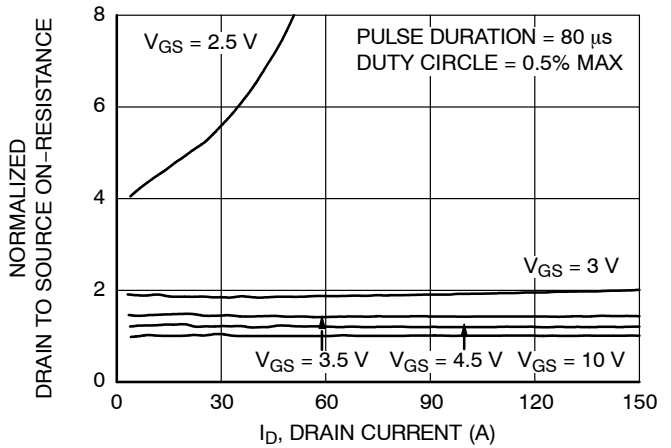


Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage

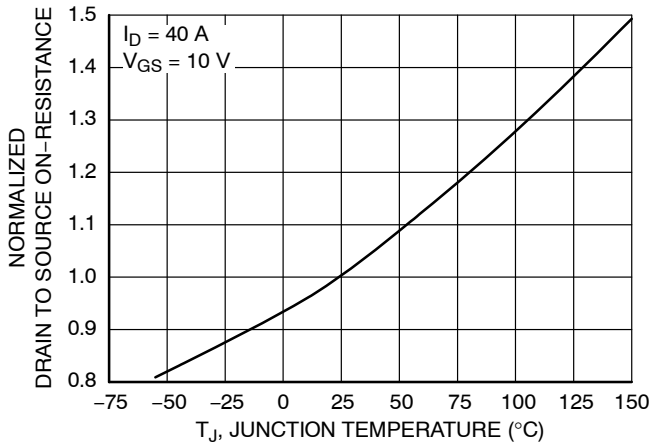


Figure 16. Normalized On-Resistance vs. Junction Temperature

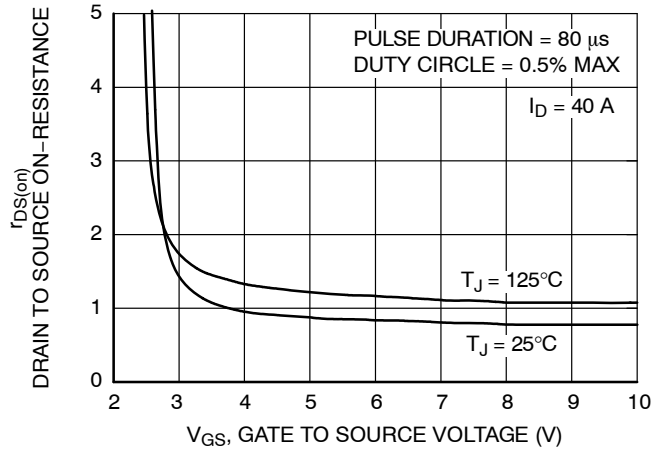


Figure 17. On-Resistance vs. Gate to Source Voltage

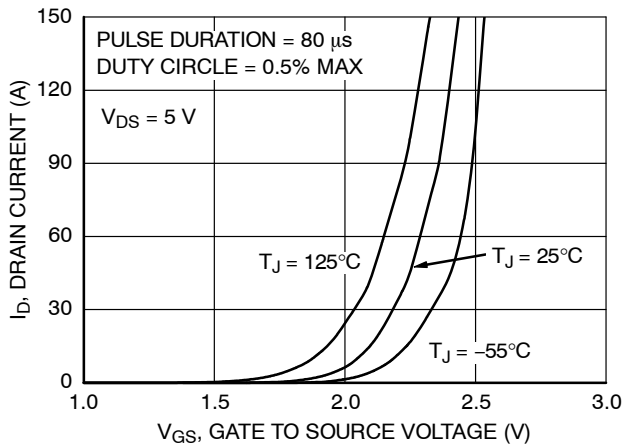


Figure 18. Transfer Characteristics

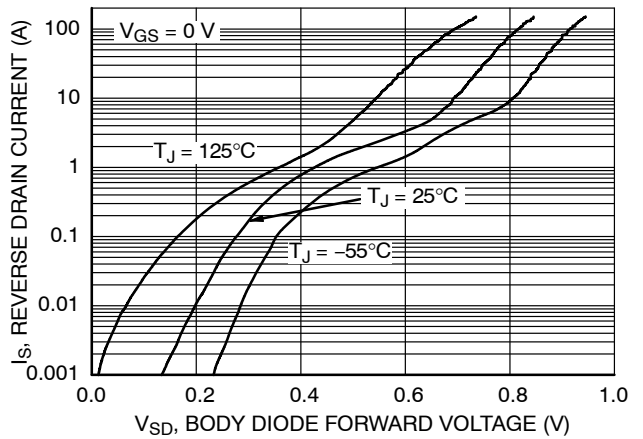


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

FDPC8014AS

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

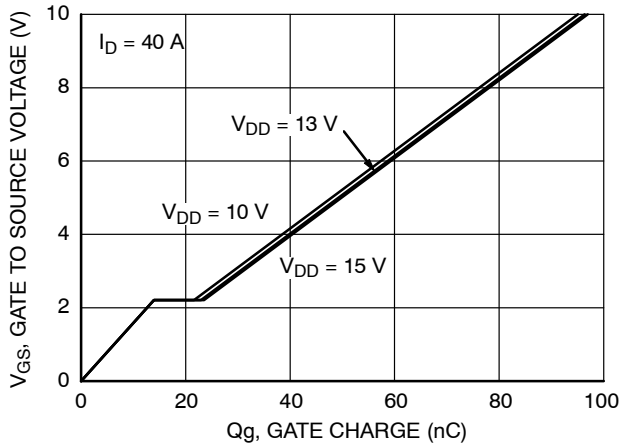


Figure 20. Gate Charge Characteristics

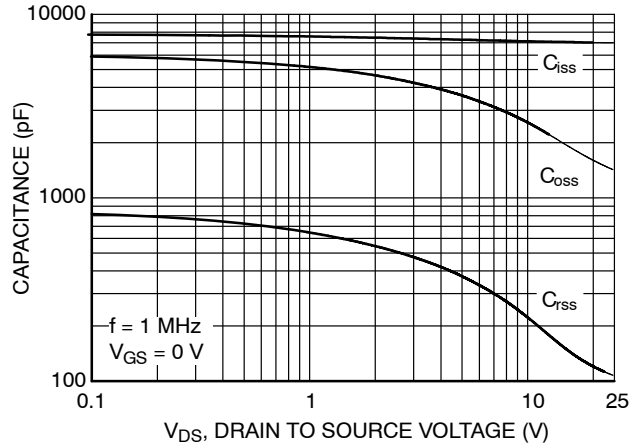


Figure 21. Capacitance vs. Drain to Source Voltage

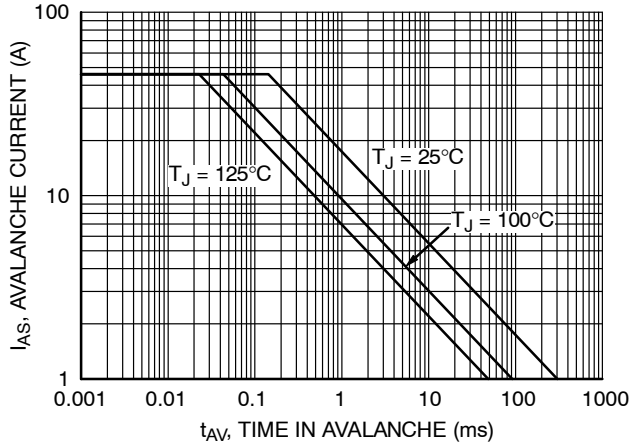


Figure 22. Unclamped Inductive Switching Capability

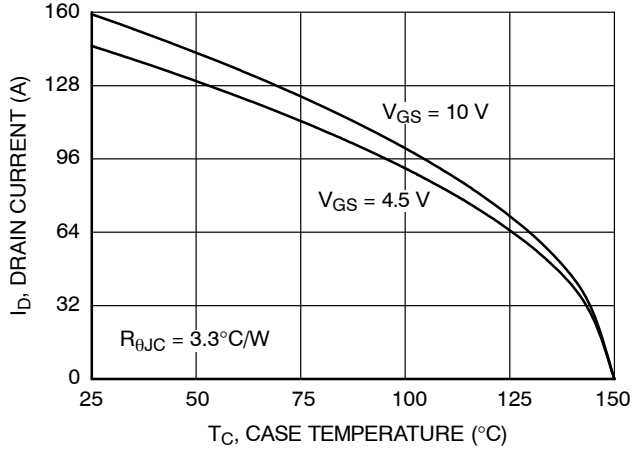


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

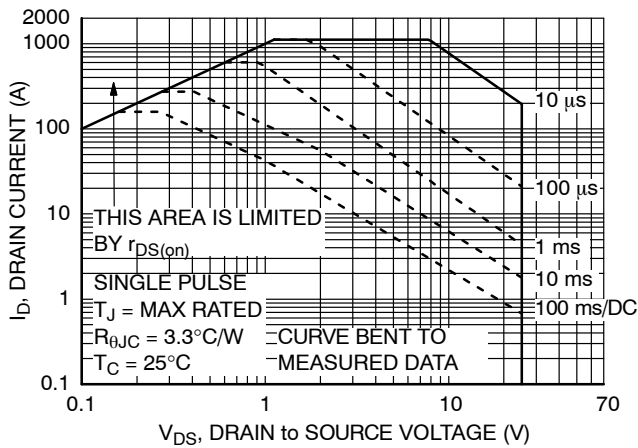


Figure 24. Forward Bias Safe Operating Area

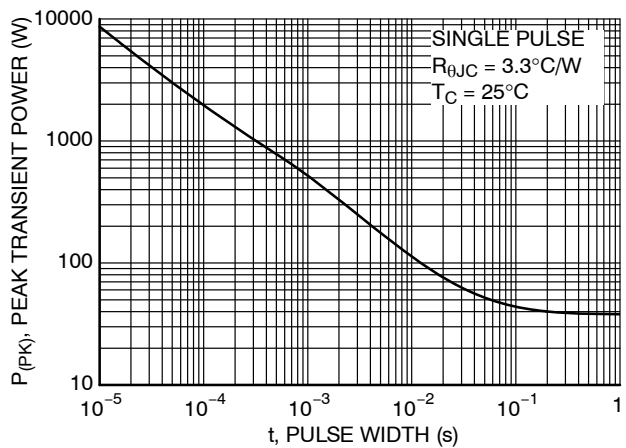


Figure 25. Single Pulse Maximum Power Dissipation

FDPC8014AS

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

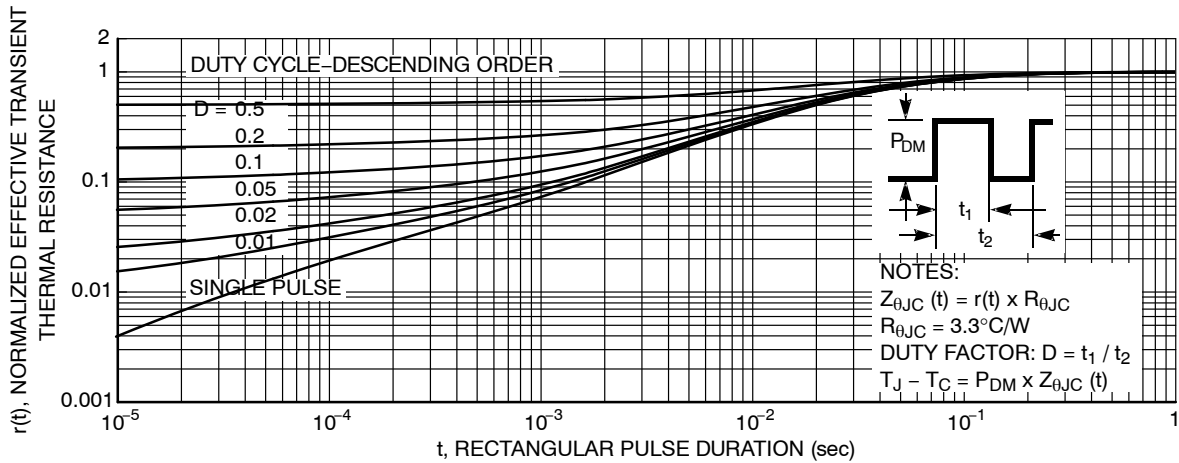


Figure 26. Junction-to-Case Transient Thermal Response Curve

TYPICAL CHARACTERISTICS

SyncFET Schottky Body Diode Characteristics

ON Semiconductor's SyncFET process embeds a Schottky diode in parallel with POWER TRENCH MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET.

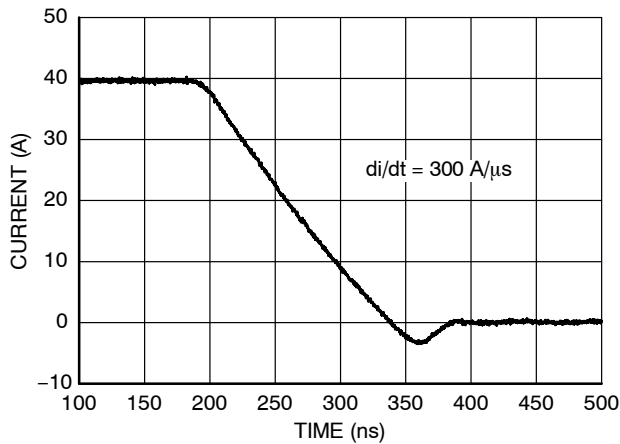


Figure 27. FDPC8014AS SyncFET Body Diode Reverse Recovery Characteristic

Figure 27 shows the reverse recovery characteristic of the FDPC8014AS.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

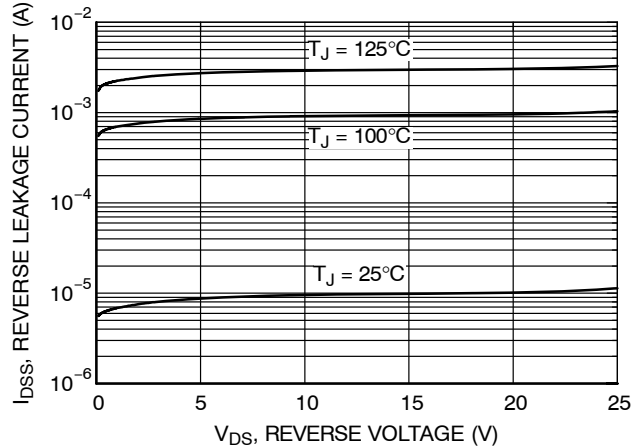


Figure 28. SyncFET Body Diode Reverse Leakage vs. Drain-source Voltage

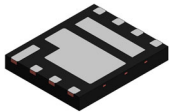
FDPC8014AS

ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping [†]
FDPC8014AS	FDPC8014AS	Power Clip 56 PDFN8 5x6, 1.27P (Pb-Free)	13"	12 mm	2000 / Tape & Reel

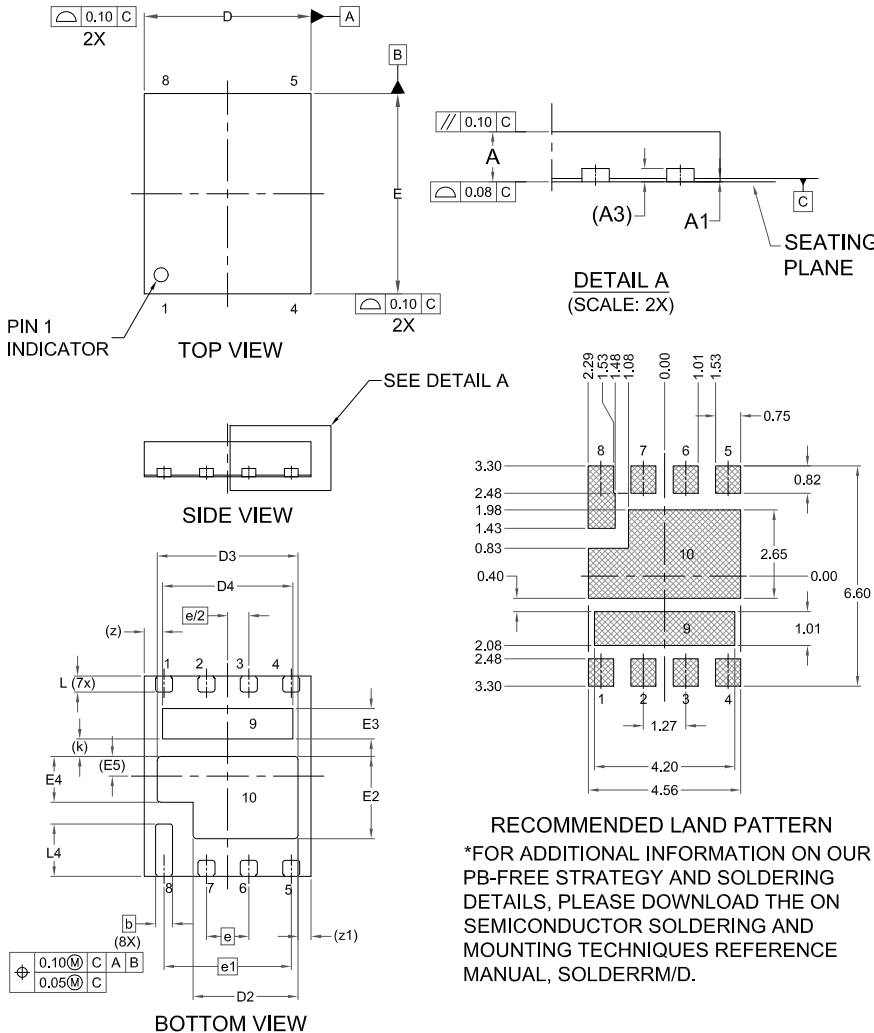
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

POWERTRENCH is registered trademark and SyncFET is trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.



PQFN8 5.00x6.00x0.75, 1.27P
CASE 483AR
ISSUE D

DATE 06 NOV 2023



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.51 BSC		
D	4.90	5.00	5.10
D2	3.05	3.15	3.25
D3	4.12	4.22	4.32
D4	3.80	3.90	4.00
E	5.90	6.00	6.10
E2	2.36	2.46	2.56
E3	0.81	0.91	1.01
E4	1.27	1.37	1.47
E5	0.59 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
k	0.52 REF		
L	0.38	0.48	0.58
L4	1.47	1.57	1.67
z	0.55 REF		
z1	0.39 REF		

RECOMMENDED LAND PATTERN
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

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