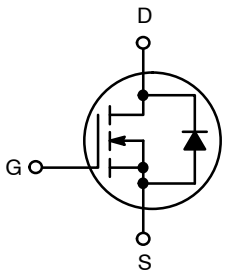
MOSFET – N-Channel, UniFET™
60 V, 55 A, 22 mΩ

FDP55N06 / FDPF55N06

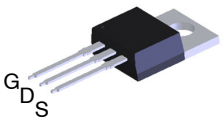


Description

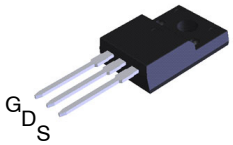
UniFET MOSFET is **onsemi**'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on−state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Features

- $R_{DS(on)}$ = 22 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 27.5 A
- Low Gate Charge (Typ. 30 nC)
- Low C_{rss} (Typ. 60 pF)
- 100% Avalanche Tested

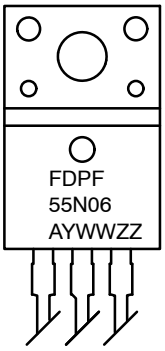


TO−220−3LD
CASE 340AT



TO−220 Fullpack, 3−Lead / TO−220F−3SG
CASE 221AT

MARKING DIAGRAM



FDP55N06, FDPF55N06	= Specific Device Code
A	= Assembly Location
YWW	= Date Code (Year & Week)
ZZ	= Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping
FDP55N06	TO−220	1000 Units / Tube
FDPF55N06	TO−220F	1000 Units / Tube

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FDP55N06	FDPF55N06	Unit
V_{DSS}	Drain to Source Voltage		60	60	V
I_D	Drain Current –	– Continuous (T_C = 25°C) – Continuous (T_C = 100°C)	55 34.8	55* 34.8*	A
I_{DM}	Drain Current	– Pulsed (Note 1)	220	220*	A
V_{GSS}	Gate–Source Voltage		±25	±25	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		480	480	mJ
I_{AR}	Avalanche Current (Note 1)		55	55	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		11.4	11.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C) – Derate Above 25°C	114 0.9	48 0.4	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150	–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 Second		300	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Drain current limited by maximum junction temperature

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. L = 5.6 mH, I_{AS} = 55 A, V_{DD} = 50 V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 55 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP55N06	FDPF55N06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction–to–Case, Max.	1.1	2.58	°C/W
$R_{\theta JS}$	Thermal Resistance, Junction–to–sink, Typ.	0.5	–	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction–to–Ambient, Max.	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain–Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	60	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.05	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 48 V, T_C = 150°C	–	–	10	
I_{GSSF}	Gate–Body Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate–Body Leakage Current, Reverse	V_{GS} = –20 V, V_{DS} = 0 V	–	–	–100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	–	4.0	V
$R_{DS(on)}$	Static Drain–Source On Resistance	V_{GS} = 10 V, I_D = 27.5 A	–	0.018	0.022	Ω
g_{FS}	Forward Transconductance	V_{DS} = 25 V, I_D = 27.5 A	–	33	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	1160	1510	pF
C_{oss}	Output Capacitance		–	375	490	pF
C_{rss}	Reverse Transfer Capacitance		–	60	90	pF

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 30 V, I_D = 55 A, R_G = 25 Ω (Note 4)	–	30	65	ns
t_r	Turn−On Rise Time		–	130	265	ns
$t_{d(off)}$	Turn−Off Delay Time		–	70	150	ns
t_f	Turn−Off Fall Time		–	95	195	ns
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DD} = 48 V, I_D = 55 A, V_{GS} = 10 V (Note 4)	–	30	37	nC
Q_{gs}	Gate−Source Gate Charge		–	6.5	–	nC
Q_{gd}	Gate−Drain Charge		–	7.5	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	55	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	220	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 55 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 55 A dI_F/dt = 100 A/μs	–	40	–	ns
Q_{rr}	Reverse Recovery Charge		–	55	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

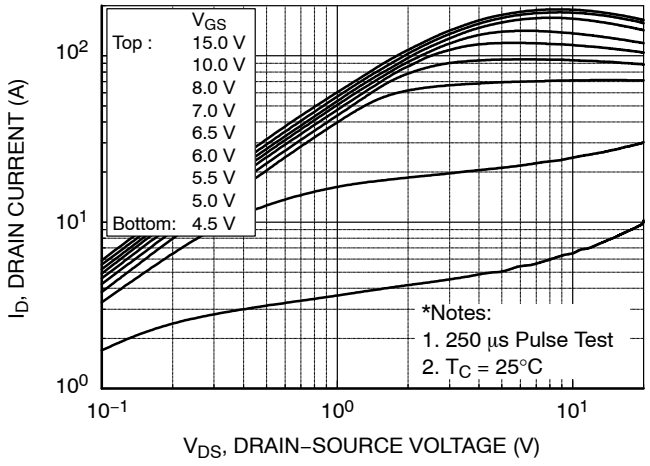


Figure 1. On−Region Characteristics

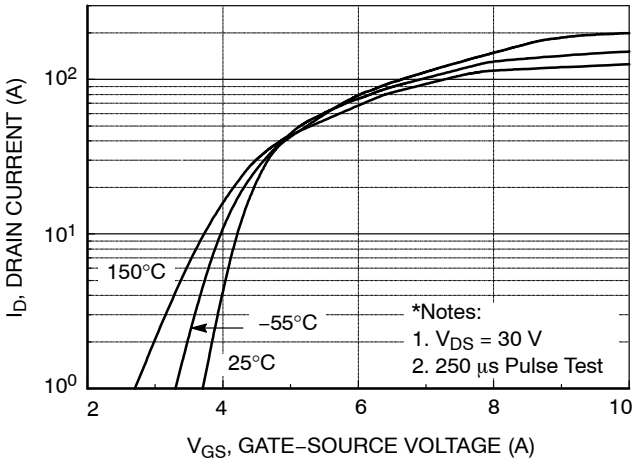


Figure 2. Transfer Characteristics

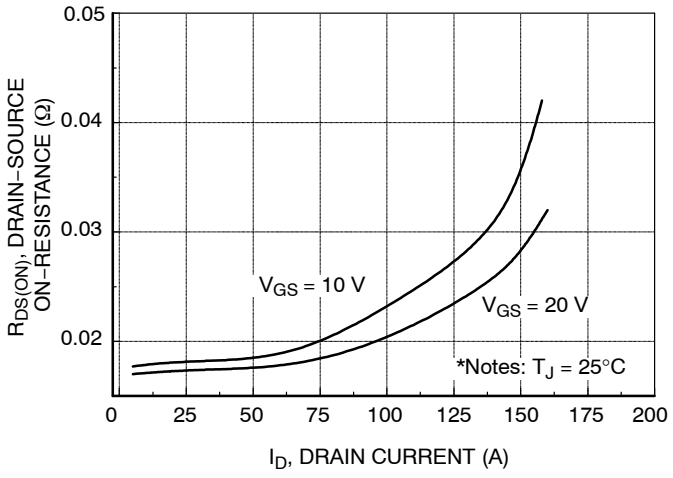


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

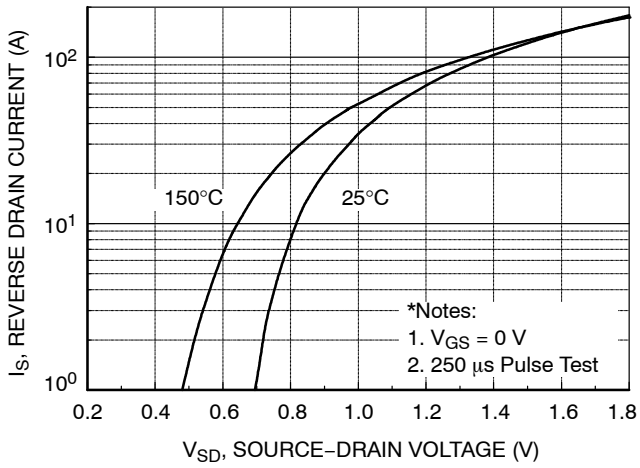


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

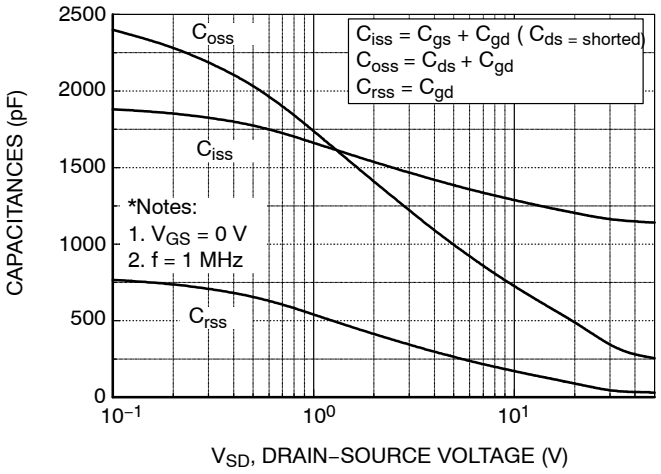


Figure 5. Capacitance Characteristics

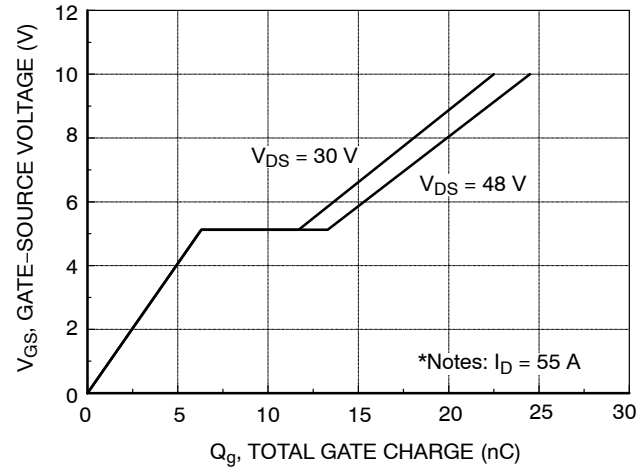


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)

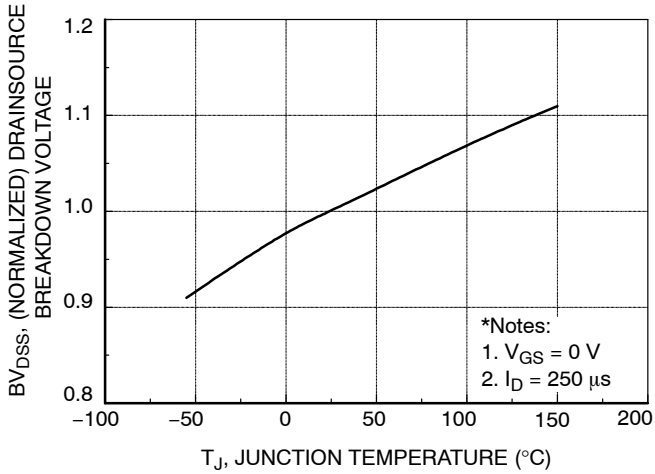


Figure 7. Breakdown Voltage Variation vs. Temperature

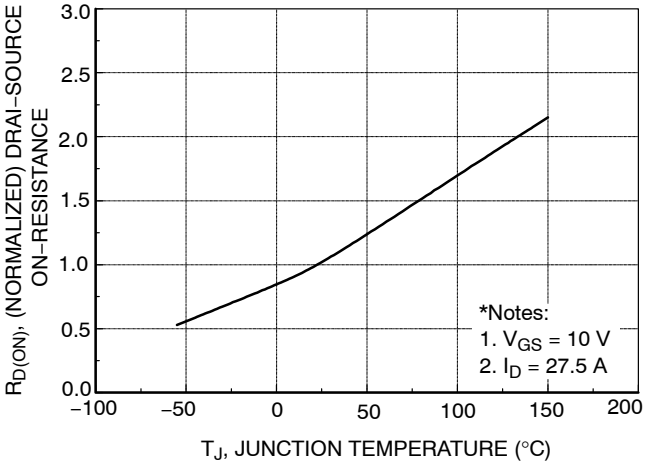


Figure 8. On−Resistance Variation vs. Temperature

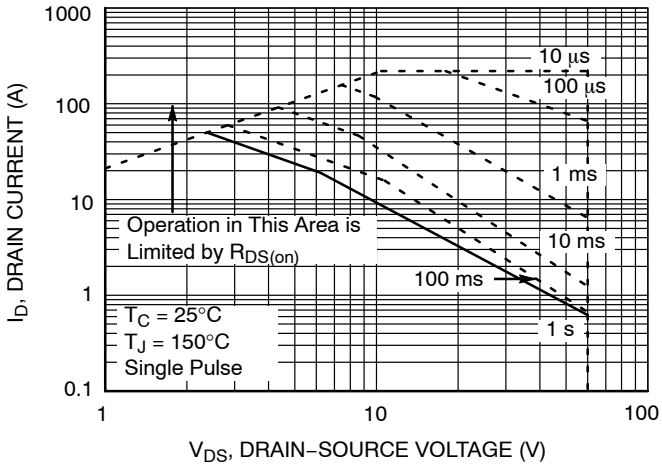


Figure 9−1. Maximum Safe Operating Area for FDP55N06

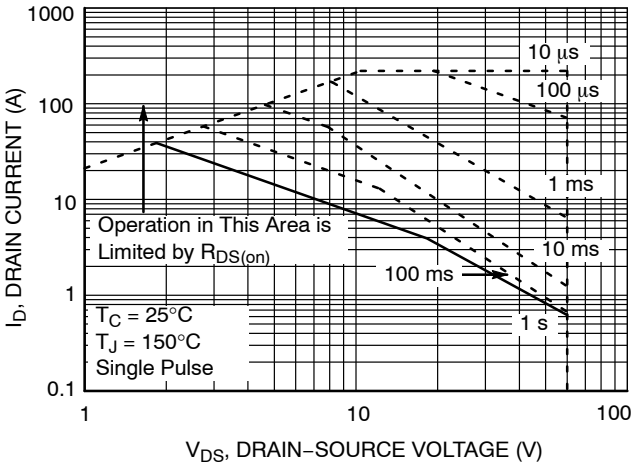


Figure 9−2. Maximum Safe Operating Area for FDPF55N06

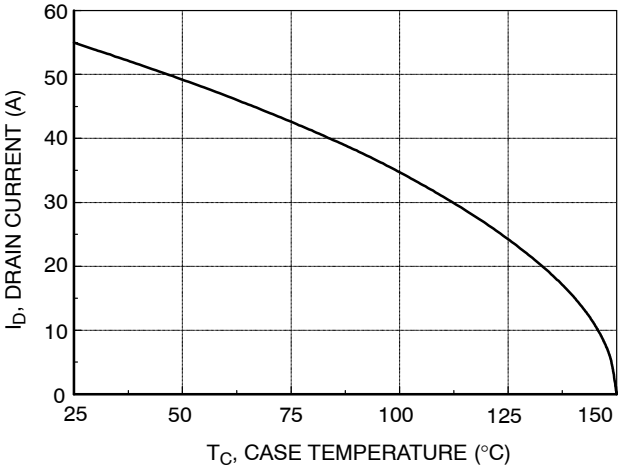


Figure 10. Maximum Drain Current vs. Case Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

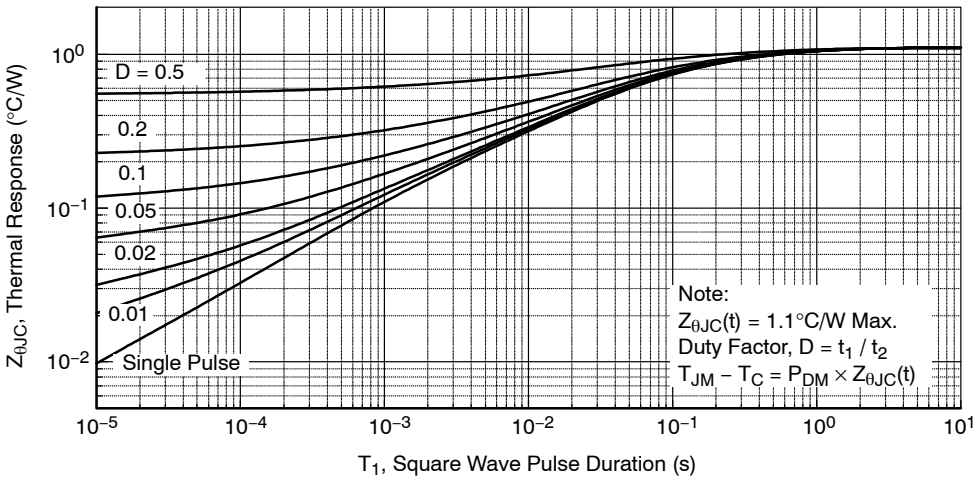


Figure 11−1. Transient Thermal Response Curve for FDP55N06

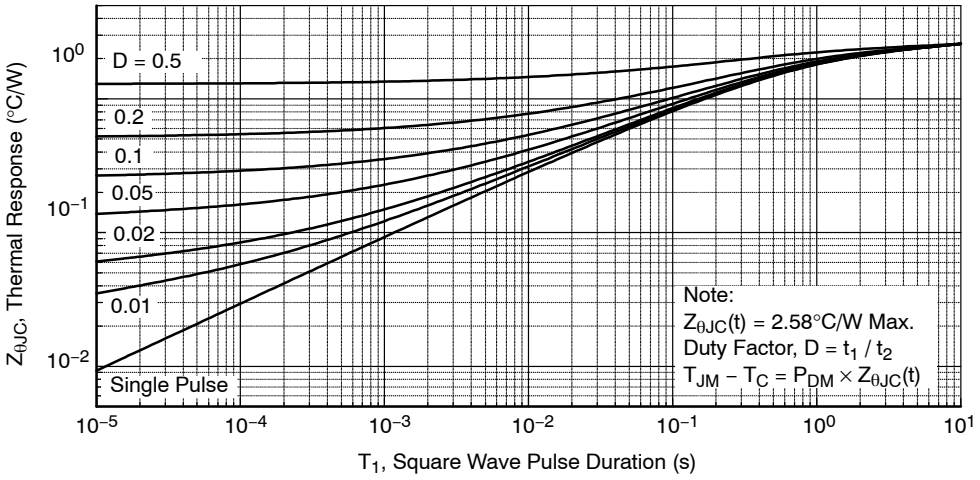


Figure 11−2. Transient Thermal Response Curve for FDPF55N06

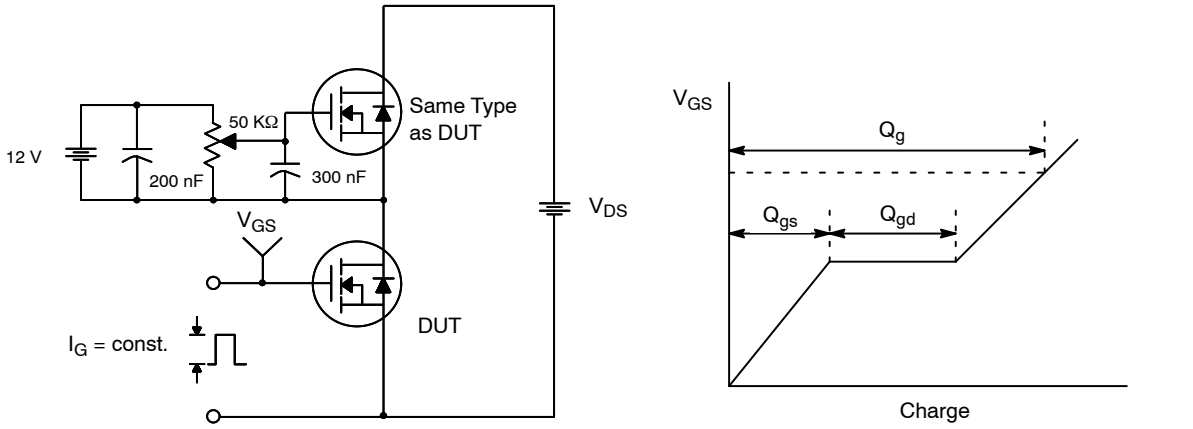


Figure 12. Gate Charge Test Circuit & Waveform

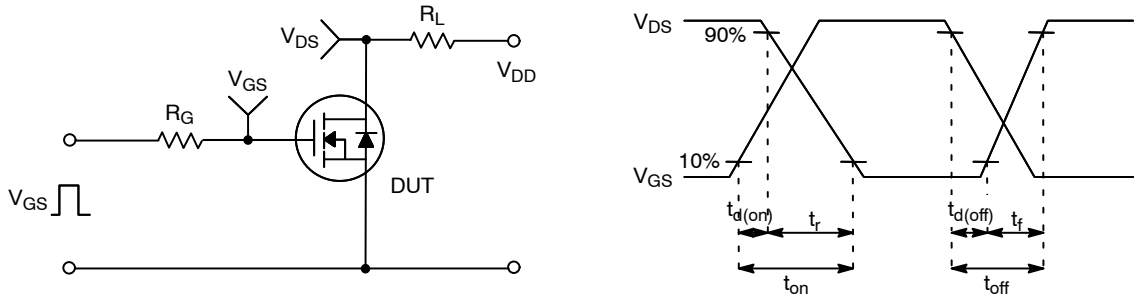


Figure 13. Resistive Switching Test Circuit & Waveforms

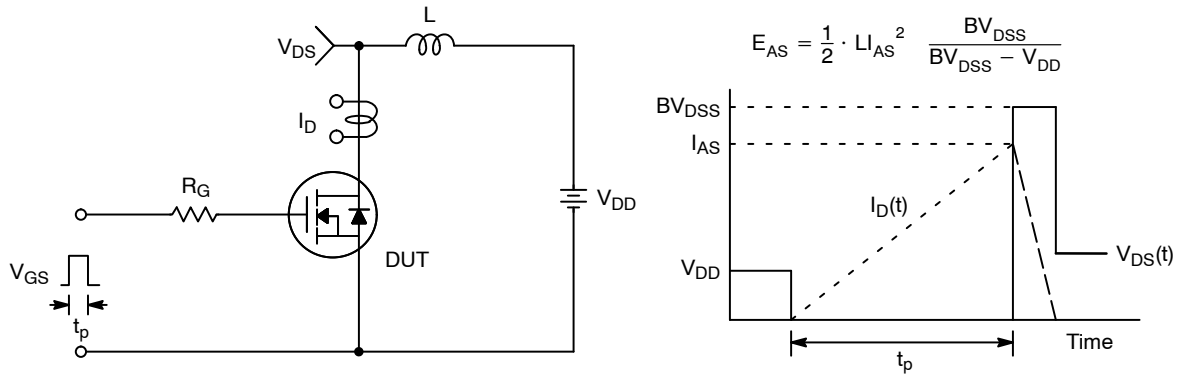


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

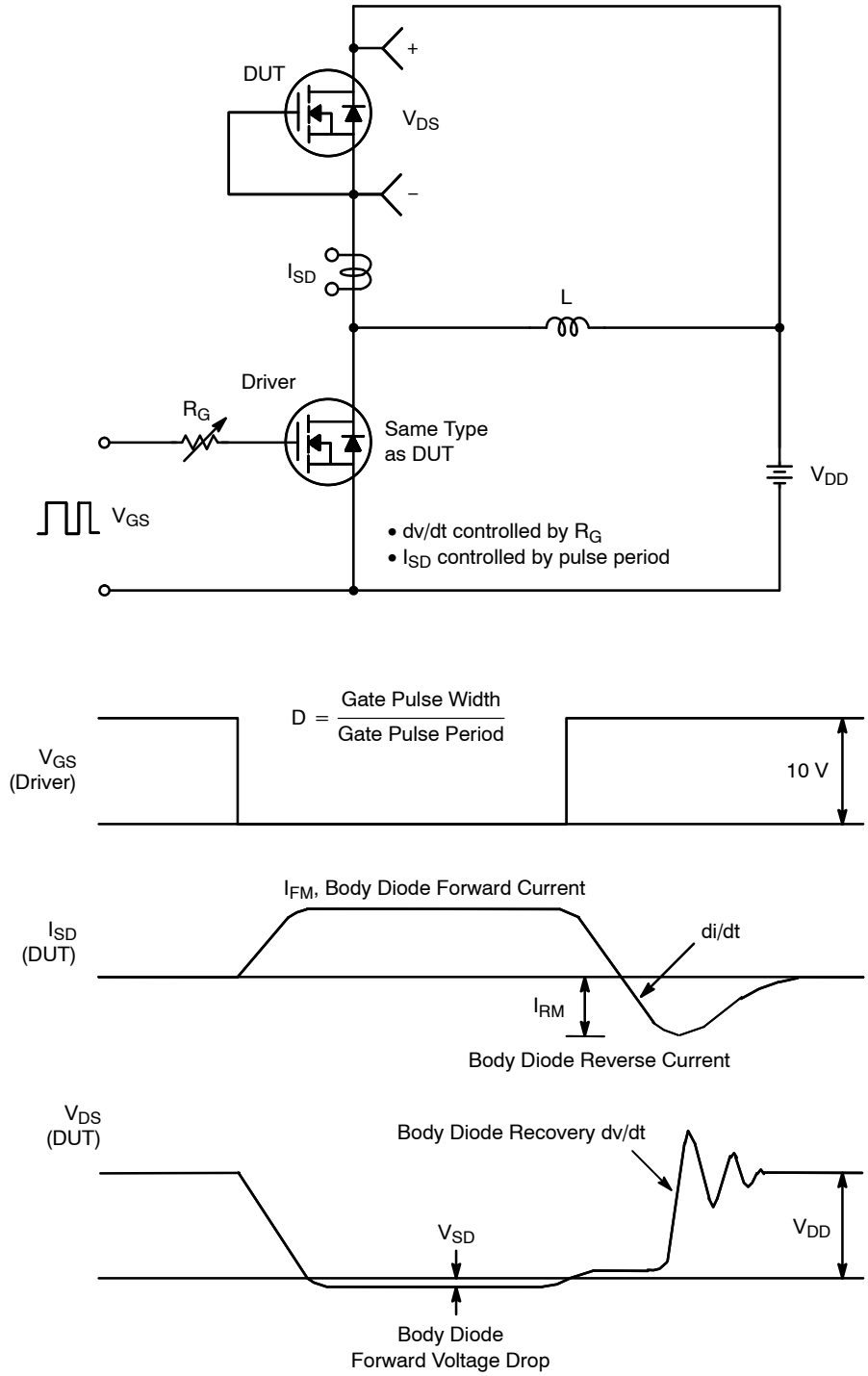
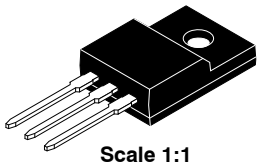


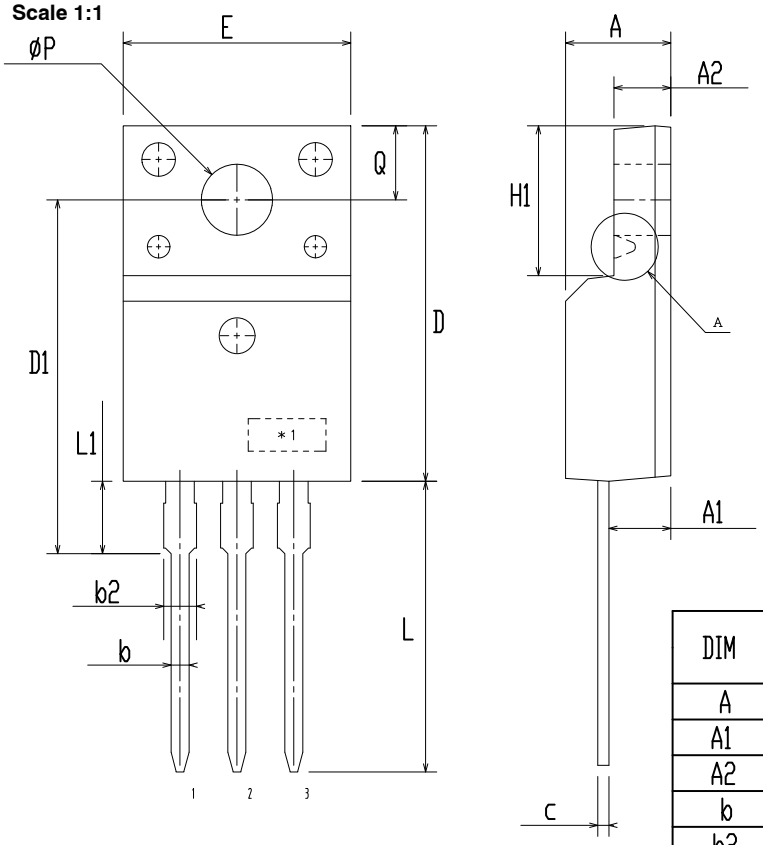
Figure 15. Peak Recovery dv/dt Test Circuit & Waveforms

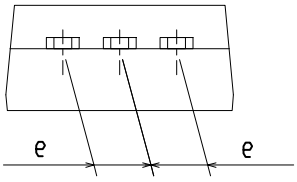
TO−220 Fullpack, 3−Lead / TO−220F−3SG
CASE 221AT
ISSUE B

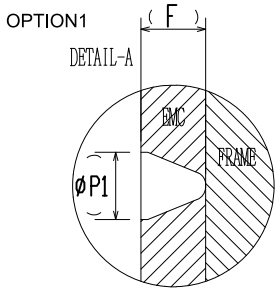
DATE 19 JAN 2021



Scale 1:1







DIM	MILLIMITERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
ø P	2.98	3.18	3.38
ø P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:
A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCSIONS.
C. OPTION 1 - WITH SUPPORT PIN HOLE
OPTION 2 - NO SUPPORT PIN HOLE

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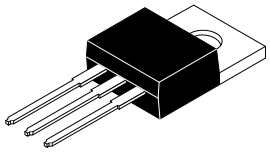
DESCRIPTION:	**TO−220 FULLPACK, 3−LEAD / TO−220F−3SG**		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−220−3LD
CASE 340AT
ISSUE A

DATE 03 OCT 2017



Scale 1:1

NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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DESCRIPTION:	**TO−220−3LD**	**PAGE 1 OF 1**

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