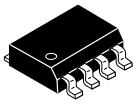
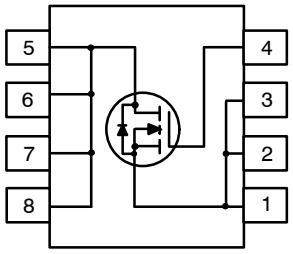
MOSFET – N-Channel, POWERTRENCH®

100 V, 7.5 A, 22 mΩ

FDS3672



SOIC8
CASE 751EB



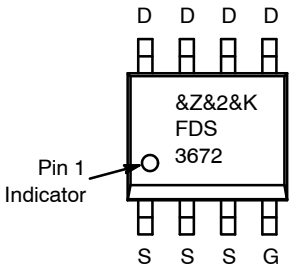
Features

- $r_{DS(ON)}$ = 19 mΩ (Typ.), V_{GS} = 10 V, I_D = 7.5 A
- Q_g(tot) = 28 nC (Typ.), V_{GS} = 10 V
- Low Miller Charge
- Low Q_{RR} Body Diode
- Optimized Efficiency at High Frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)
- Pb−Free and Halide Free

Applications

- DC−DC Converters and Off−Line UPS
- Distributed Power Architecture and VRMs
- Primary Switch for 24 V and 48 V Systems
- High Voltage Synchronous Rectifier

MARKING DIAGRAM



&Z = Assembly Plant Code
&2 = Date Code (Year & Week)
&K = Lot Traceability Code
FDS3672 = Specific Device Code

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_A = 25°C, V_{GS} = 10 V, $R_{\theta JA}$ = 50°C/W) Continuous (T_A = 100°C, V_{GS} = 10 V, $R_{\theta JA}$ = 50°C/W) Pulsed	 7.5 4.8 Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	416	mJ
P_D	Power Dissipation	2.5	W
	Derate above 25°C	20	mW/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting T_J = 25°C, L = 13 mH, I_{AS} = 8 A.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 10 s (Note 3)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 1000 s (Note 3)	85	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 2)	25	°C/W

2. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
3. $R_{\theta JA}$ is measured with 1.0 in^2 copper on FR−4 board.

ORDERING INFORMATION

Device	Package	Shipping
FDS3672	SOIC8 (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 80 V, V_{GS} = 0 V, T_C = 150°C	–	–	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	–	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 7.5 A, V_{GS} = 10 V I_D = 6.8 A, V_{GS} = 6 V, I_D = 7.5 A, V_{GS} = 10 V, T_C = 150°C	– – –	0.019 0.023 0.035	0.023 0.028 0.043	Ω
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	2015	–	pF
C_{OSS}	Output Capacitance		–	285	–	pF
C_{RSS}	Reverse Transfer Capacitance		–	70	–	pF
$Q_{g(TOT)}$	Total Gate Charge at 10 V	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_D = 7.5 A, I_g = 1.0 A	–	28	37	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0 V to 2 V, V_{DD} = 50 V, I_D = 7.5 A, I_g = 1.0 A	–	4	6	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 50 V, I_D = 7.5 A, I_g = 1.0 A	–	10	–	nC
Q_{gs2}	Gate Charge Threshold to Plateau		–	6.8	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	6	–	nC
SWITCHING CHARACTERISTICS (V_{GS} = 10 V)						
t_{ON}	Turn−On Time	V_{DD} = 50 V, I_D = 4 A, V_{GS} = 10 V, R_{GS} = 10 Ω	–	–	51	ns
$t_{d(ON)}$	Turn−On Delay Time		–	14	–	ns
t_r	Rise Time		–	20	–	ns
$t_{d(OFF)}$	Turn−Off Delay Time		–	37	–	ns
t_f	Fall Time		–	27	–	ns
t_{OFF}	Turn−Off Time		–	–	96	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Drain to Source Diode Voltage	I_{SD} = 7.5 A	–	–	1.25	V
		I_{SD} = 4 A	–	–	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 7.5 A, dI_{SD}/dt = 100 A/μs	–	–	55	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 7.5 A, dI_{SD}/dt = 100 A/μs	–	–	90	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

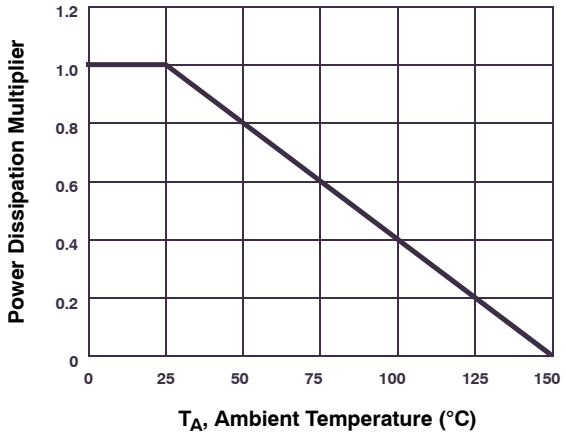


Figure 1. Normalized Power Dissipation vs. Ambient Temperature

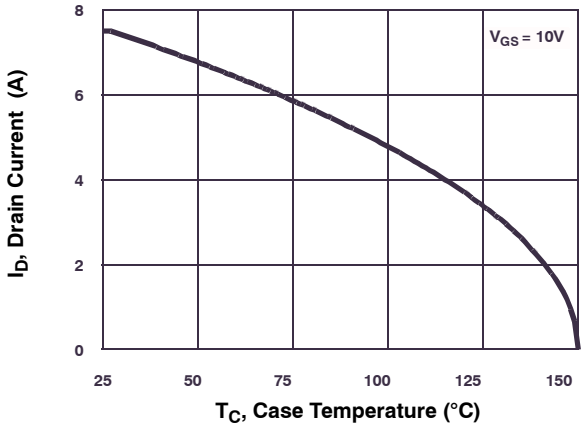


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

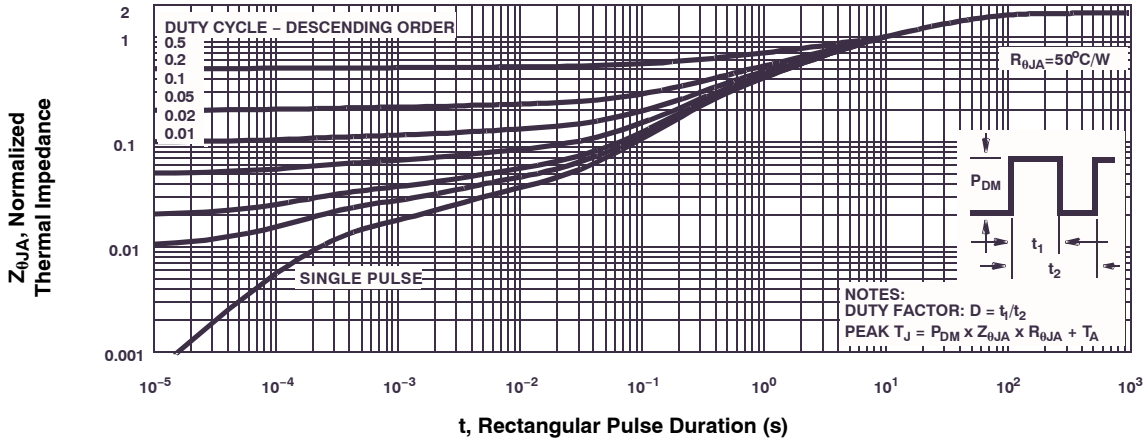


Figure 3. Normalized Maximum Transient Thermal Impedance

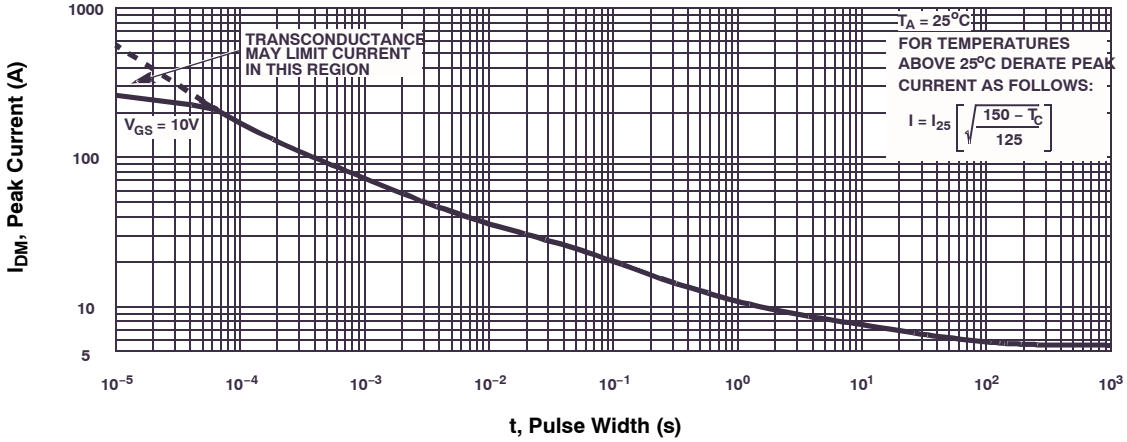


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (Continued)

(T_A = 25°C unless otherwise noted)

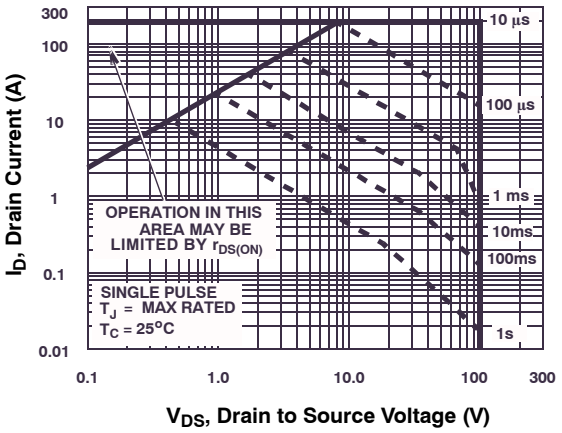


Figure 5. Forward Bias Safe Operating Area

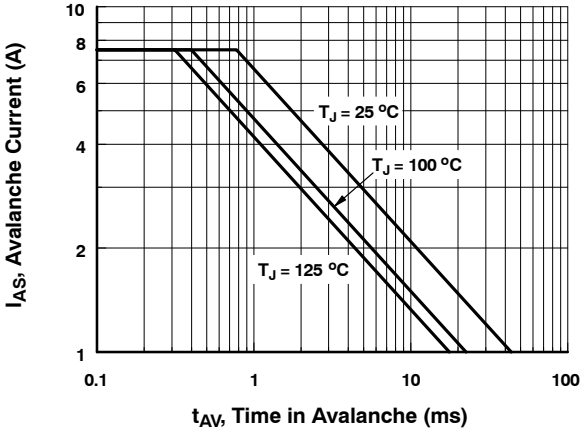


Figure 6. Unclamped Inductive Switching Capability

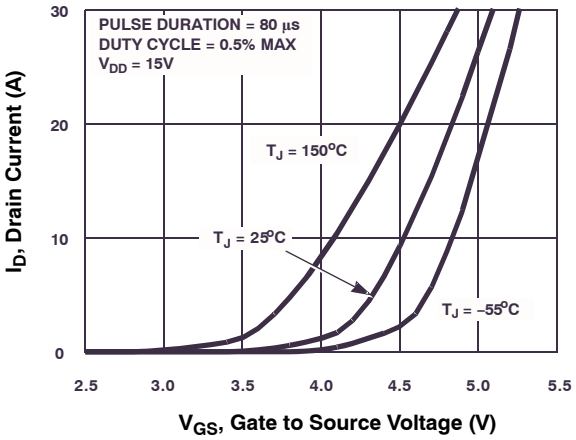


Figure 7. Transfer Characteristics

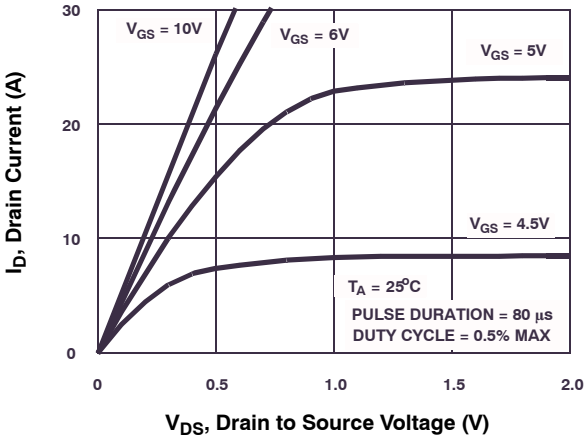


Figure 8. Saturation Characteristics

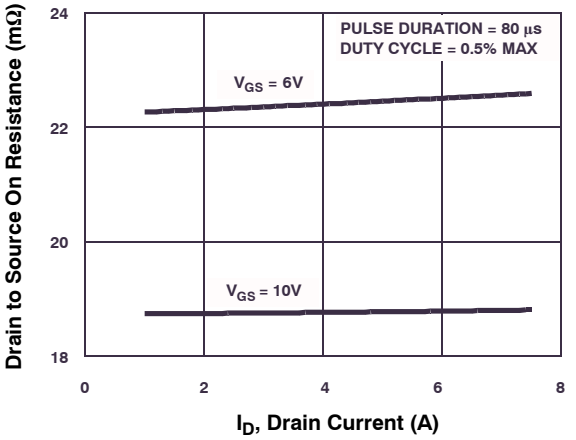


Figure 9. Drain to Source On Resistance vs. Drain Current

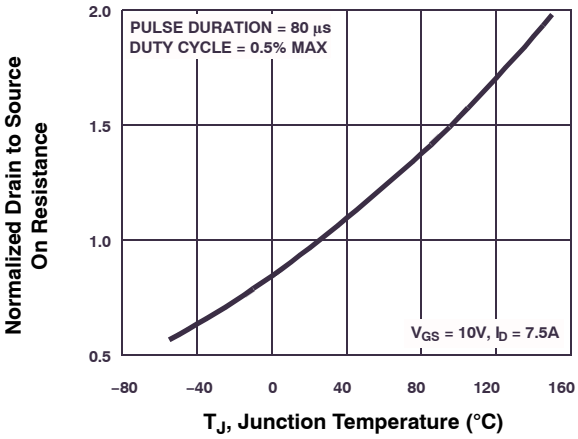


Figure 10. Normalized Drain to Source On Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (Continued)

(T_A = 25°C unless otherwise noted)

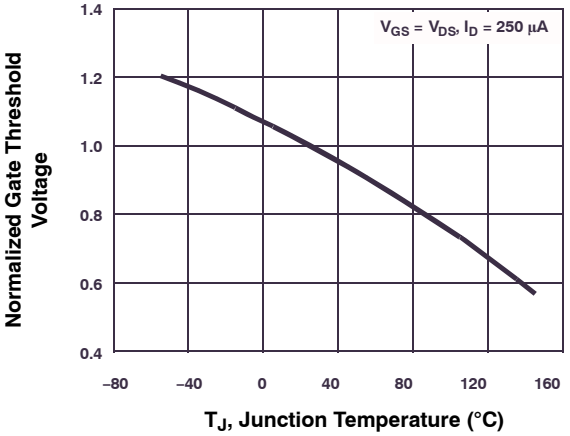


Figure 11. Normalized Gate Threshold Voltage vs. Junction Temperature

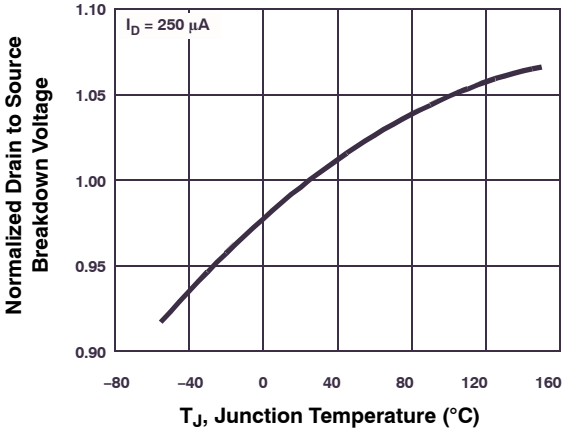


Figure 12. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

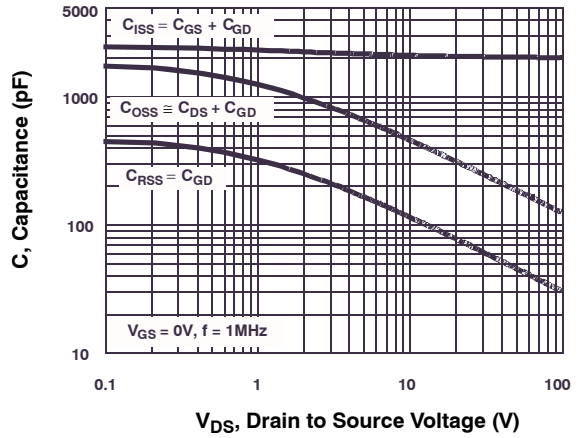


Figure 13. Capacitance vs. Drain to Source Voltage

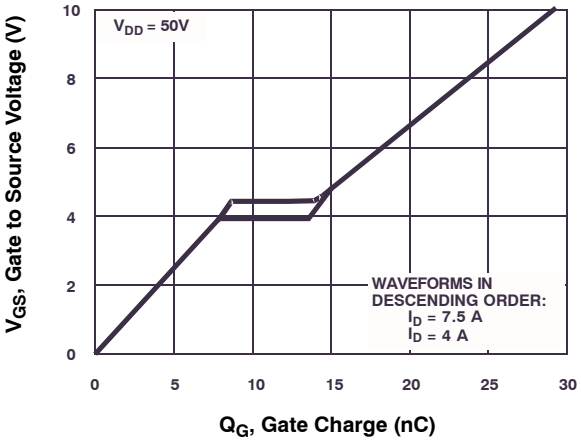


Figure 14. Gate Charge Waveforms for Constant Gate Currents

TEST CIRCUITS AND WAVEFORMS

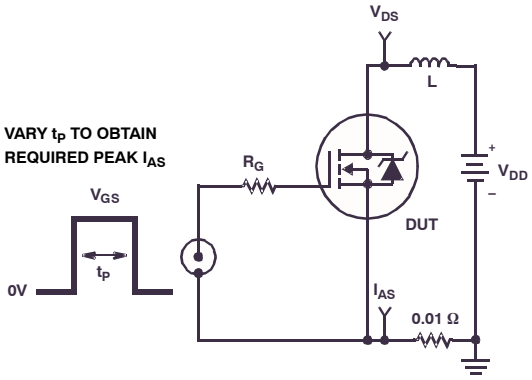


Figure 15. Unclamped Energy Test Circuit

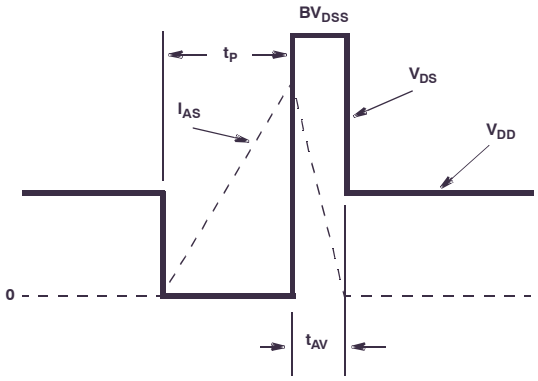


Figure 16. Unclamped Energy Waveforms

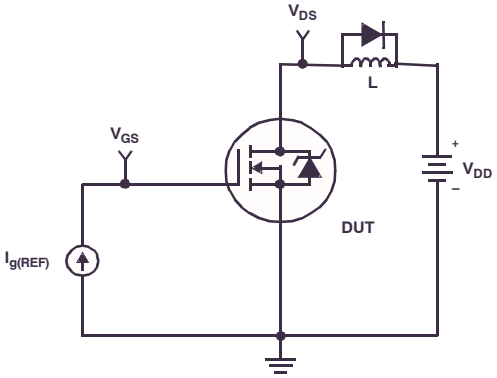


Figure 17. Gate Charge Test Circuit

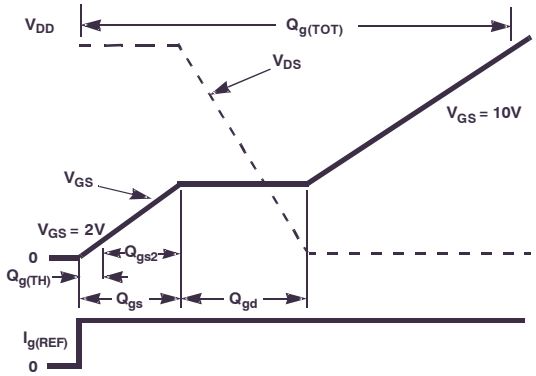


Figure 18. Gate Charge Waveforms

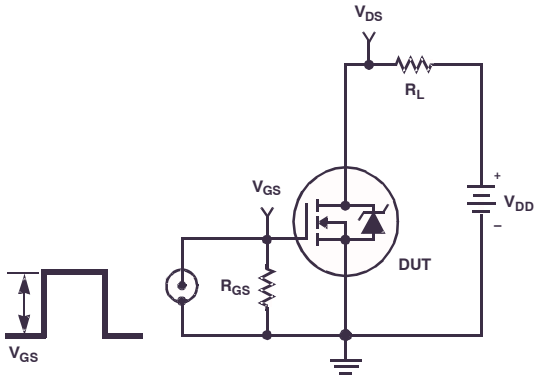


Figure 19. Switching Time Test Circuit

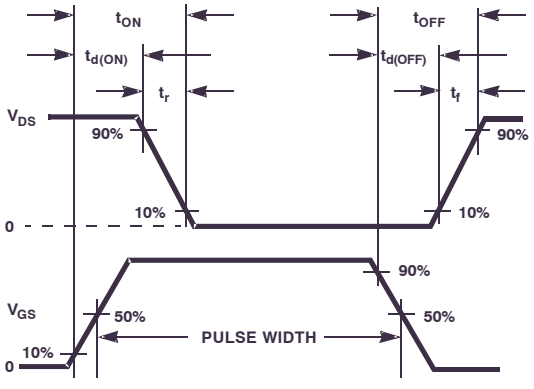


Figure 20. Switching Time Waveforms

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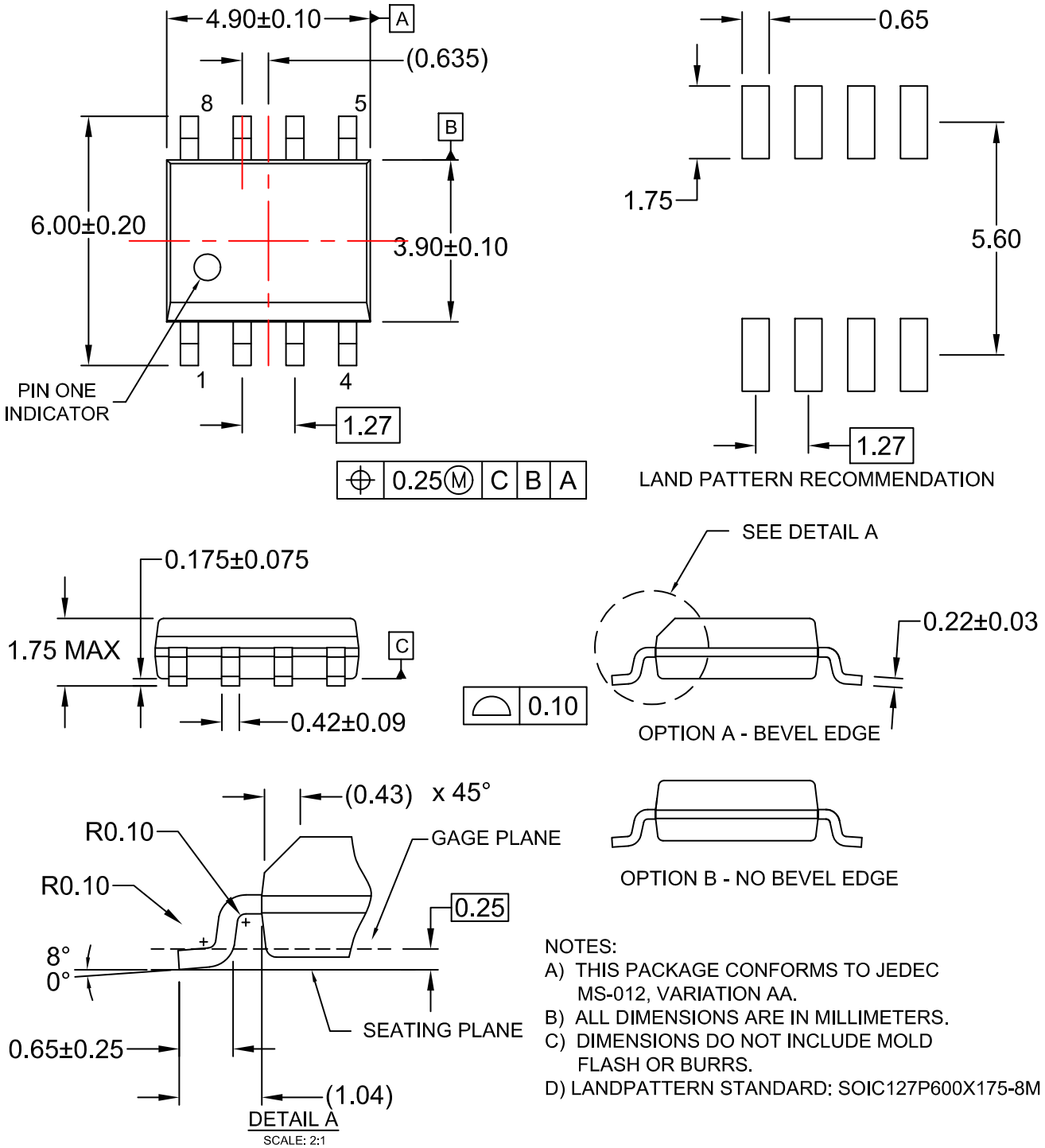
ISSUE A

DATE 24 AUG 2017



NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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