

MOSFET – Complementary, POWERTRENCH®

60 V

FDS4559

General Description

This complementary MOSFET device is produced using onsemi’s advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Features

- Q1: N-Channel
 - ◆ 4.5 A, 60 V
 - $R_{DS(on)} = 55\text{ m}\Omega @ V_{GS} = 10\text{ V}$
 - $R_{DS(on)} = 75\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
- Q2: P-Channel
 - ◆ -3.5 A, -60 V
 - $R_{DS(on)} = 105\text{ m}\Omega @ V_{GS} = -10\text{ V}$
 - $R_{DS(on)} = 135\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$

Applications

- DC/DC converter
- Power management
- LCD backlight inverter
- This is a Pb-Free and Halide Free Device

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

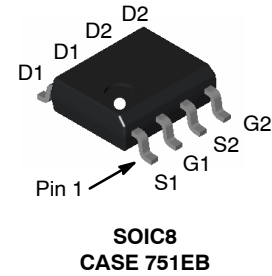
Symbol	Parameter	Q1	Q2	Unit	
V _{DSS}	Drain-Source Voltage	60	-60	V	
V _{GSS}	Gate-Source Voltage	±20	±20	V	
I _D	Drain Current	Continuous (Note 1a)	4.5	-3.5	A
		Pulsed	20	-20	
P _D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1.2		
		(Note 1c)	1		
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +175		°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

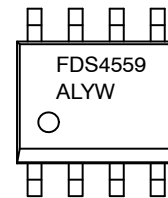
THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

V _{DSS}	R _{DS(on)} Max	I _D Max
N-Channel 60 V	55 mΩ @ 10 V	4.5 A
	75 mΩ @ 4.5 V	
P-Channel -60 V	105 mΩ @ -10 V	-3.5 A
	135 mΩ @ -4.5 V	

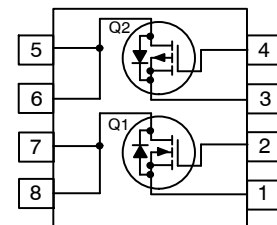


MARKING DIAGRAM



FDS4559 = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

N-Channel / P-Channel



ORDERING INFORMATION

Device	Package	Shipping†
FDS4559	SOIC8 (Pb-Free, Halide Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

FDS4559

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Typ	Min	Typ	Max	Unit
--------	-----------	----------------	-----	-----	-----	-----	------

DRAIN-SOURCE AVALANCHE RATINGS (Note 1)

W _{DSS}	Single Pulse Drain-Source Avalanche Energy	V _{DD} = 30 V, I _D = 25 A	Q1	-	-	90	V
I _{AR}	Maximum Drain-Source Avalanche Current		Q1	-	-	4.5	V

OFF CHARACTERISTICS

BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA V _{GS} = 0 V, I _D = -250 μA	Q1 Q2	60 -60	- -	- -	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C I _D = -250 μA, Referenced to 25°C	Q1 Q2	- -	58 -49	- -	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 48 V, V _{GS} = 0 V V _{DS} = -48 V, V _{GS} = 0 V	Q1 Q2	- -	- -	1 -1	μA
I _{GSS}	Gate-Body Leakage	V _{GS} = ±20 V, V _{DS} = 0 V V _{GS} = ±20 V, V _{DS} = 0 V	Q1 Q2	- -	- -	±100 ±100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA V _{DS} = V _{GS} , I _D = -250 μA	Q1 Q2	1 -1	2.2 -1.6	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C I _D = -250 μA, Referenced to 25°C	Q1 Q2	- -	-5.5 4	- -	mV/°C
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 4.5 A V _{GS} = 10 V, I _D = 4.5 A, T _j = 125°C V _{GS} = 4.5 V, I _D = 4 A	Q1	- - -	42 72 55	55 94 75	mΩ
		V _{GS} = -10 V, I _D = -3.5 A V _{GS} = -10 V, I _D = -3.5 A, T _j = 125°C V _{GS} = -4.5 V, I _D = -3.1 A	Q2	- - -	82 130 105	105 190 135	mΩ
I _{D(on)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V V _{GS} = -10 V, V _{DS} = -5 V	Q1 Q2	20 -20	- -	- -	A
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 4.5 A V _{DS} = -5 V, I _D = -3.5 A	Q1 Q2	- -	14 9	- -	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	Q1 V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 Mhz	Q1 Q2	- -	650 759	- -	pF
C _{oss}	Output Capacitance		Q1 Q2	- -	80 90	- -	pF
C _{rss}	Reverse Transfer Capacitance	Q2 V _{DS} = -30 V, V _{GS} = 0 V, f = 1.0 MHz	Q1 Q2	- -	35 39	- -	pF

SWITCHING CHARACTERISTICS (Note 2)

t _{d(on)}	Turn-On Delay Time	Q1 V _{DD} = 30 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	Q1 Q2	- -	11 7	20 14	ns
t _r	Turn-On Rise Time		Q1 Q2	- -	8 10	18 20	ns
t _{d(off)}	Turn-Off Delay Time	Q2 V _{DD} = -30 V, I _D = -1 A, V _{GS} = -10 V, R _{GEN} = 6 Ω	Q1 Q2	- -	19 19	35 34	ns
t _f	Turn-Off Fall Time		Q1 Q2	- -	6 12	15 22	ns
Q _g	Total Gate Charge	Q1 V _{DD} = 30 V, I _D = 4.5 A, V _{GS} = 10 V	Q1 Q2	- -	12.5 15	18 21	nC
Q _{gs}	Gate-Source Charge		Q1 Q2	- -	2.4 2.5	- -	nC
Q _{gd}	Gate-Drain Charge	Q2 V _{DD} = -30 V, I _D = -3.5 A, V _{GS} = -10 V	Q1 Q2	- -	2.6 3.0	- -	nC

FDS4559

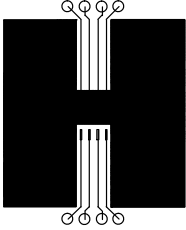
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

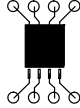
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2	- -	- -	1.3 -1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)	Q1 Q2	- -	0.8 -0.8	1.2 -1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

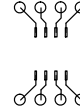
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in^2 pad of 2 oz copper



b) 125°C/W when mounted on a $.02\text{ in}^2$ pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad

Scale 1:1 on letter size paper

- Pulse Test: Pulse Width $< 300\ \mu\text{s}$, Duty Cycle $< 2.0\%$

TYPICAL CHARACTERISTICS (Q2 P-CHANNEL)

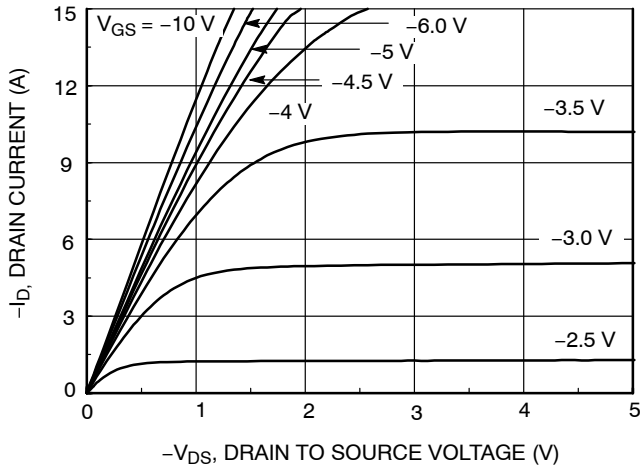


Figure 1. On-Region Characteristics

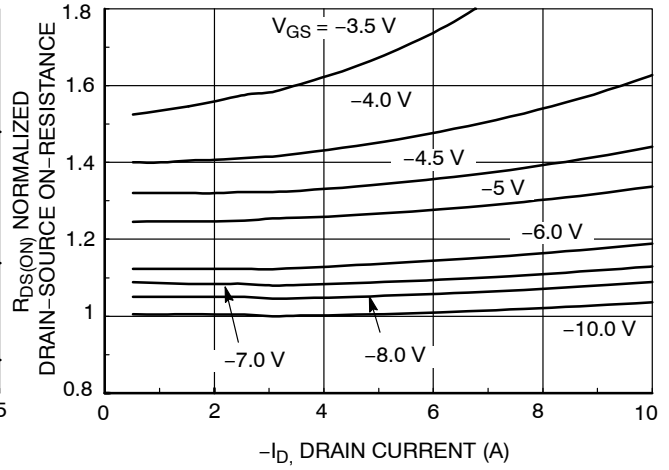


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

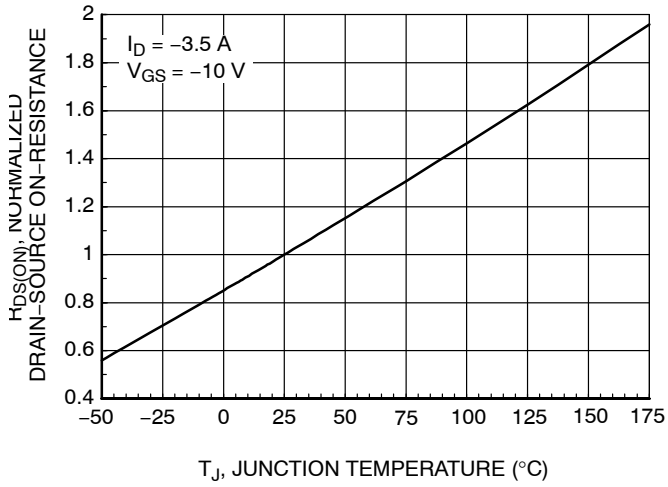


Figure 3. On-Resistance Variation with Temperature

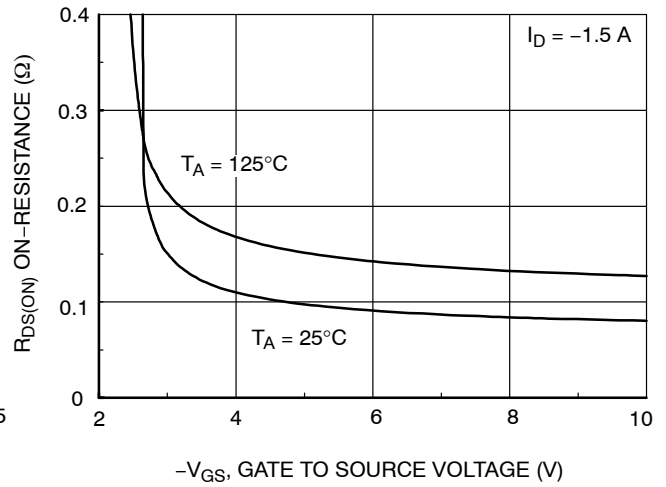


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

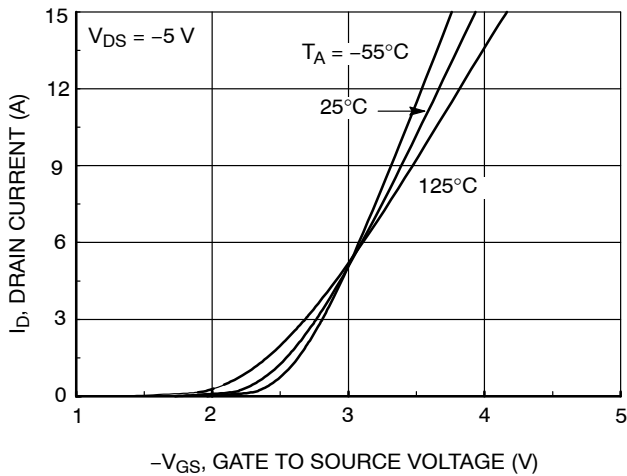


Figure 5. Transfer Characteristics

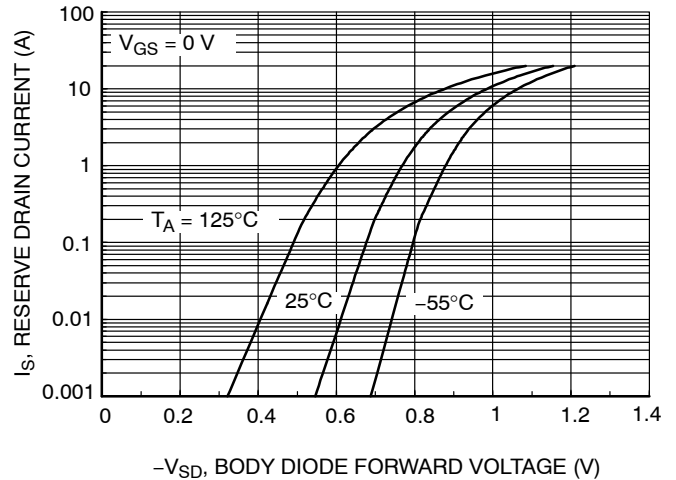


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (Q2 P-CHANNEL) (continued)

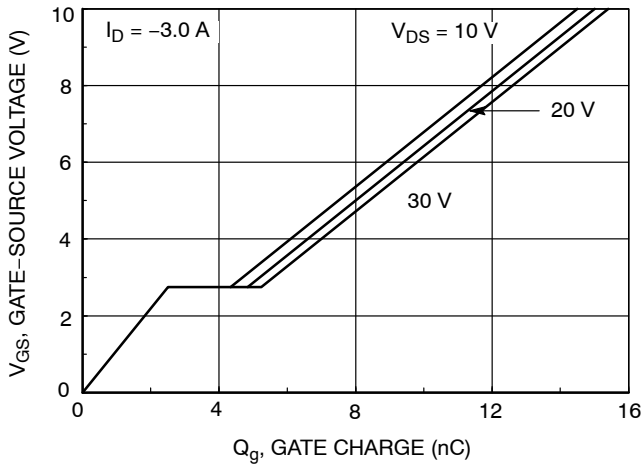


Figure 7. Gate Charge Characteristics

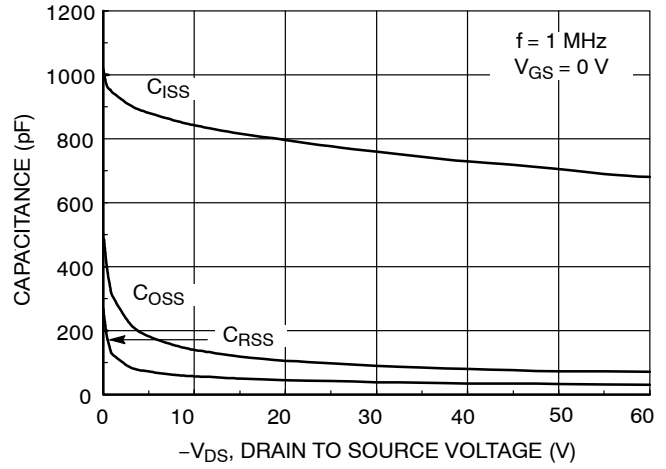


Figure 8. Capacitance Characteristics

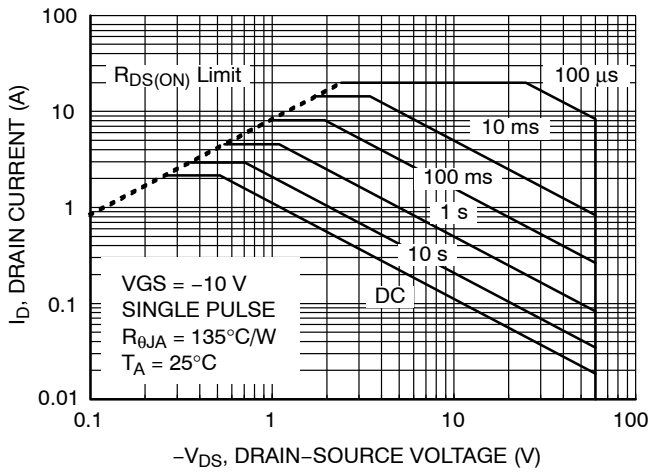


Figure 9. Maximum Safe Operating Area

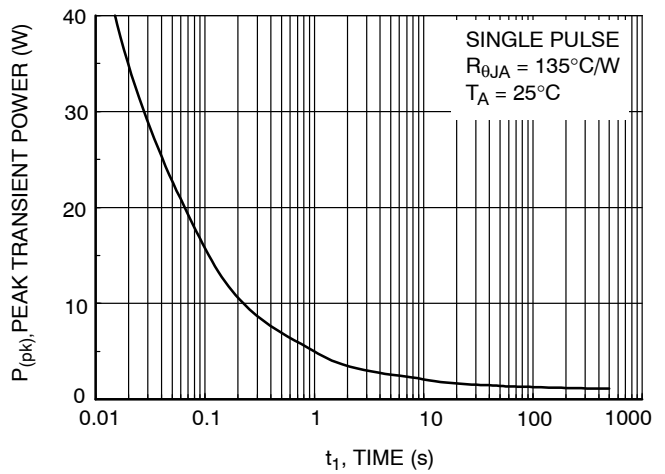


Figure 10. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)

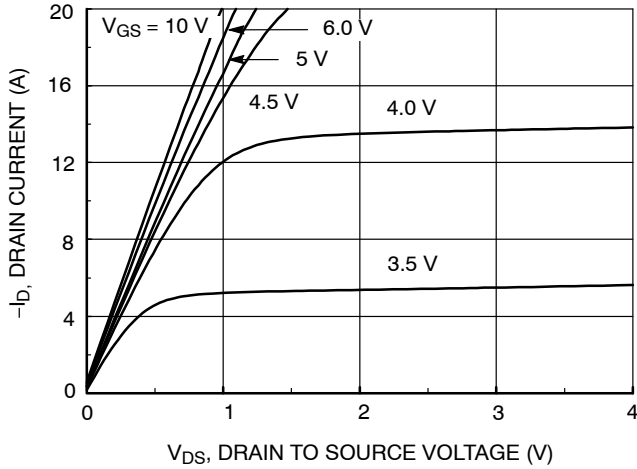


Figure 11. On-Region Characteristics

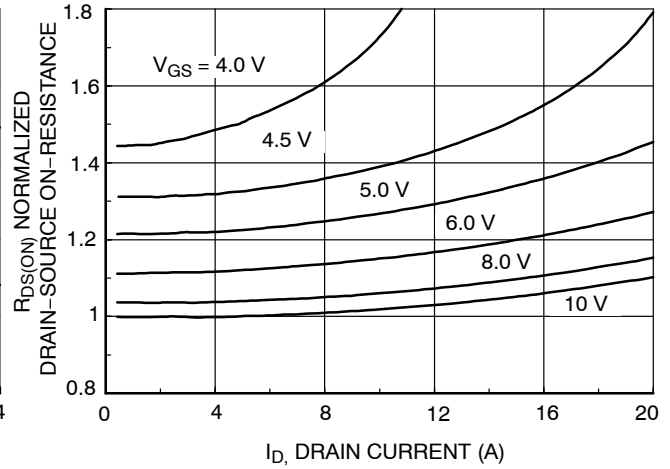


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage

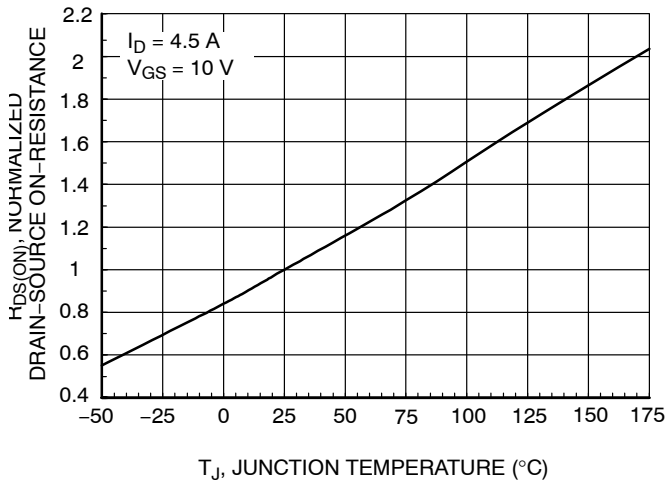


Figure 13. On-Resistance Variation with Temperature

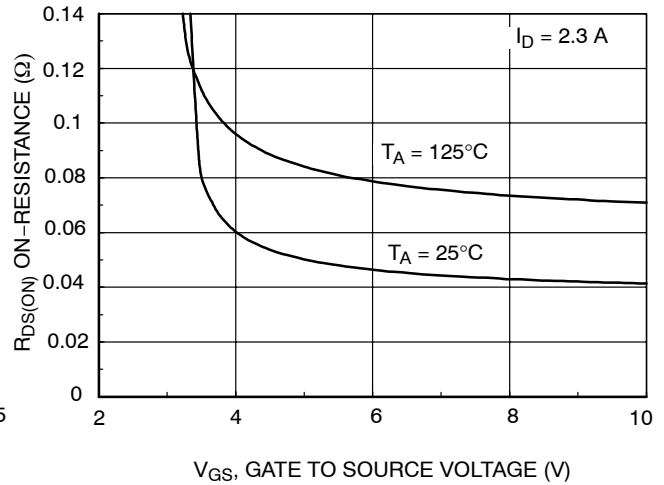


Figure 14. On-Resistance Variation with Gate-to-Source Voltage

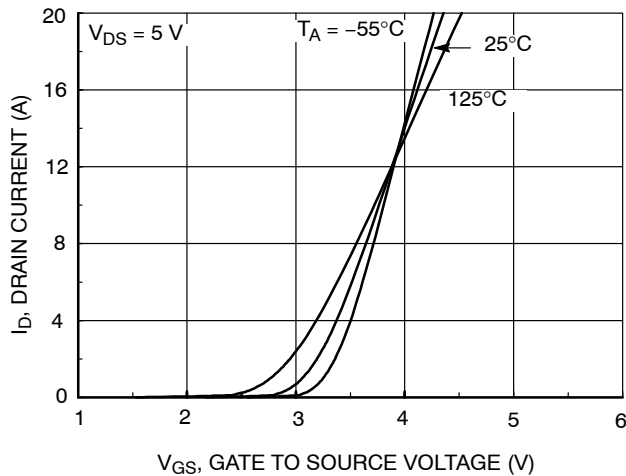


Figure 15. Transfer Characteristics

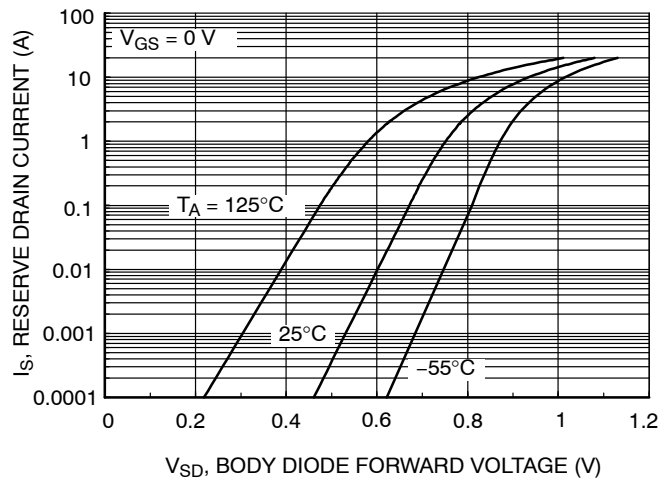


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) (continued)

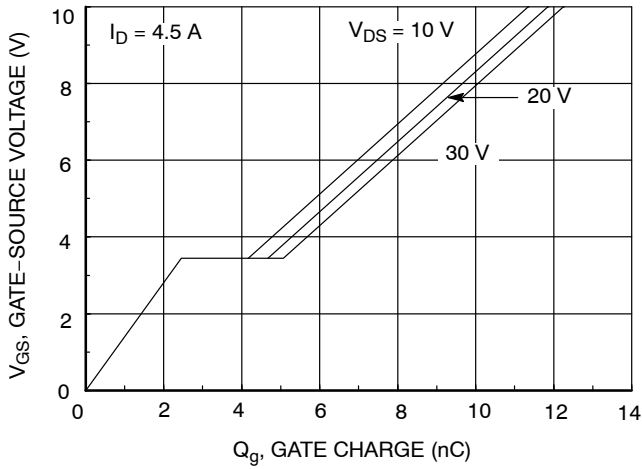


Figure 17. Gate Charge Characteristics

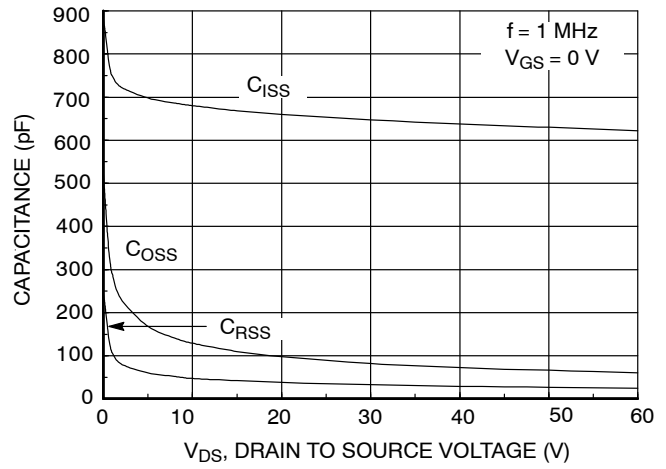


Figure 18. Capacitance Characteristics

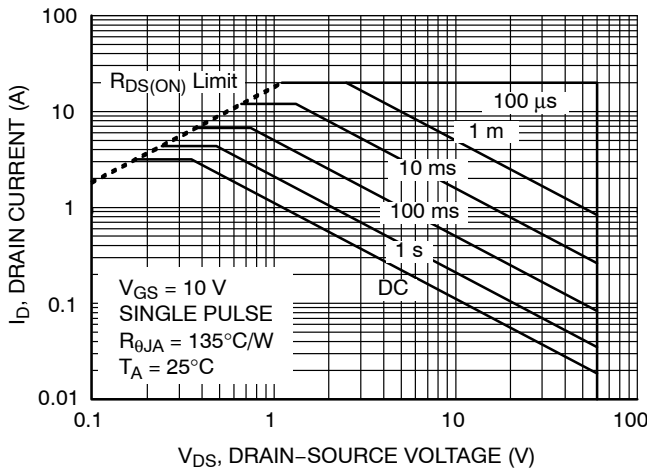


Figure 19. Maximum Safe Operating Area

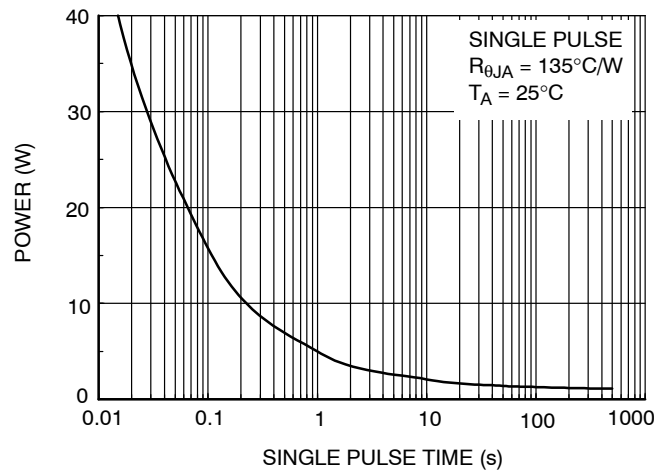


Figure 20. Single Pulse Maximum Power Dissipation

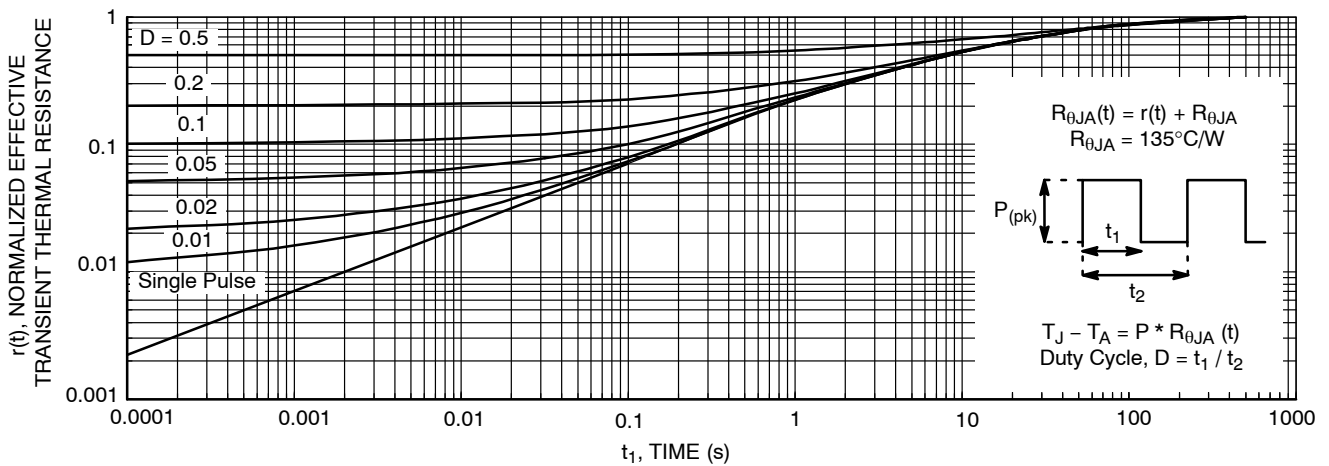


Figure 21. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

POWERTRENCH is a registered trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

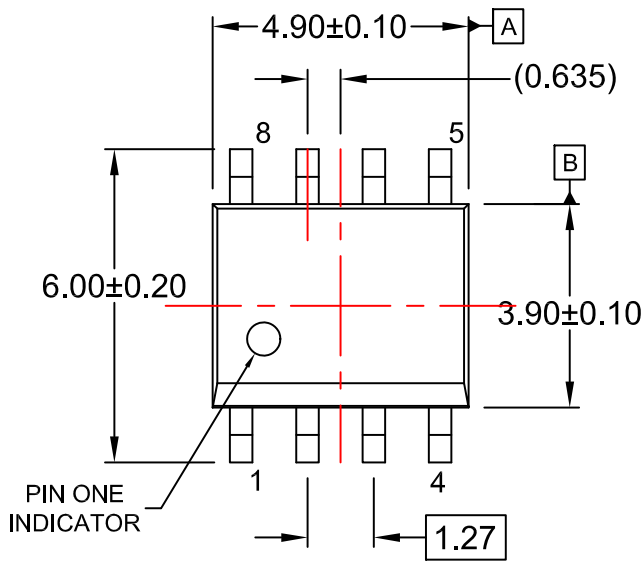
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

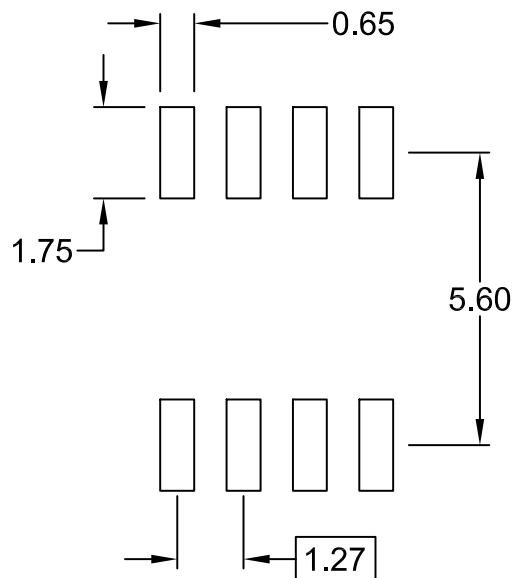


SOIC8
CASE 751EB
ISSUE A

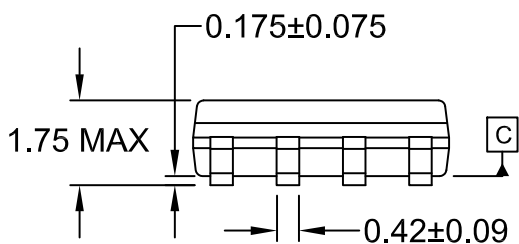
DATE 24 AUG 2017



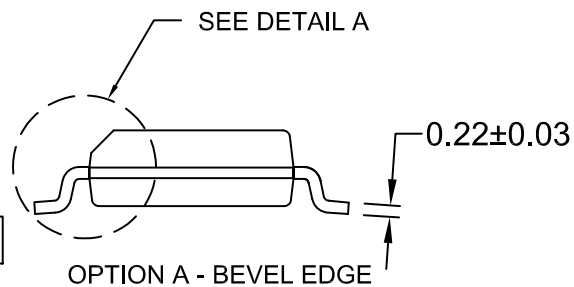
\varnothing 0.25 (M) C B A



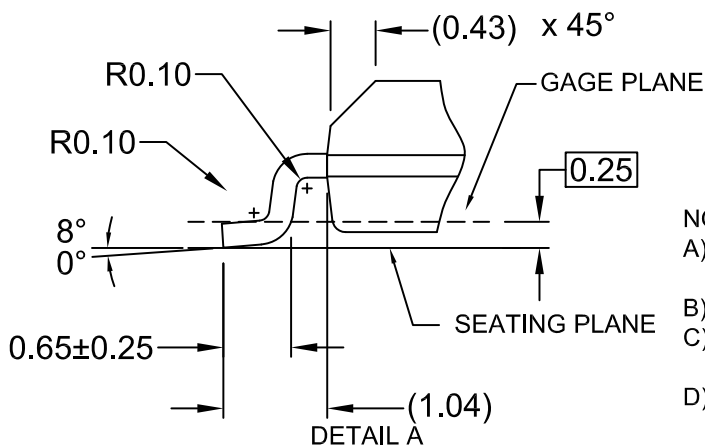
LAND PATTERN RECOMMENDATION



$\frac{1}{2}$ 0.10



OPTION B - NO BEVEL EDGE



SCALE: 2:1

NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

DOCUMENT NUMBER:	98AON13735G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC8	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

