



ON Semiconductor®

FDS8958B

Dual N & P-Channel PowerTrench® MOSFET

Q1-N-Channel: 30 V, 6.4 A, 26 mΩ Q2-P-Channel: -30 V, -4.5 A, 51 mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 26 mΩ at $V_{GS} = 10$ V, $I_D = 6.4$ A
- Max $r_{DS(on)}$ = 39 mΩ at $V_{GS} = 4.5$ V, $I_D = 5.2$ A

Q2: P-Channel

- Max $r_{DS(on)}$ = 51 mΩ at $V_{GS} = -10$ V, $I_D = -4.5$ A
- Max $r_{DS(on)}$ = 80 mΩ at $V_{GS} = -4.5$ V, $I_D = -3.3$ A
- HBM ESD protection level > 3.5 kV (Note 3)
- RoHS Compliant

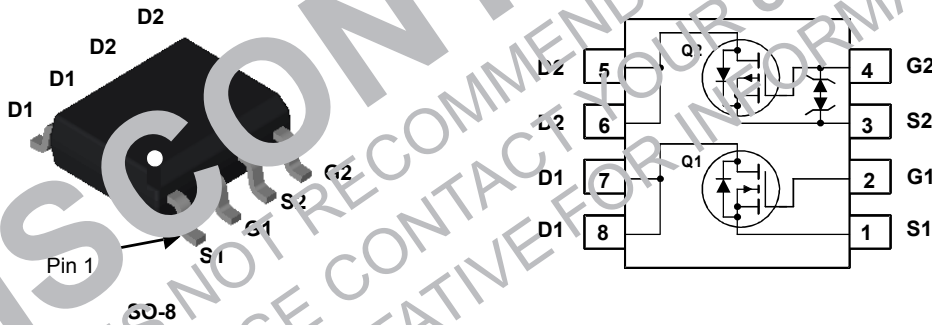
General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance all yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low on-state power loss and fast switching are required.

Applications

- DC-DC Conversion
- Battery and motor drive inverter



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	30	-30	V
V_{GS}	Gate to Source Voltage	± 20	± 25	V
I_D	Drain Current - Continuous	6.4	-4.5	A
	- Pulsed	30	-30	
P_D	Power Dissipation for Dual Operation	2.0		W
	Power Dissipation for Single Operation	$T_A = 25^\circ\text{C}$ (Note 1a)		
		$T_A = 25^\circ\text{C}$ (Note 1b)		
E_{AS}	Single Pulse Avalanche Energy	18	5	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	78	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS8958B	FDS8958B	SO-8	13"	12 mm	2500 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$ $I_D = -250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	Q1 Q2	30 -30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ $I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		24 -21		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2			1 -1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = \pm 25\text{ V}, V_{DS} = 0\text{ V}$	Q1 Q2			± 100 ± 10	nA μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$ $V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	Q1 Q2	1.0 -1.0	2.0 1.9	3.0 -3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ $I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 6.4\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 5.2\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 6.4\text{ A}, T_J = 25$ $V_{GS} = -10\text{ V}, I_D = -6.4\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -5.2\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -6.4\text{ A}, T_J = 125\text{ }^\circ\text{C}$	Q1 Q2		21 29 31 38 60 53	26 39 39 51 80 72	m Ω
g_{FS}	Forward Transconductance	$V_{DD} = 5\text{ V}, I_D = 6.4\text{ A}$ $V_{GS} = -5\text{ V}, I_D = -4.5\text{ A}$	Q1 Q2		20 10		S

Dynamic Characteristics

C_{iss}	Input Capacitance	Q1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1 Q2		405 570	540 760	pF
C_{oss}	Output Capacitance	Q2	Q1 Q2		75 115	100 155	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1 Q2		55 100	80 150	pF
R_g	Gate Resistance		Q1 Q2		2.4 4.4		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 15\text{ V}, I_D = 6.4\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$	Q1 Q2		4.3 6.0	10 12	ns
t_r	Rise Time		Q1 Q2		2.0 6.0	10 12	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = -15\text{ V}, I_D = -4.5\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\text{ }\Omega$	Q1 Q2		12 17	22 30	ns
t_f	Fall Time		Q1 Q2		2.0 7.0	10 14	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}$ $V_{GS} = -10\text{ V}$	Q1 Q2		8.3 14	12 19	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 4.5\text{ V}$ $V_{GS} = -4.5\text{ V}$	Q1 Q2	$V_{DD} = 15\text{ V},$ $I_D = 6.4\text{ A}$	4.1 7.0	5.8 9.6	nC
Q_{gs}	Gate to Source Charge		Q1 Q2		1.3 1.9		nC
Q_{gd}	Gate to Drain "Miller" Charge		Q1 Q2	$V_{DD} = -15\text{ V},$ $I_D = -4.5\text{ A}$	1.7 3.6		nC

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)	Q1		0.8	1.2	V
		$V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)	Q2		-0.8	-1.2	
t_{rr}	Reverse Recovery Time	Q1 $I_F = 6.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1		17	30	ns
			Q2		20	36	
Q_{rr}	Reverse Recovery Charge	Q2 $I_F = -4.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1		6	12	nC
			Q2		8	16	

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78 °C/W when mounted on a 1 in² pad of 2 oz copper



b) 135 °C/W when mounted on a minimum pad

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection against V_{SD} . No gate overvoltage rating is implied.

4. UIL condition: Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1\text{ mH}$, $I_{AS} = 6\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 0\text{ V}$. (Q1)
Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1\text{ mH}$, $I_{AS} = -4\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 0\text{ V}$. (Q2)

DISCONTINUED

THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN

PLEASE CONTACT YOUR onsemi REPRESENTATIVE FOR INFORMATION

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

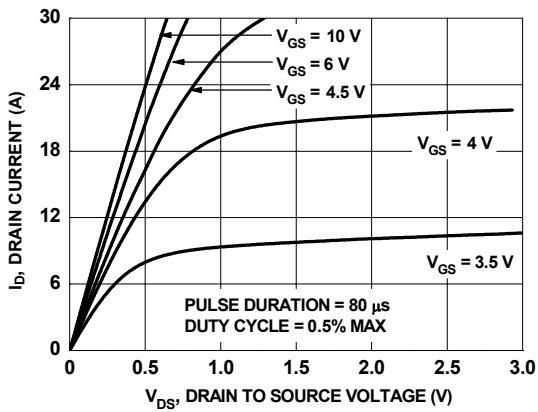


Figure 1. On Region Characteristics

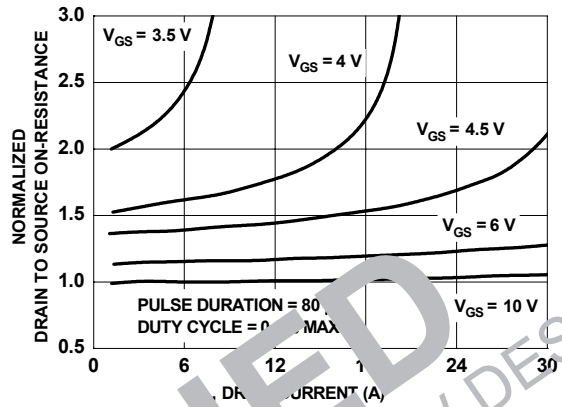


Figure 2. Normalized On-Resistance Drain Current and Gate Voltage

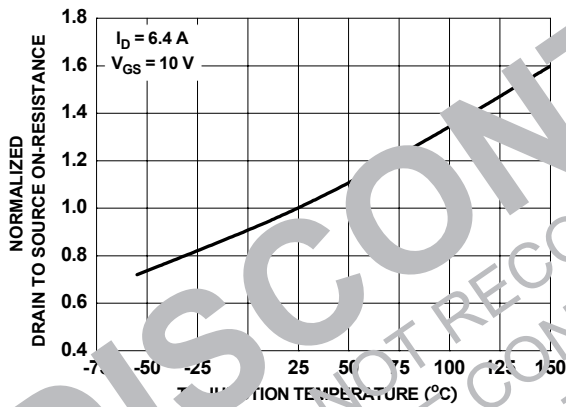


Figure 3. Normalized On-Resistance vs Junction Temperature

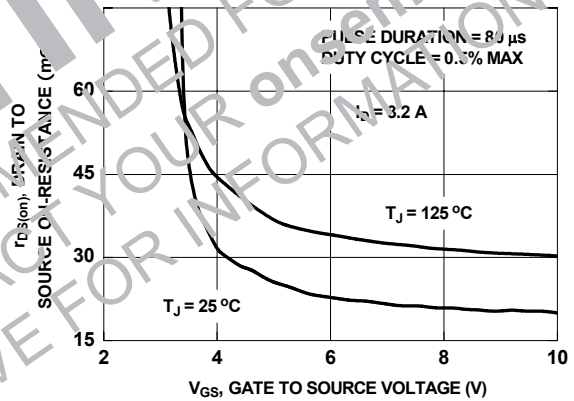


Figure 4. On-Resistance vs Gate to Source Voltage

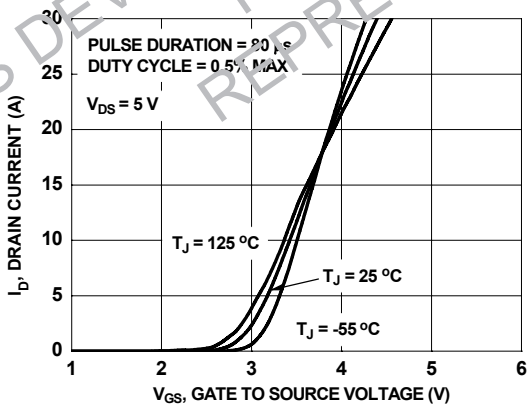


Figure 5. Transfer Characteristics

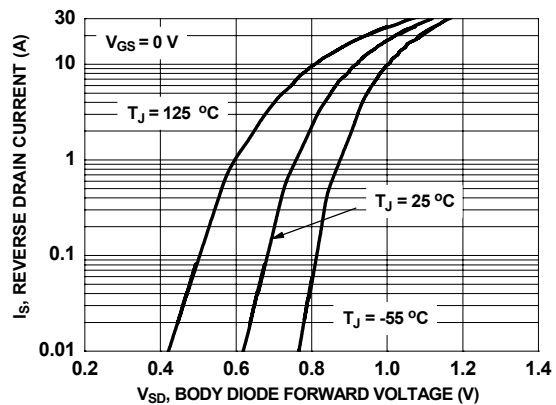


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

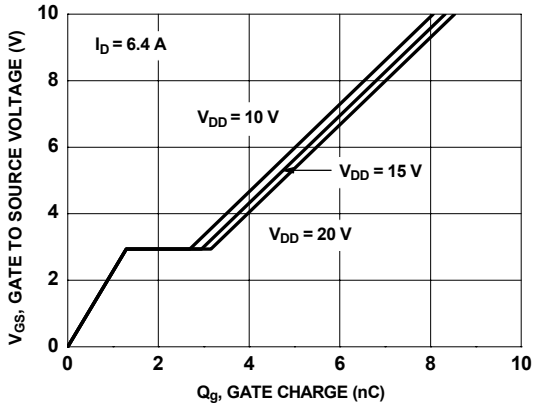


Figure 7. Gate Charge Characteristics

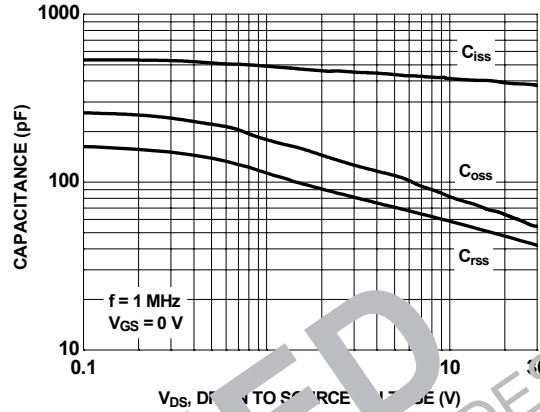


Figure 8. Capacitance vs Drain to Source Voltage

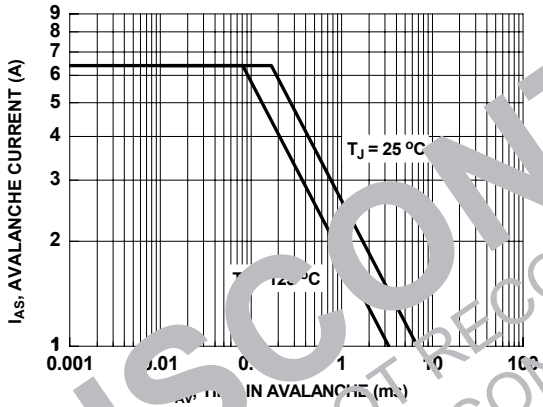


Figure 9. Unclamped Inductive Switching Capability

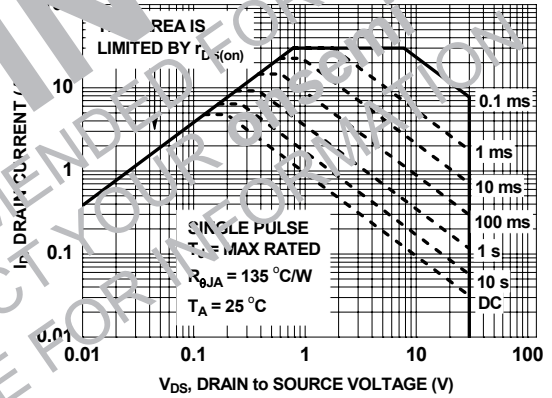


Figure 10. Forward Bias Safe Operating Area

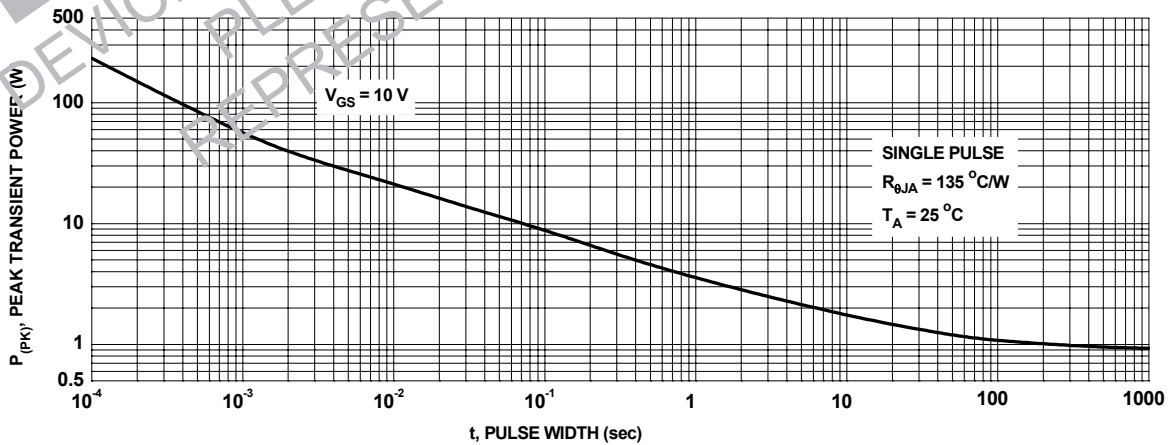


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

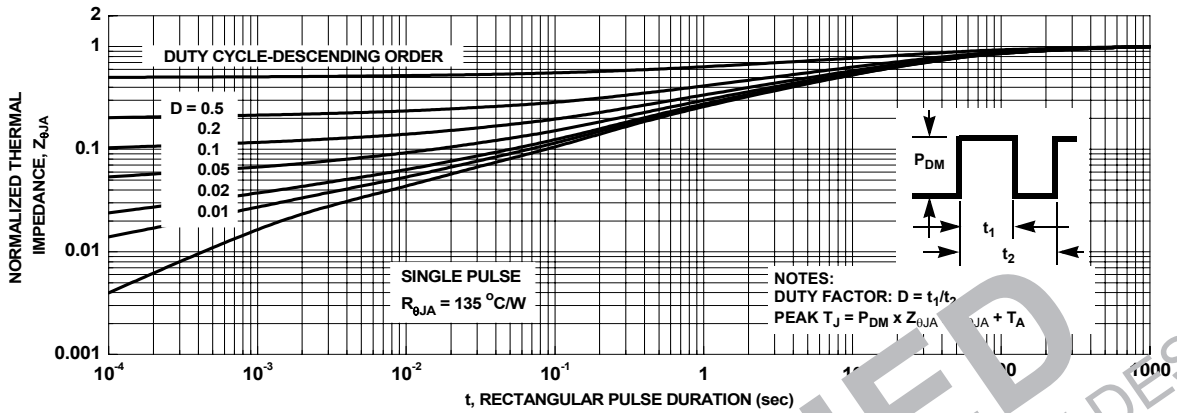


Figure 12. Junction-to-Ambient Transient Thermal Response Curves

DISCONTINUED
 THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
 PLEASE CONTACT YOUR onsemi
 REPRESENTATIVE FOR INFORMATION

Typical Characteristics (Q2 P-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

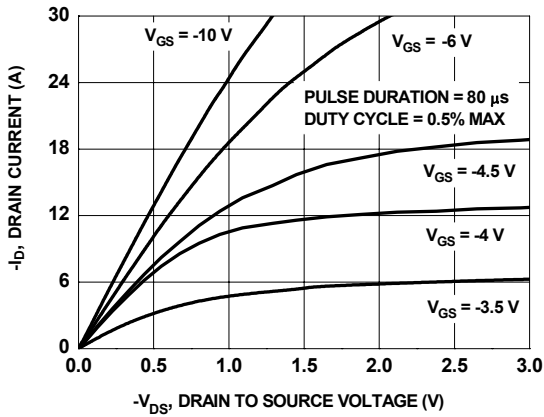


Figure 15. On-Region Characteristics

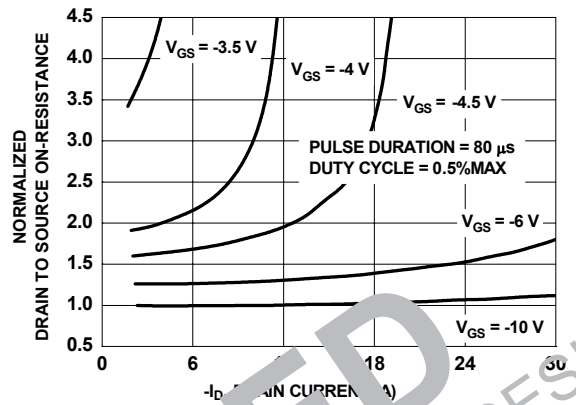


Figure 16. Normalized on-resistance vs Drain Current and Gate Voltage

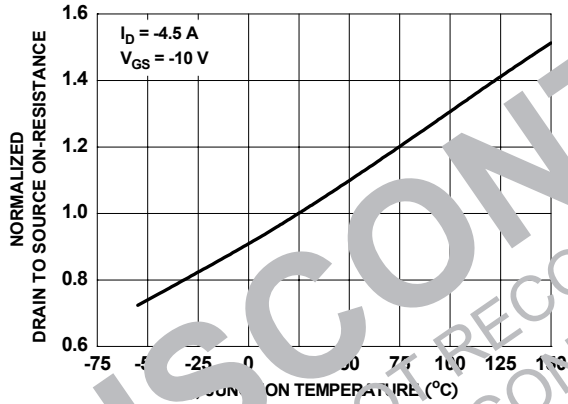


Figure 17. Normalized On-Resistance vs Junction Temperature

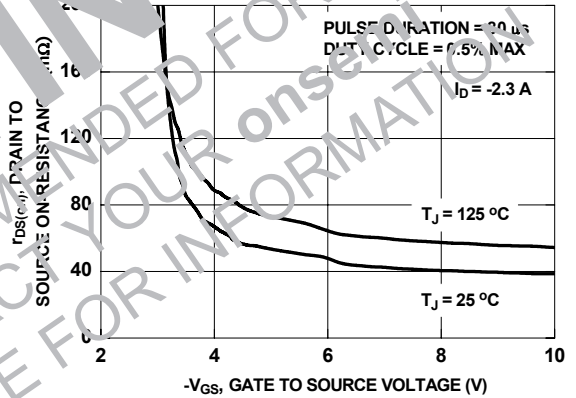


Figure 18. On-Resistance vs Gate to Source Voltage

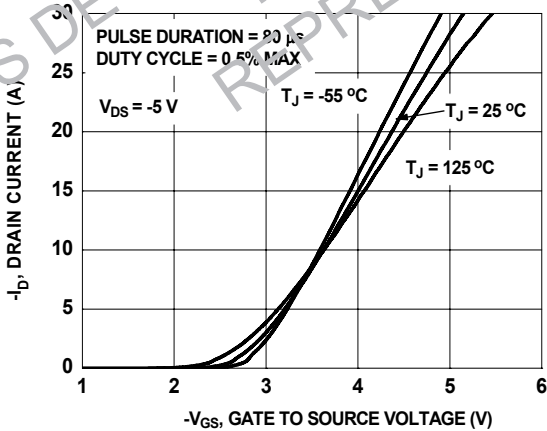


Figure 19. Transfer Characteristics

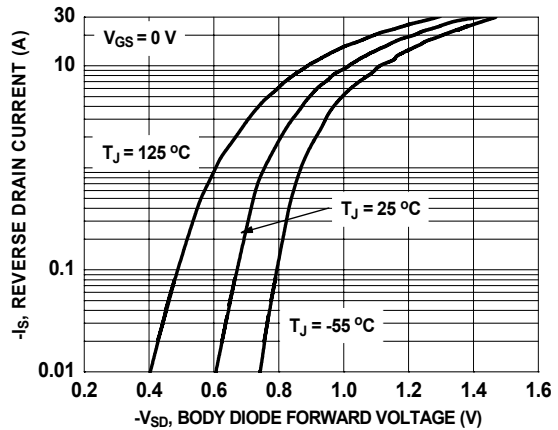


Figure 20. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

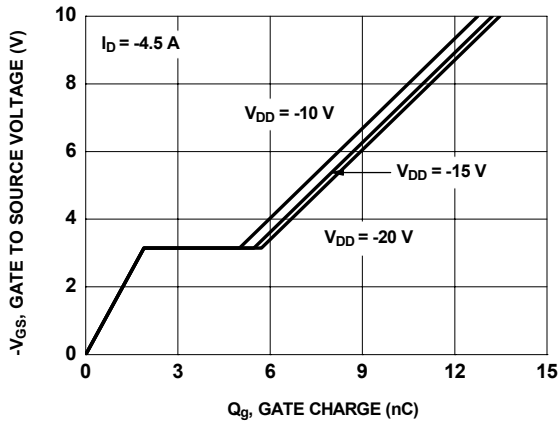


Figure 21. Gate Charge Characteristics

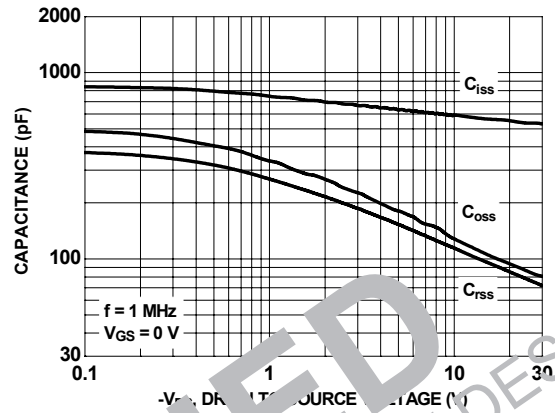


Figure 22. Capacitance vs Drain to Source Voltage

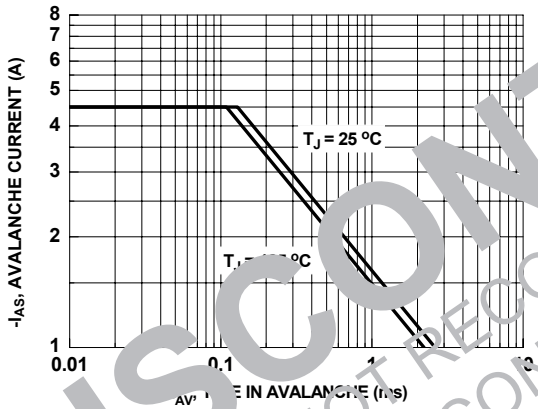


Figure 23. Unclamped Inductive Switching Capability

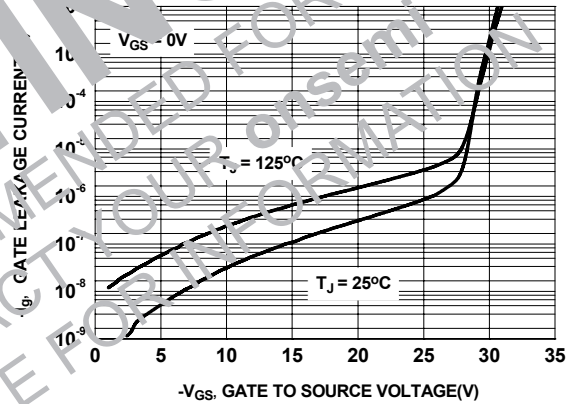


Figure 24. I_g vs V_{gs}

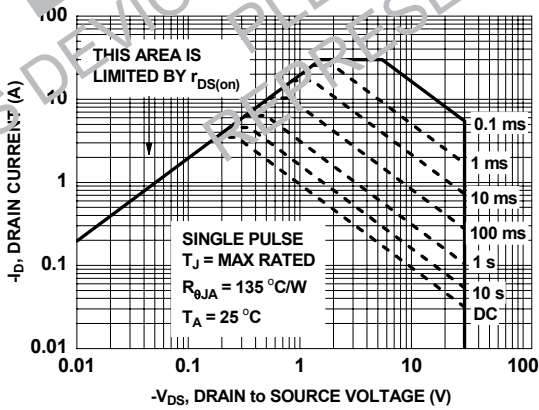


Figure 25. Forward Bias Safe Operating Area

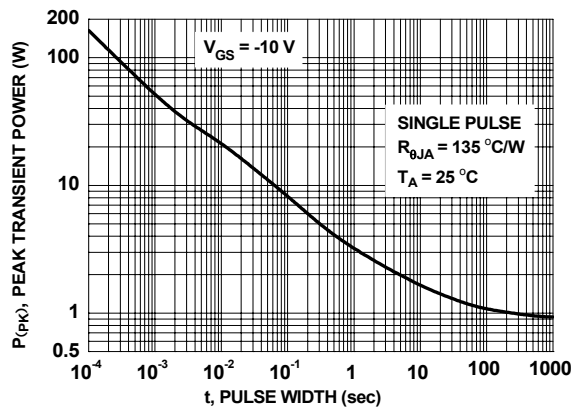


Figure 26. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

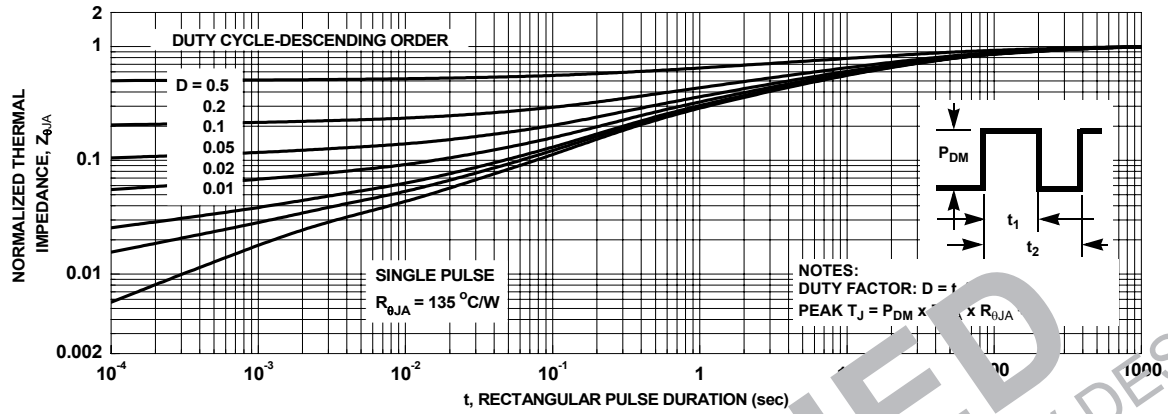


Figure 27. Junction-to-Ambient Transient Thermal Response Curve

DISCONTINUED
 THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
 PLEASE CONTACT YOUR onsemi
 REPRESENTATIVE FOR INFORMATION

Physical Dimensions

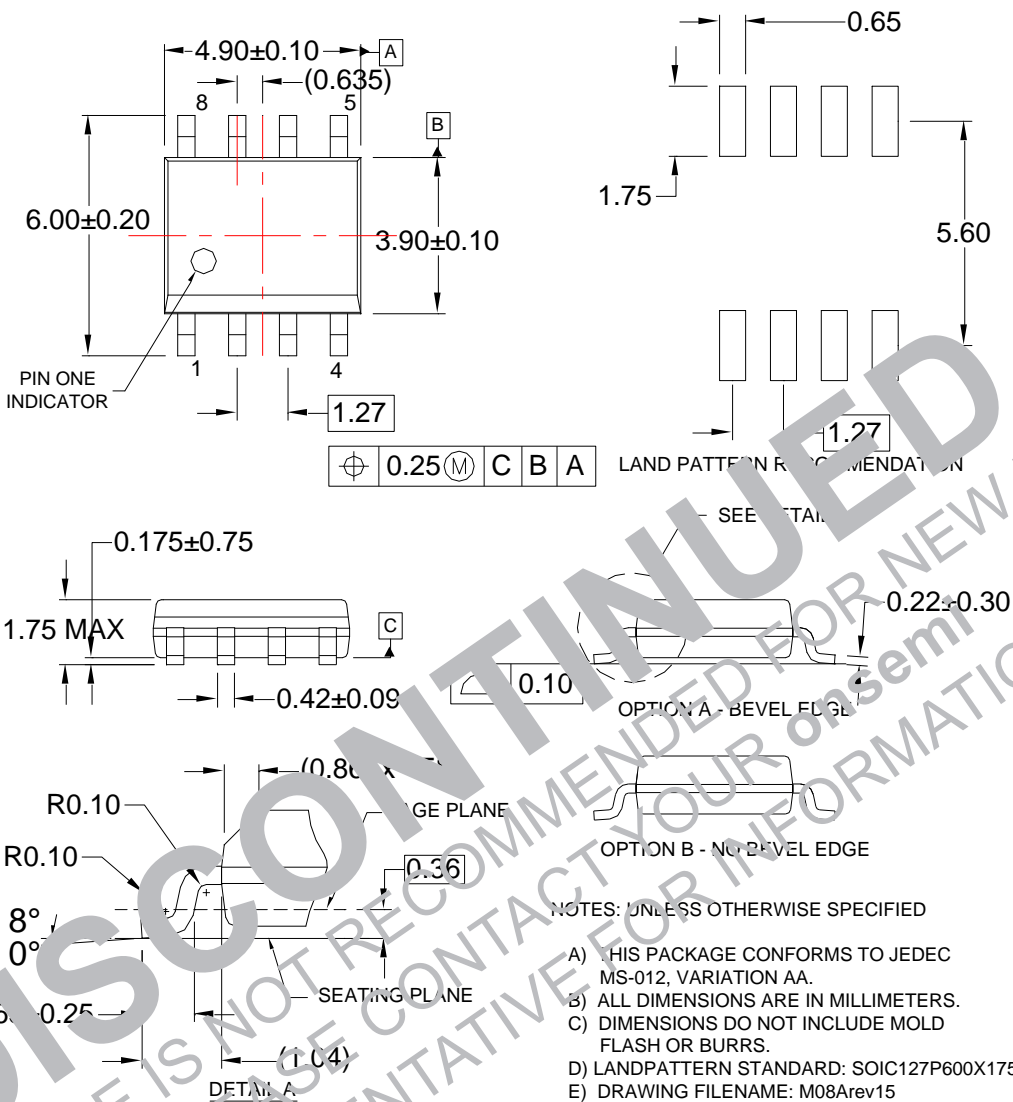



Figure 16 9-Lead, SOIC, JEDEC MS-012, .150-inch Narrow Body

Package drawings are provided as a service to customers considering ON Semiconductor components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a ON Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of ON Semiconductor's worldwide terms and conditions, specifically the warranty therein, which covers ON Semiconductor products.

DISCONTINUED

THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative