

# MOSFET – Power, Dual P-Channel

**-40 V, -20 A, 12.5 mΩ**

## FDWS9520L-F085

### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low QG and Capacitance to Minimize Driver Losses
- Wettable Flanks for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		$V_{DS}$	-40	V
Gate-to-Source Voltage		$V_{GS}$	$\pm 16$	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	-60.8	A
		$T_C = 100^\circ\text{C}$	-43.0	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	75	W
		$T_C = 100^\circ\text{C}$	37.5	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_C = 25^\circ\text{C}$	-12.2	A
		$T_C = 100^\circ\text{C}$	-8.6	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	Steady State	$T_C = 25^\circ\text{C}$	3.0	W
		$T_C = 100^\circ\text{C}$	1.5	
Pulsed Drain Current	$T_C = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	-281	A
Operating Junction and Storage Temperature		$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)		$I_S$	-20	A
Single Pulse Drain-to-Source Avalanche Energy ( $I_L(pk) = -19$ )		$E_{AS}$	90	mJ
Lead Temperature for Soldering Purposes (1/83 from case for 10 s)		$T_L$	260	$^\circ\text{C}$

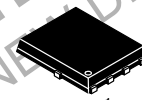
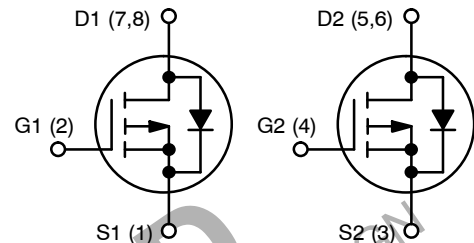
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	2	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
-40 V	12.5 mΩ @ -10 V	-20 A
	19.5 mΩ @ -4.5 V	



**PQFN8 5x6, 1.27P  
CASE 483BL**

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 3 of this data sheet.

# FDWS9520L-F085

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### Off Characteristics

Drain to Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			21		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -40 V	T <sub>J</sub> = 25°C		-1	μA
			T <sub>J</sub> = 175°C		-1	mA
Zero Gate Voltage Drain Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±16 V			±100	nA

### On Characteristics (Note 4)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-1	-1.8	-3	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			-5.5		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V	I <sub>D</sub> = -20 A	10.4	12.5	mΩ
		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -10 A	14.6	19.5	

### Charges, Capacitances & Gate Resistance

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = -20 V		2370		pF
Output Capacitance	C <sub>oss</sub>			940		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			40		pF
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> = 0.5 V, f = 1 MHz		17		Ω
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = -10 V, V <sub>DS</sub> = -32 V; I <sub>D</sub> = -20 A		33		nC
		V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -32 V; I <sub>D</sub> = -20 A		13		
Threshold Gate Charge	Q <sub>g(th)</sub>	V <sub>GS</sub> = 0 to -1 V		2		
Gate to Source Gate Charge	Q <sub>gs</sub>	V <sub>DD</sub> = -20 V, I <sub>D</sub> = -20 A		7		
Gate to Drain "Miller" Charge	Q <sub>gd</sub>			4		
Plateau Voltage	V <sub>GP</sub>			-4		V

### Switching Characteristics

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>DD</sub> = -20 V, I <sub>D</sub> = -20 A, V <sub>GS</sub> = -10 V, R <sub>GEN</sub> = 6 Ω		8		ns
Turn-On Rise Time	t <sub>r</sub>			21		ns
Turn-Off Delay Time	t <sub>d(OFF)</sub>			120		ns
Turn-Off Fall Time	t <sub>f</sub>			34		ns

### Drain-Source Diode Characteristics

Source to Drain Diode Voltage	V <sub>SD</sub>	I <sub>SD</sub> = -20 A, V <sub>GS</sub> = 0 V		-0.9	-1.25	V
		I <sub>SD</sub> = -10 A, V <sub>GS</sub> = 0 V		-0.83	-1.2	V
Reverse Recovery Time	T <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>SD</sub> /dt = 100 A/us, I <sub>S</sub> = -20 A		46		ns
Charge Time	t <sub>a</sub>			22		
Discharge Time	t <sub>b</sub>			24		
Reverse Recovery Charge	Q <sub>RR</sub>			37		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%

5. Switching characteristics are independent of operating junction temperatures.

# FDWS9520L-F085

## ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
FDWS9520L-F085	FDWS9520L	PQFN8 5x6, 12.7P (Pb-Free, Halogen Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

**DISCONTINUED**  
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN  
PLEASE CONTACT YOUR onsemi  
REPRESENTATIVE FOR INFORMATION

TYPICAL CHARACTERISTICS

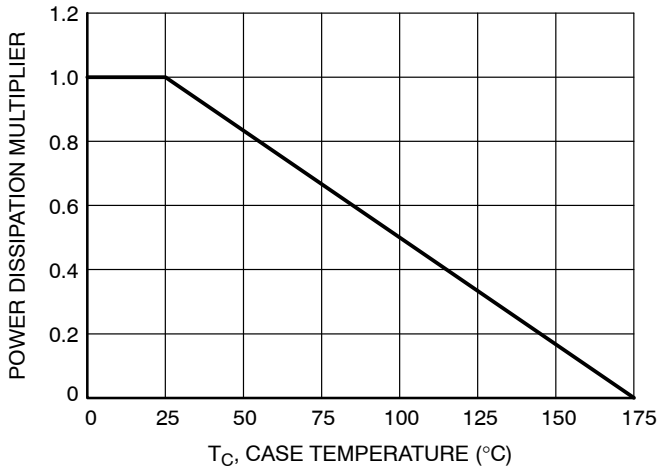


Figure 1. Normalized Power Dissipation vs. Case Temperature

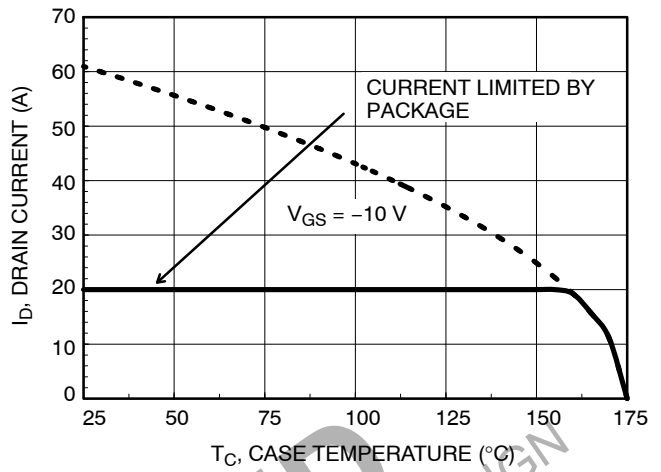


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

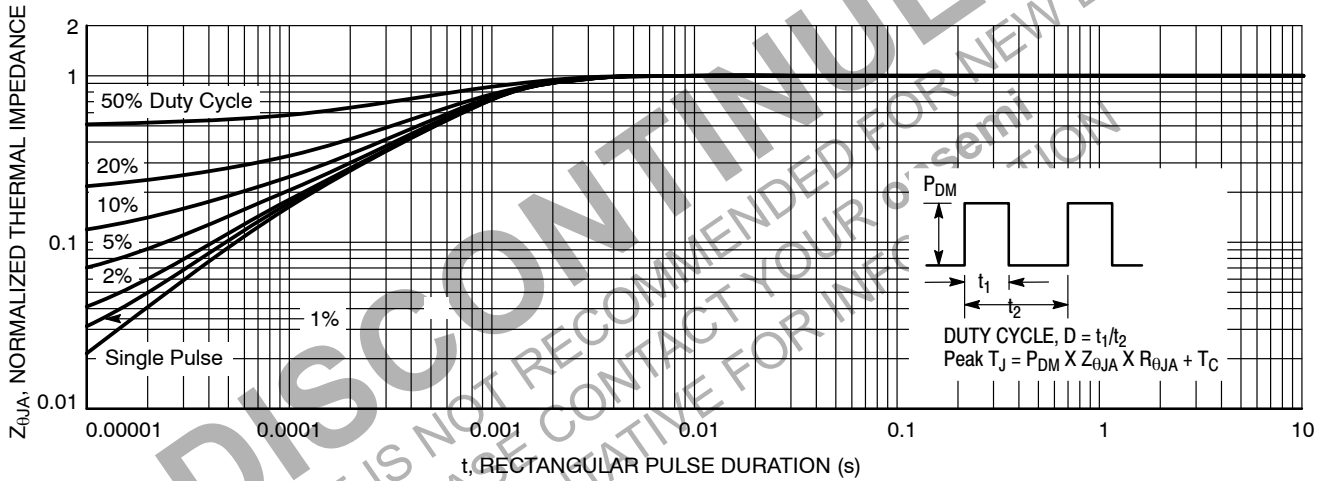


Figure 3. Normalized Maximum Transient Thermal Impedance

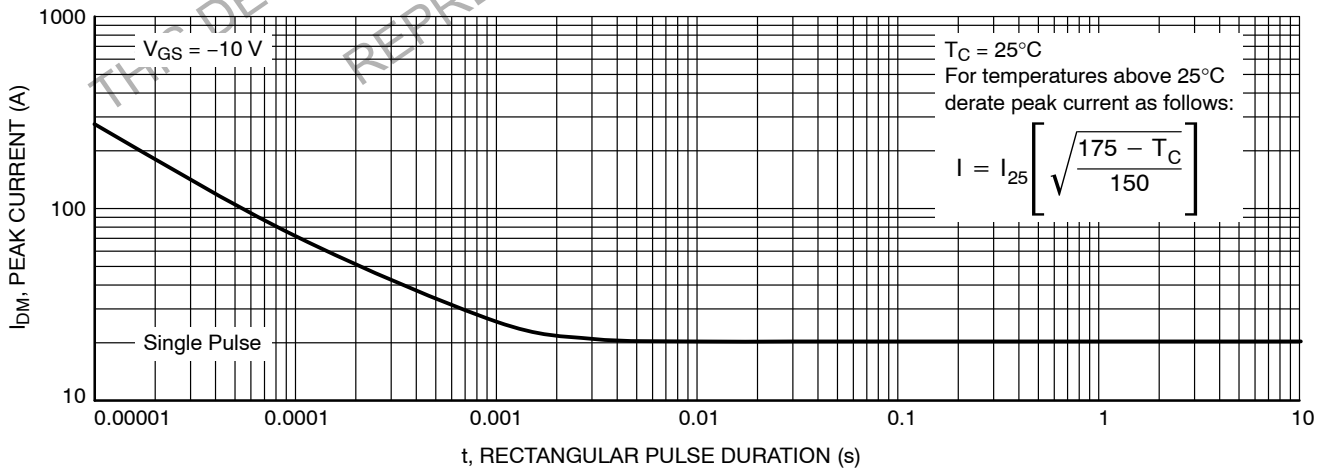


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

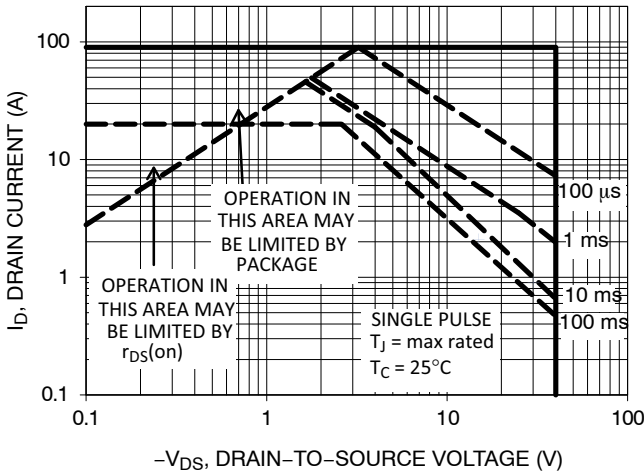


Figure 5. Forward Bias Safe Operating Area

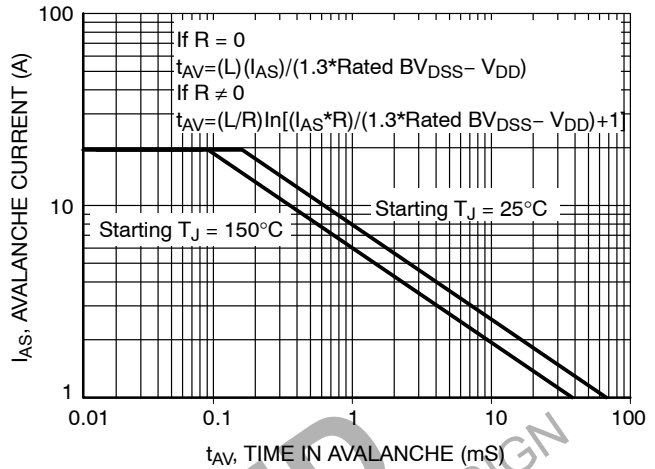


Figure 6. Unclamped Inductive Switching Capability

(Note: Refer to onsemi Applications Notes [AN7514](#) and [AN7515](#))

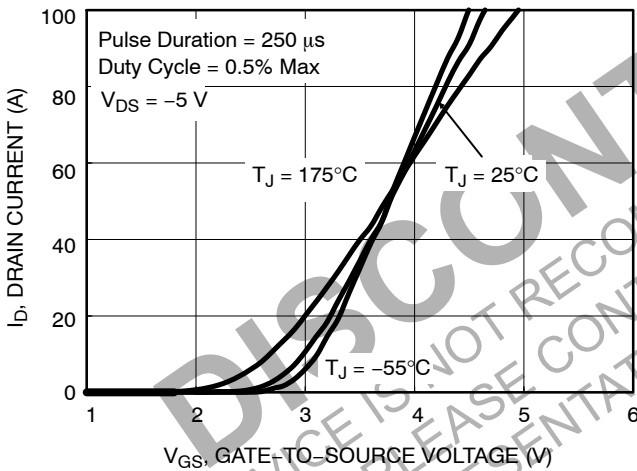


Figure 7. Transfer Characteristics

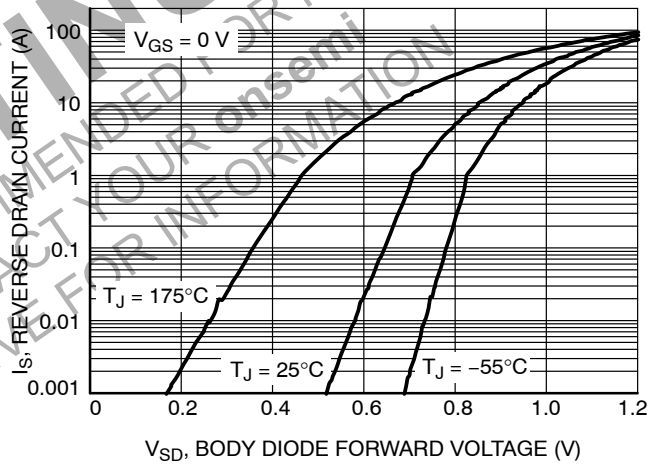


Figure 8. Forward Diode Characteristics

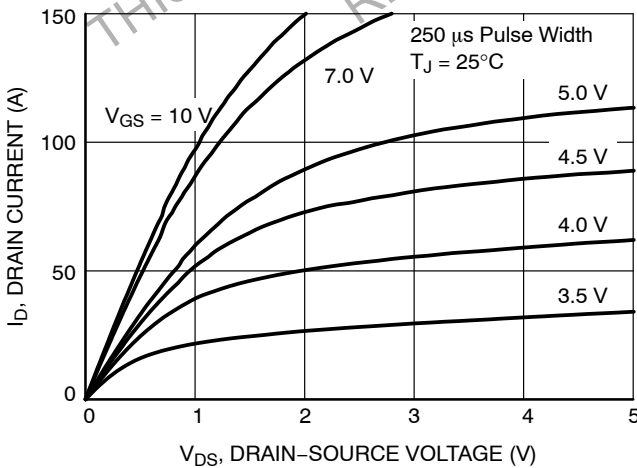


Figure 9. Saturation Characteristics

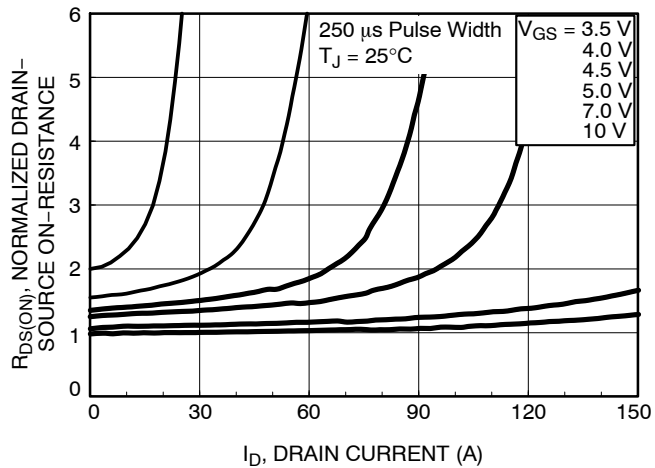


Figure 10. Normalized  $R_{DS(on)}$  vs. Drain Current

TYPICAL CHARACTERISTICS

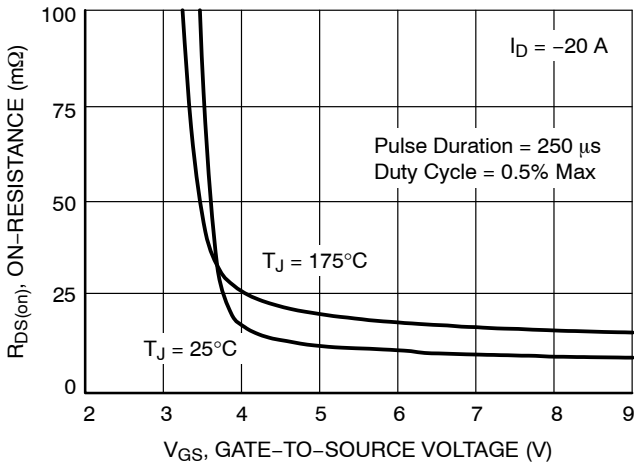


Figure 11.  $R_{DS(on)}$  vs. Gate Voltage

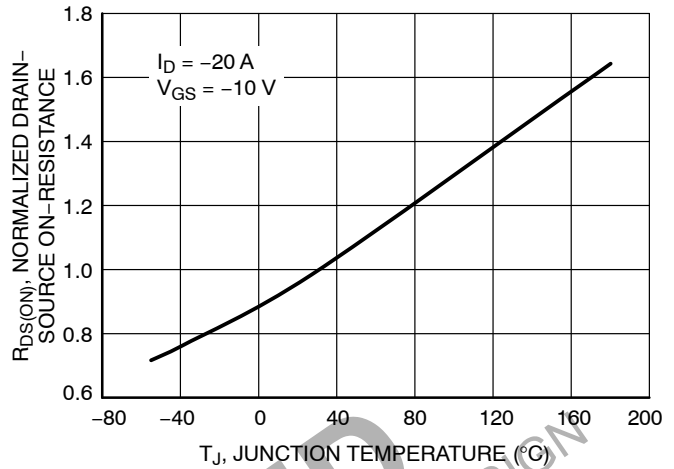


Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature

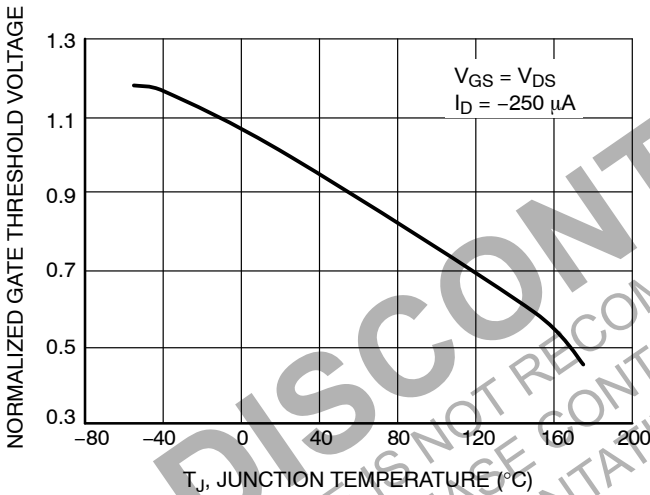


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

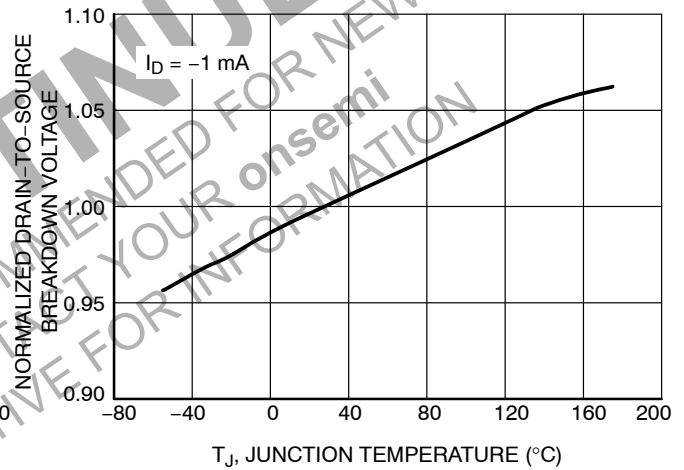


Figure 14. Normalized Drain-to-Source Breakdown Voltage vs. Junction Temperature

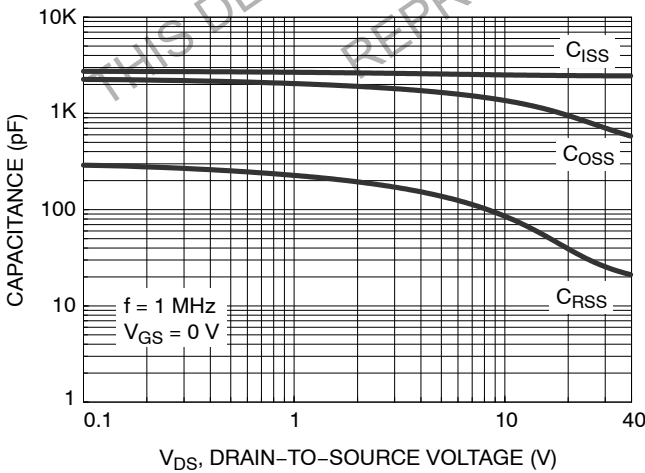


Figure 15. Capacitance vs. Drain-to-Source Voltage

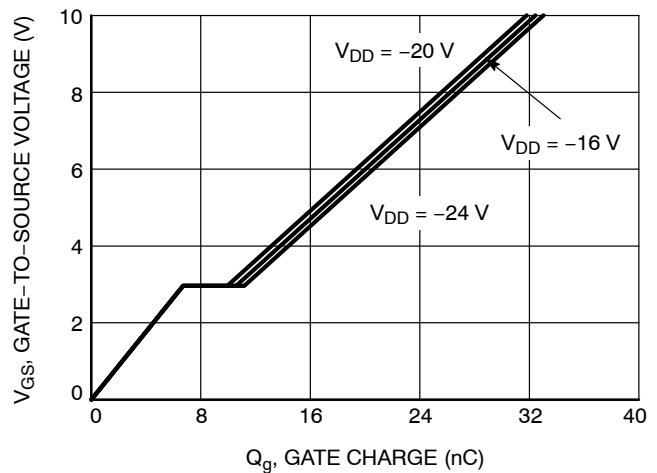
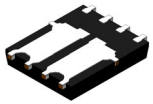


Figure 16. Gate Charge vs. Gate-to-Source Voltage

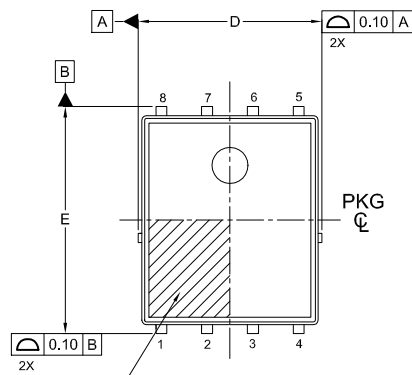


**PQFN8 5X6, 1.27P**  
**CASE 483BL**  
**ISSUE A**

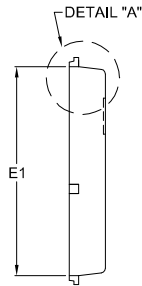
DATE 23 APR 2021

NOTES:

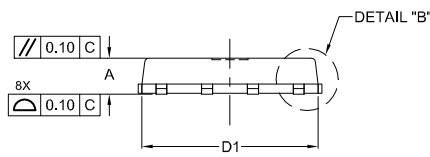
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



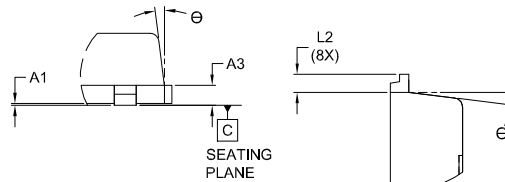
TOP VIEW



SIDE VIEW

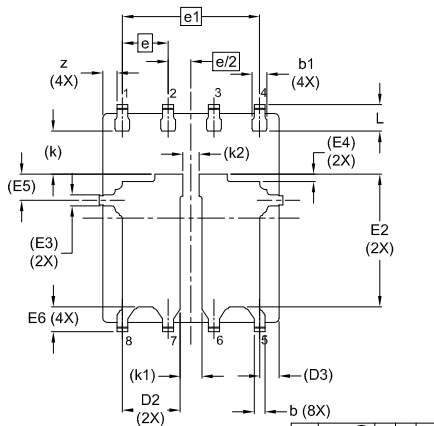


FRONT VIEW

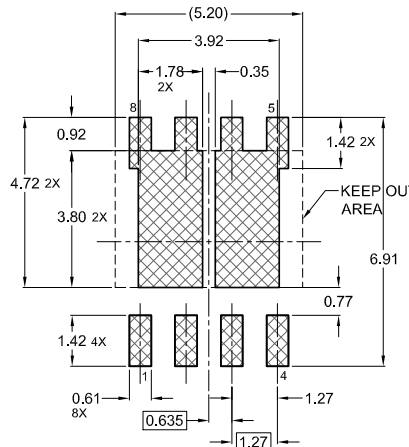


DETAIL "B"

DETAIL "A"



BOTTOM VIEW



LAND PATTERN  
RECOMMENDATION

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.23	0.28	0.33
b	0.26	0.31	0.36
b1	0.36	0.41	0.46
D	5.00	5.10	5.20
D1	4.80	4.90	5.00
D2	1.51	1.61	1.71
D3	0.54 REF		
E	6.20	6.30	6.40
E1	5.70	5.80	5.90
E2	3.58	3.68	3.78
E3	0.30 REF		
E4	0.10	0.20	0.30
E5	0.72 REF		
E6	0.59	0.69	0.79
e	1.27 BSC		
e1	3.81 BSC		
e/2	0.635 BSC		
k	1.19 REF		
k1	0.60 REF		
k2	0.45 REF		
L	0.64	0.74	0.84
L2	0.15	0.25	0.35
z	0.39 REF		
θ	0°	-	7°

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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