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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

January 2007

FDY3000NZ

Dual N-Channel 2.5V Specified PowerTrench® MOSFET

General Description

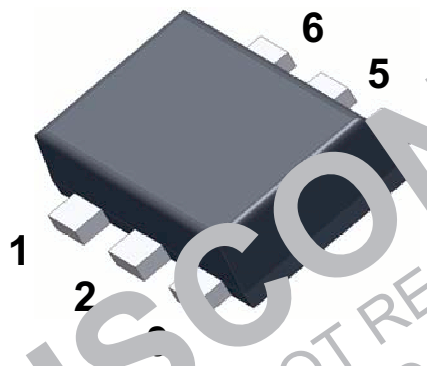
This Dual N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench process to optimize the $R_{DS(ON)}$ @ V_{GS} = 2.5v.

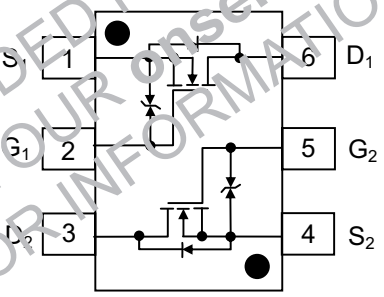
Applications

- Li-Ion Battery Pack

Features

- 600 mA, 20 V $R_{DS(ON)}$ = 700 m[illegible] @ V_{GS} [illegible] 4.5 V
  $R_{DS(ON)}$ = [illegible] m[illegible] @ V_{GS} = [illegible].5 V
- ESD protection diode [illegible]
- RoHS Co[illegible]pliant





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		± 12	V
I_D	Drain Current – Continuous	(Note 1a)	600	mA
	– Pulsed		1000	
P_D	Power Dissipation (Steady State)	(Note 1a)	625	mW
		(Note 1b)	446	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	200	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	280	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
C	FDY3000NZ	7 ”	8 mm	3000 units

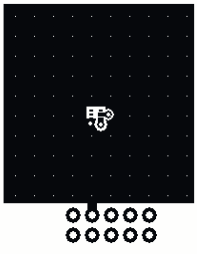
Electrical Characteristics

T_A = 25°C unless otherwise noted

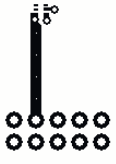
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		14		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate–Body Leakage,	V_{GS} = ± 12 V, V_{DS} = 0 V			± 10	μA
		V_{GS} = ± 4.5 V, V_{DS} = 0 V			± 1	μA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.6	1.0	1.3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		-3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 4.5 V, I_D = 600 mA		0.5	0.70	Ω
		V_{GS} = 2.5 V, I_D = 500 mA		0.37	0.55	
		V_{GS} = 1.8 V, I_D = 150 mA		0.73	1.25	
		V_{GS} = 4.5 V, I_D=600 mA, T_J = 125		0.35	1.00	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 600 mA		1.8		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V,		69		pF
C_{oss}	Output Capacitance	f = 1.0 MHz		20		pF
C_{rss}	Reverse Transfer Capacitance			10		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 10 V, I_D = 1 A		6	12	ns
t_r	Turn–On Rise Time	V_{GS} = 4.5 V, R_{GEN} = 6 Ω		8	16	ns
$t_{d(off)}$	Turn–Off Delay Time			8	16	ns
t_f	Turn–Off Fall Time			2.4	4.8	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 600 mA,		0.8	1.1	nC
Q_{gs}	Gate–Source Charge	V_{GS} = 4.5 V		0.16		nC
Q_{gd}	Gate–Drain Charge			0.26		nC
Drain–Source Diode Characteristics and Maximum Ratings						
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 150 mA (Note 2)		0.7	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 600 mA,		8		nS
Q_{rr}	Diode Reverse Recovery Charge	dI_F/dt = 100 A/μs		1		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design



a) 200°C/W when mounted on a 1in² pad of 2 oz copper



b) 280°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection againts ESD. No gate overvoltage rating is implied.

Typical Characteristics

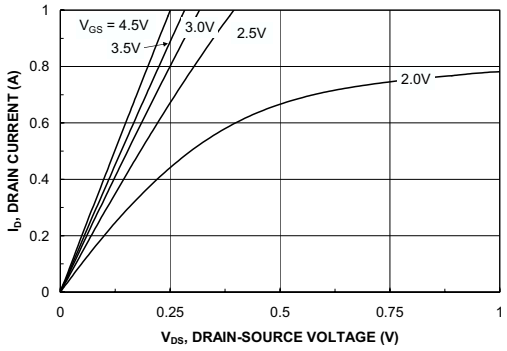


Figure 1. On-Region Characteristics.

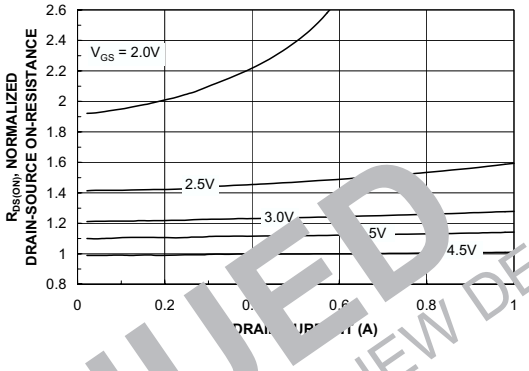


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

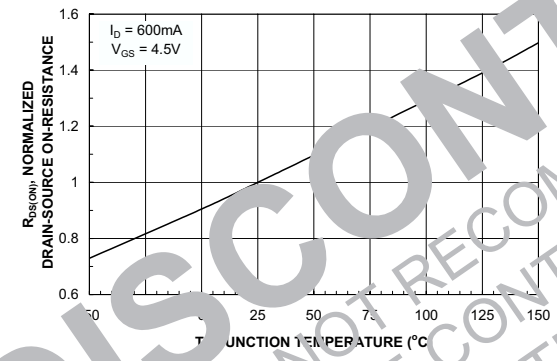


Figure 3. On-Resistance Variation with Temperature.

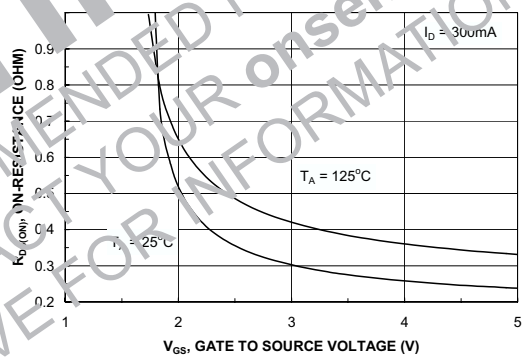


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

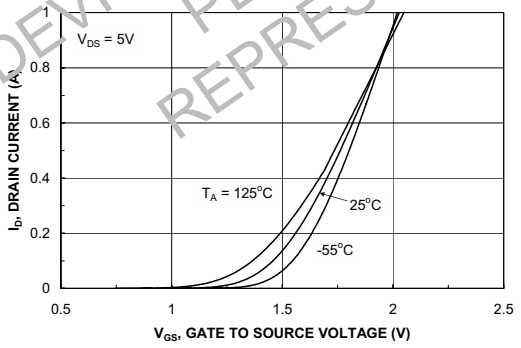


Figure 5. Transfer Characteristics.

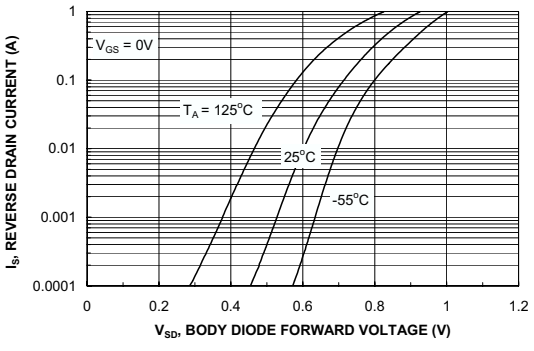


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

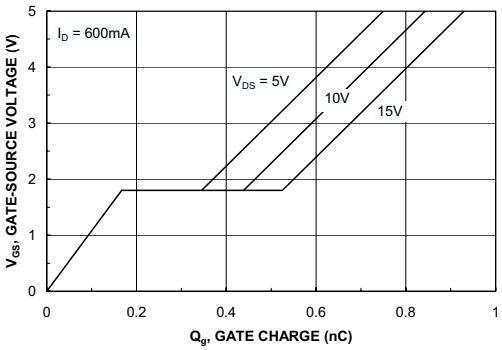


Figure 7. Gate Charge Characteristics.

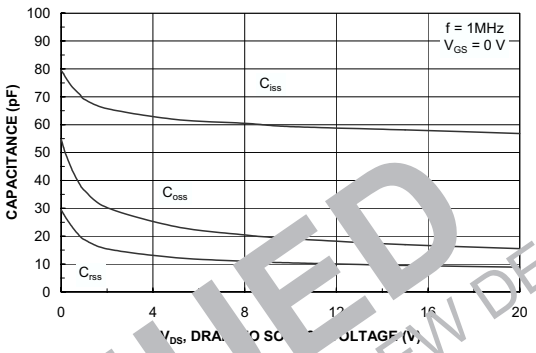


Figure 8. Capacitance Characteristics.

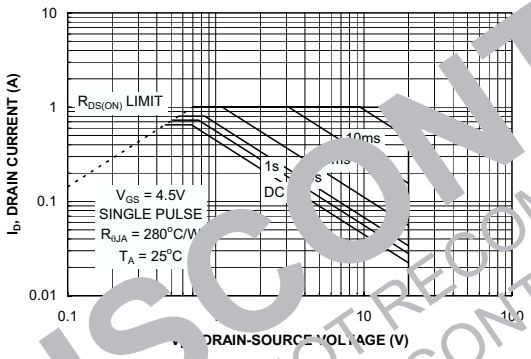


Figure 9. Maximum Safe Operating Area.

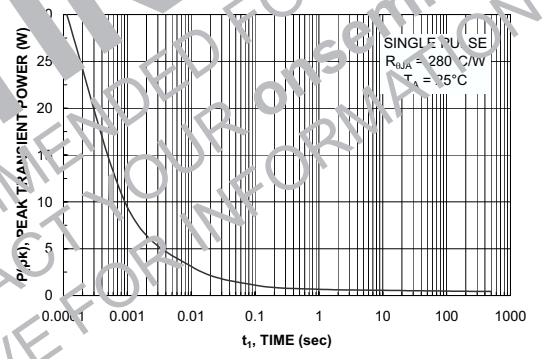


Figure 10. Single Pulse Maximum Power Dissipation.

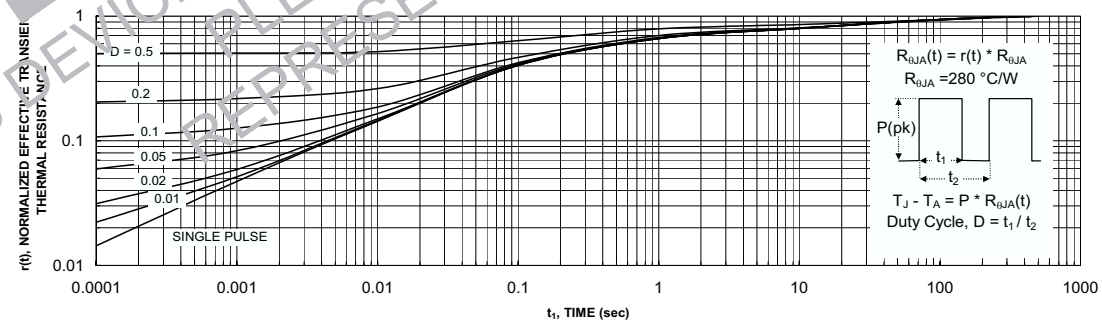
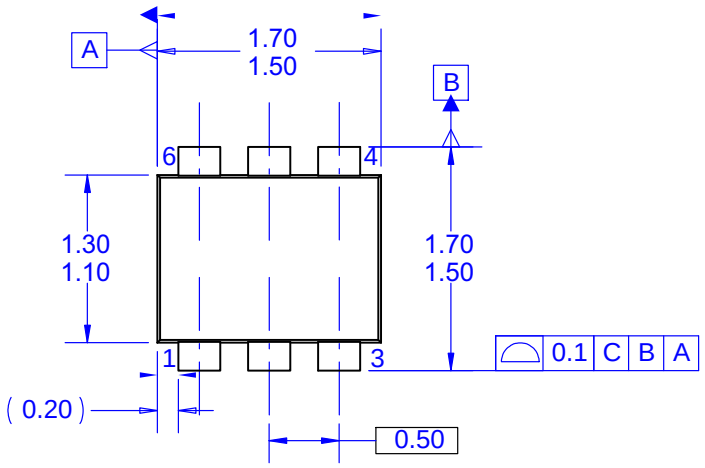


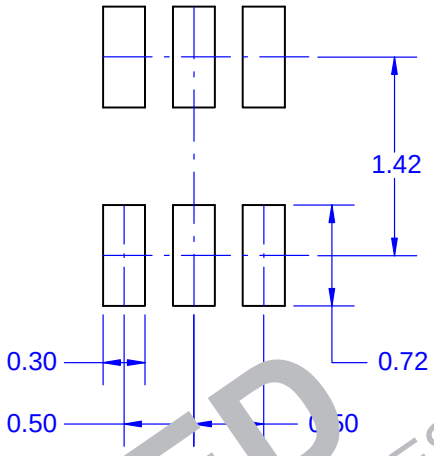
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

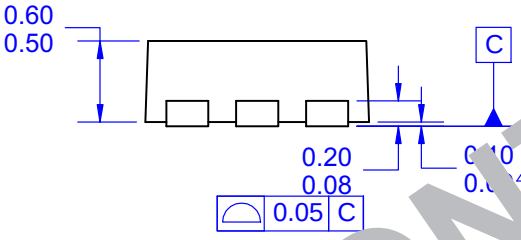
SOT−563
CASE 419BH
ISSUE O

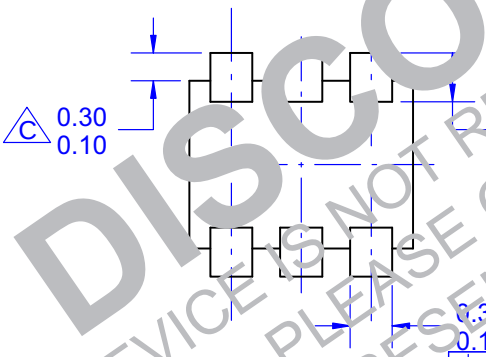


TOP VIEW



LAND PATTERN
RECOMMENDATION





BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED.
A. REFERENCE TO JEDEC MO293.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DOES NOT COMPLY JEDEC STANDARD VALUE
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSION.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5−2009.
F. LANDPATTERN RECOMMENDATION GENERATEI WITH IPC LANDPATTERN GENERATOR

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