

# **MOSFET** - N-Channel, QFET

# 150 V, 70 A, 28 m $\Omega$

# **FQA70N15**

### Description

This N-Channel enhancement mode power MOSFET is produced using **onsemi**'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

#### **Features**

- 70 A, 100 V,  $R_{DS(on)} = 28 \text{ m}\Omega \text{ (Max)} @ V_{GS} = 10 \text{ V},$  $I_D = 35 \text{ A}$
- Low Gate Charge (Typ. 135 nC)
- Low Crss (Typ. 135 pF)
- 100% Avalanche Tested
- This is a Pb-Free Device

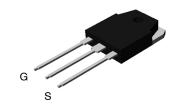
### **ABSOLUTE MAXIMUM RATINGS**

(T<sub>C</sub> = 25°C unless otherwise noted)

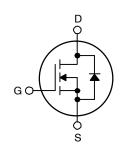
Symbol	Parameter	FQA70N15	Unit
V <sub>DSS</sub>	Drain to Source Voltage	150	V
I <sub>D</sub>	Drain Current Continuous ( $T_C = 25^{\circ}C$ ) Continuous ( $T_C = 100^{\circ}C$ )	70 50	Α
I <sub>DM</sub>	Drain Current – Pulsed (Note 1)	250	Α
$V_{GSS}$	Gate to Source Voltage	±25	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	1000	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	70	Α
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	33	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C) – Derate above 25°C	330 2.2	W W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +175	°C
TL	Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. L = 0.34 mH,  $I_{AS}$  = 70 A,  $V_{DD}$  = 25 V,  $R_{G}$  = 25  $\Omega$ , Starting  $T_{J}$  = 25°C.
- 3.  $I_{SD} \le 70$  A, di/dt  $\le 300$  A/ $\mu$ s,  $V_{DD} \le BV_{DSS}$ , Starting  $T_J = 25$ °C.



TO-3P-3LD / EIAJ SC-65, ISOLATED CASE 340BZ



### **MARKING DIAGRAM**

&Z&3&K FQA 70N15

&Z = Assembly Location

&3 = Date Code (Year and Week)

&K = Lot Code

FQA70N15 = Specific Device Code

### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
FQA70N15	TO-3P (Pb-Free)	450 / Tube

### THERMAL CHARACTERISTICS

Symbol	Parameter	FQA70N15	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max	0.45	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max	40	°C/W

# **ELECTRICAL CHARACTERISTICS** (T<sub>C</sub> = 25°C, unless otherwise noted)

Symbol	Parameter Test Conditions		Min	Тур	Max	Unit
OFF CHAR	ACTERISTIC					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	150	-	-	V
$\Delta BV_{DSS} / \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	-	0.15	-	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V	-	-	1	μΑ
		V <sub>DS</sub> = 120 V, T <sub>C</sub> = 150°C	-	-	10	1
I <sub>GSSF</sub>	Gate to Body Leakage Current, Forward	V <sub>GS</sub> = 25 V, V <sub>DS</sub> = 0 V	-	-	100	nA
I <sub>GSSR</sub>	Gate to Body Leakage Current, Reverse	V <sub>GS</sub> = -25 V, V <sub>DS</sub> = 0 V	-	-	-100	
ON CHARA	CTERISTICS					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	2.0	_	4.0	V
R <sub>DS(on)</sub>	Static Drain to Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 35 A	-	0.023	0.028	Ω
9FS	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 35 A	_	48	-	S
OYNAMIC (	CHARACTERISTICS		-			-
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V,	_	4150	5400	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz	_	840	1100	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1	_	135	175	pF
SWITCHING	G CHARACTERISTICS		-			-
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 75 V, I <sub>D</sub> = 70 A,	_	60	130	ns
t <sub>r</sub>	Turn-On Rise Time	$R_G = 25 \Omega$ (Note 4)	_	420	850	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	1	_	340	690	ns
t <sub>f</sub>	Turn-Off Fall Time	1	_	290	590	ns
Qg	Total Gate Charge	$V_{DS} = 120 \text{ V}, I_D = 70 \text{ A},$ $V_{GS} = 10 \text{ V}$ (Note 4)	_	135	175	nC
Q <sub>gs</sub>	Gate to Source Charge		_	25	-	nC
$Q_{gd}$	Gate to Drain Charge	, , ,	_	65	-	nC
DRAIN-SO	URCE DIODE CHARACTERISTICS AND M	AXIMUM RATINGS				
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	70	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	280	Α
$V_{SD}$	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 70 A	-	-	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 70 A,	-	150	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> /dt = 100 A/μs	_	0.67	-	μС

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

#### **TYPICAL CHARACTERISTICS**

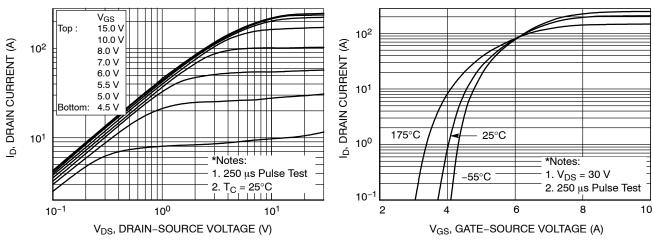


Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics

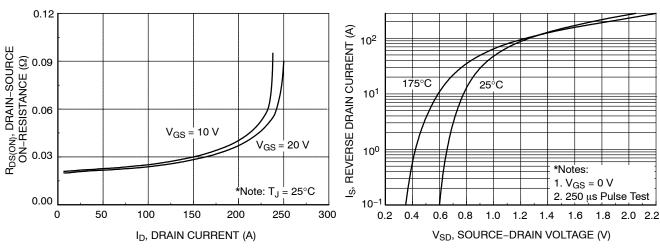


Figure 3. On-Resistance Variation vs. Drain **Current and Gate Voltage** 

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

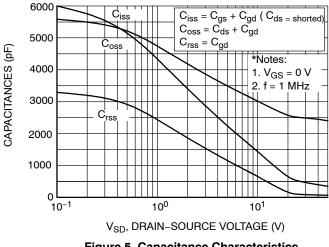


Figure 5. Capacitance Characteristics

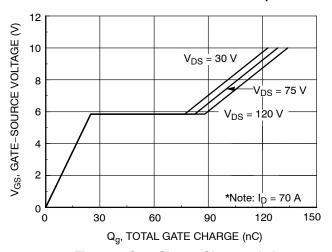


Figure 6. Gate Charge Characteristics

### TYPICAL CHARACTERISTICS (CONTINUED)

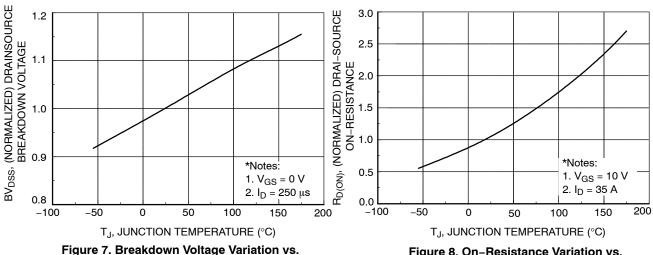


Figure 7. Breakdown Voltage Variation vs.
Temperature

Figure 8. On–Resistance Variation vs.
Temperature

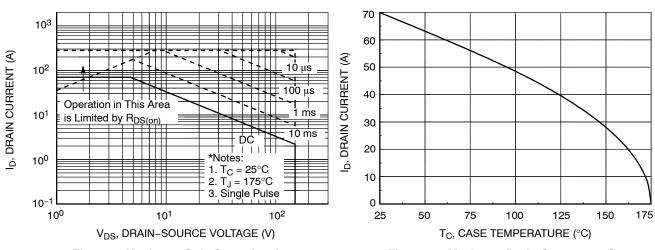


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

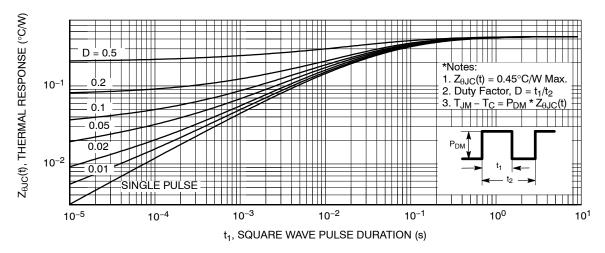


Figure 11. Transient Thermal Response Curve

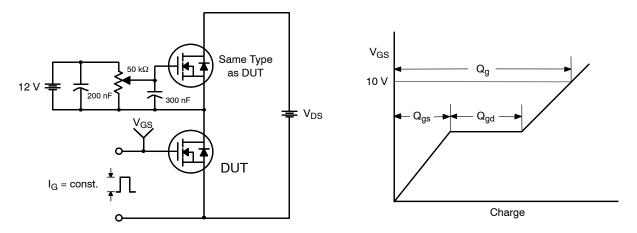


Figure 12. Gate Charge Test Circuit & Waveform

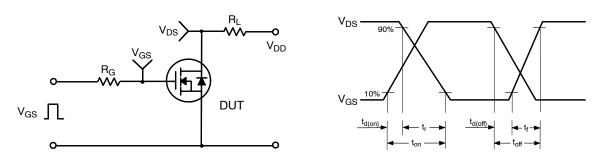


Figure 13. Resistive Switching Test Circuit & Waveforms

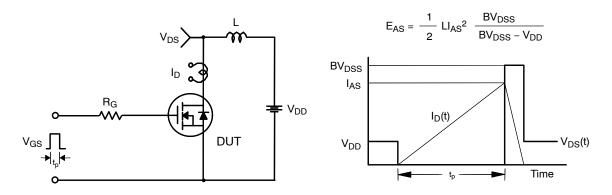
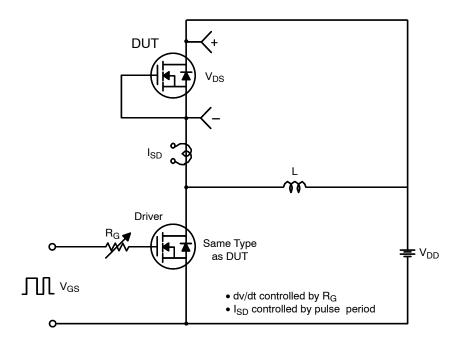


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



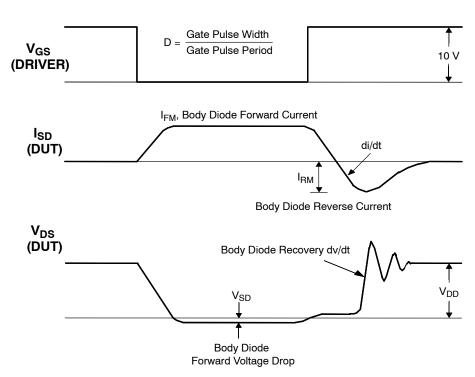
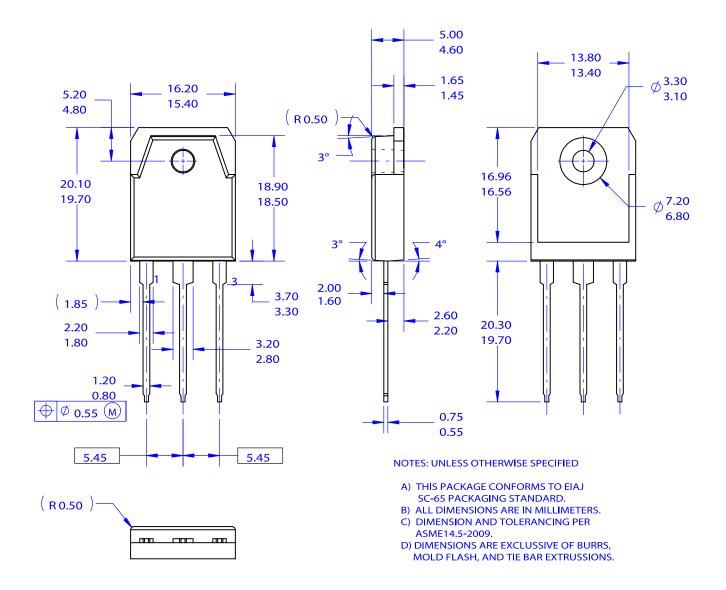


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



### TO-3P-3LD / EIAJ SC-65, ISOLATED CASE 340BZ ISSUE O

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