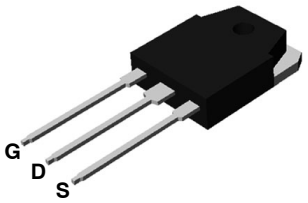
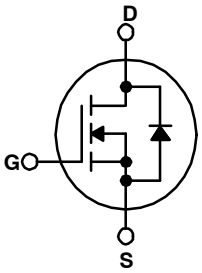
MOSFET – N-Channel QFET

1000 V, 8 A, 1.45 Ω

FQA8N100C



TO−3P−3LD
CASE 340BZ



Description

These N−Channel Enhancement Mode power field effect transistors are produced using **onsemi**'s proprietary, planar stripe, DMOS technology.

This Advanced Technology has been especially tailored to minimize on−state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies.

Features

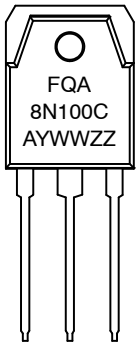
- $R_{DS(on)}$ = 1.45 Ω (Max.) @ V_{GS} = 10 V, I_D = 4 A
- Low Gate Charge (Typ. 53 nC)
- Low Crss (Typ. 16 pF)
- 100% Avalanche Tested
- This Device is Pb−Free Halide, Free and RoHS Compliant

MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted.)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	1000	V
I_D	Drain Current − Continuous (T_C = 25°C) − Continuous (T_C = 100°C)	 8 5	A
I_{DM}	Drain Current − Pulsed (Note 1)	32	A
V_{GSS}	Gate to Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy (Note 2)	850	mJ
I_{AR}	Avalanche Current (Note 1)	8	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	22.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.0	V/ns
P_D	Power Dissipation − (T_C = 25°C) − Derate Above 25°C	 225 1.79	 W W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



FQA8N100C = Specific Device Code
A = Assembly Location
YWW = Date Code (Year & Week)
ZZ = Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping†
FQA8N100C	TO−3P−3LD (Pb−Free)	450 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.56	°C/W
$R_{\theta CS}$	Thermal Resistance, Case−to−Sink, Typ.	0.24	
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient, Max.	40	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	1000	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	1.4	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 1000 V, V_{GS} = 0 V	–	–	10	μA
	Zero Gate Voltage Drain Current	V_{DS} = 800 V, T_C = 125°C	–	–	100	μA
I_{GSSF}	Gate to Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate to Body Leakage Current, Reverse	V_{GS} = −30 V, V_{DS} = 0 V	–	–	−100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 4 A	–	1.2	1.45	Ω
g_{FS}	Forward Transconductance	V_{DS} = 50 V, I_D = 4 A	–	8.0	–	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	–	2475	3220	pF
C_{oss}	Output Capacitance		–	195	255	pF
C_{rss}	Reverse Transfer Capacitance		–	16	24	pF
Switching Characteristics						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 500 V, I_D = 8 A, R_G = 25 Ω (Note 4)	–	50	110	ns
t_r	Turn−On Rise Time		–	95	200	ns
$t_{d(off)}$	Turn−Off Delay Time		–	122	254	ns
t_f	Turn−Off Fall Time		–	80	170	ns
Qg	Total Gate Charge	V_{DS} = 800 V, I_D = 8 A, V_{GS} = 10 V (Note 4)	–	53	70	nC
Qgs	Gate−Source Charge		–	13	–	nC
Qgd	Gate−Drain Charge		–	23	–	nC
Drain−Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	8	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	32	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 8 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 8 A, dI_F/dt = 100 A/μs	–	620	–	ns
Q_{rr}	Reverse Recovery Charge		–	5.2	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. L = 25 mH, I_{AS} = 8 A, V_{DD} = 50 V, R_G = 25 Ω starting T_J = 25°C.
3. I_{SD} ≤ 8 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

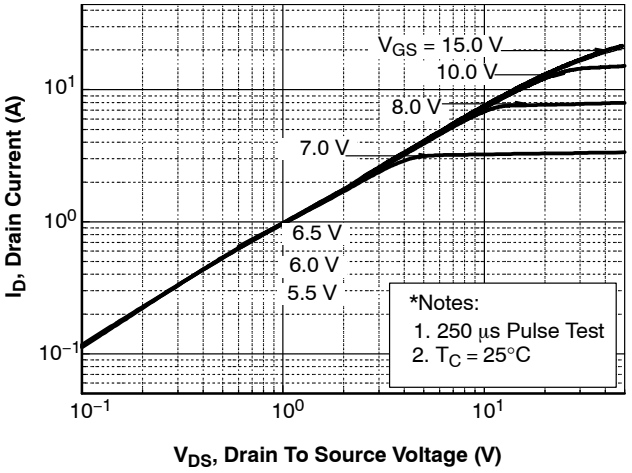


Figure 1. On−Region Characteristics

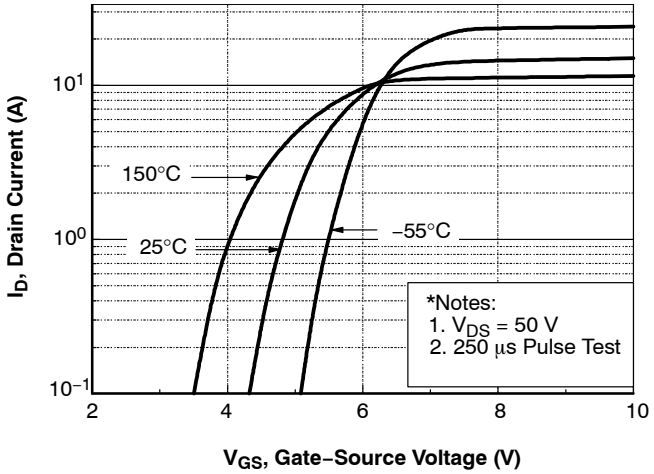


Figure 2. Transfer Characteristics

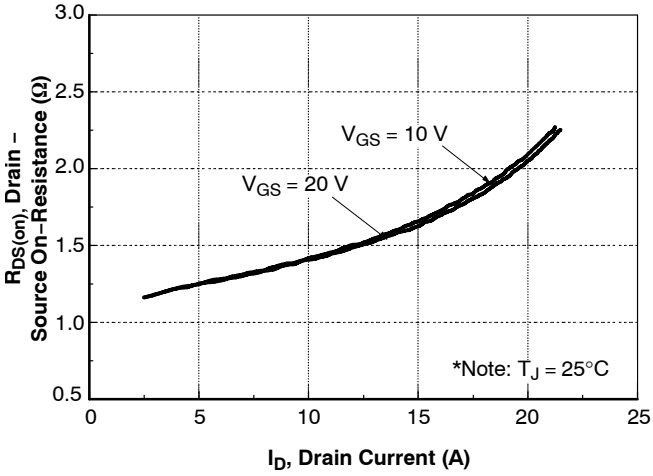


Figure 3. On−Resistance Variation vs Drain Current and Gate Voltage

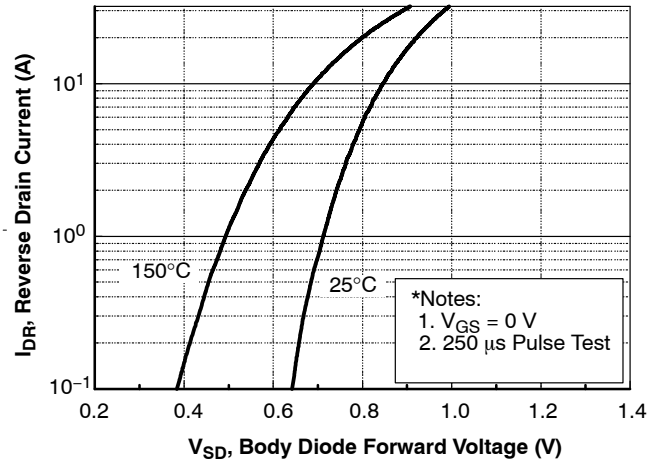


Figure 4. Body Diode Forward Voltage Variation vs Source Current and Temperature

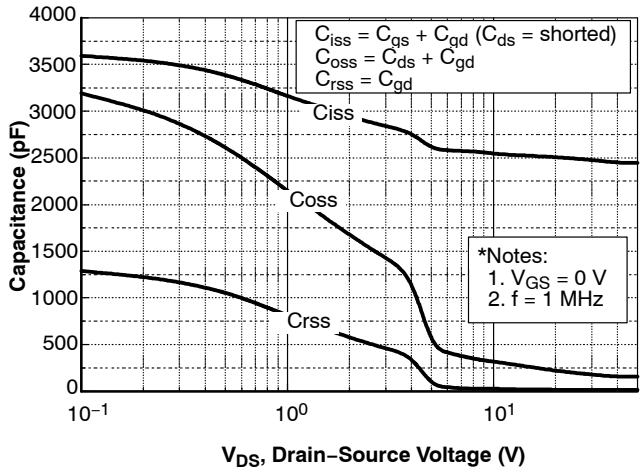


Figure 5. Capacitance Characteristics

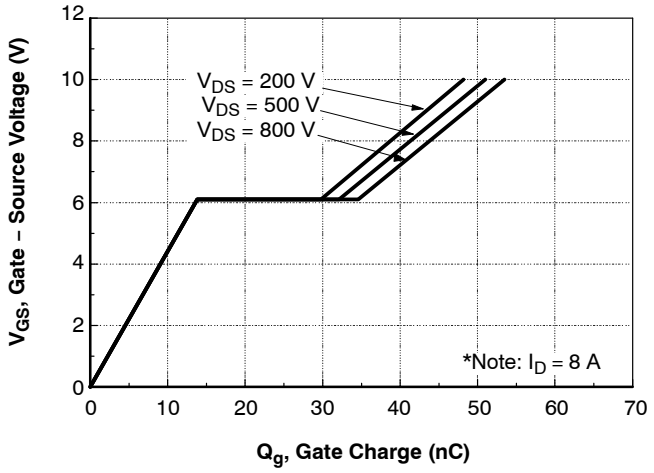


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

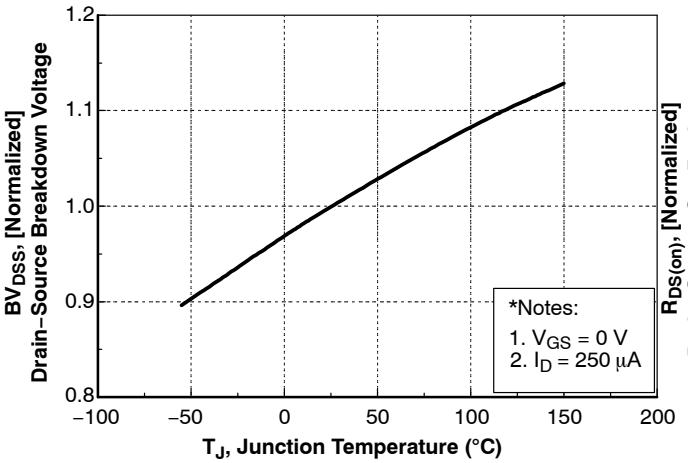


Figure 7. Breakdown Voltage Variation vs Temperature

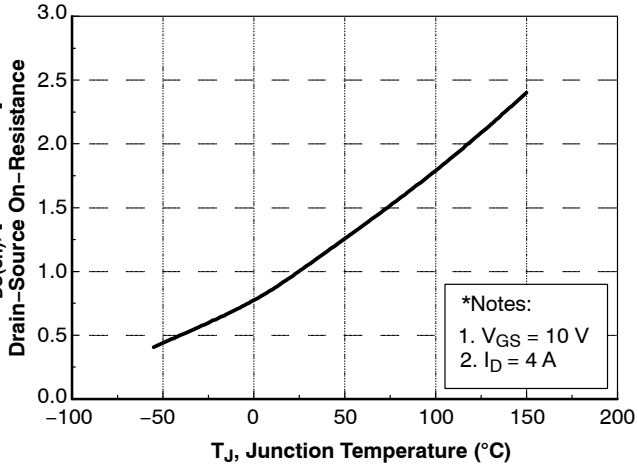


Figure 8. On−Resistance Variation vs Temperature

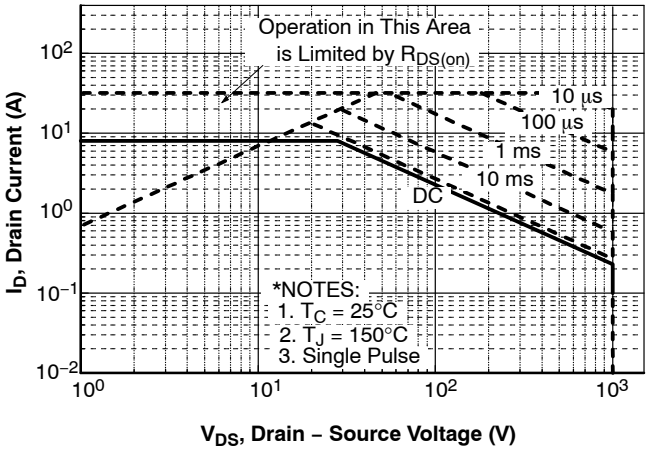


Figure 9. Maximum Safe Operating Area

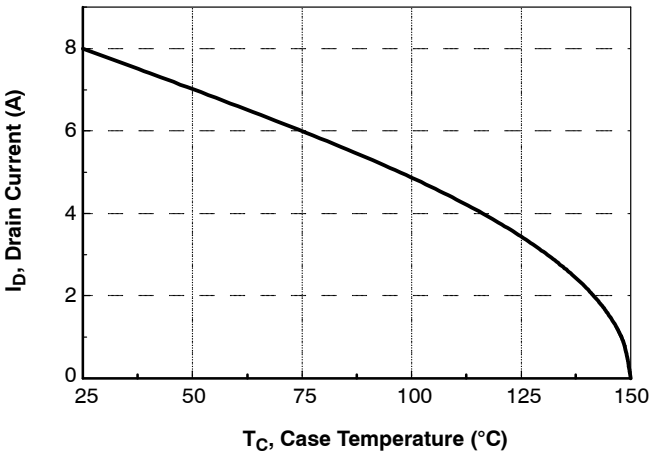


Figure 10. Maximum Drain Current vs. Case Temperature

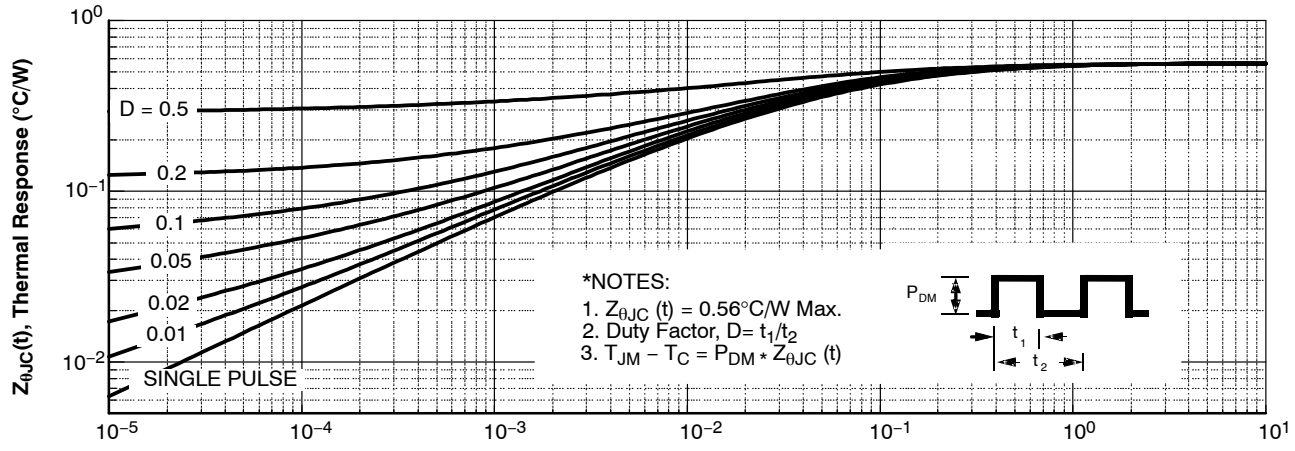


Figure 11. Transient Thermal Response Curve

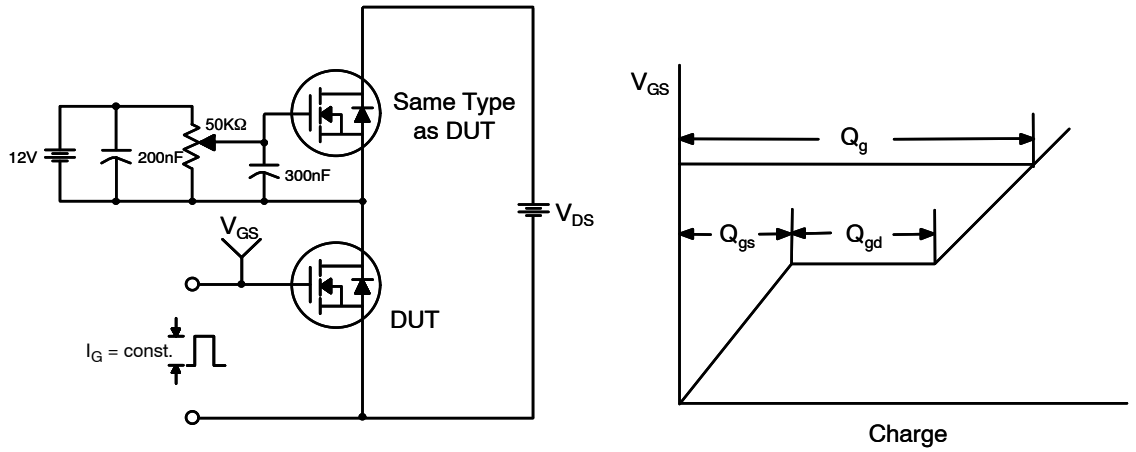


Figure 12. Gate Charge Test Circuit & Waveform

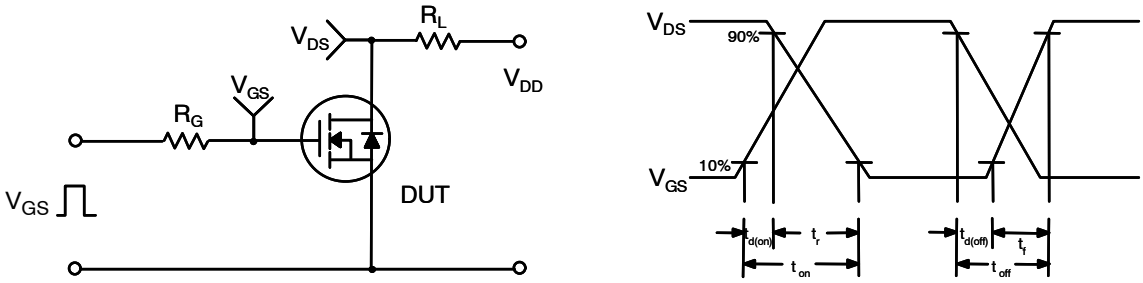


Figure 13. Resistive Switching Test Circuit & Waveforms

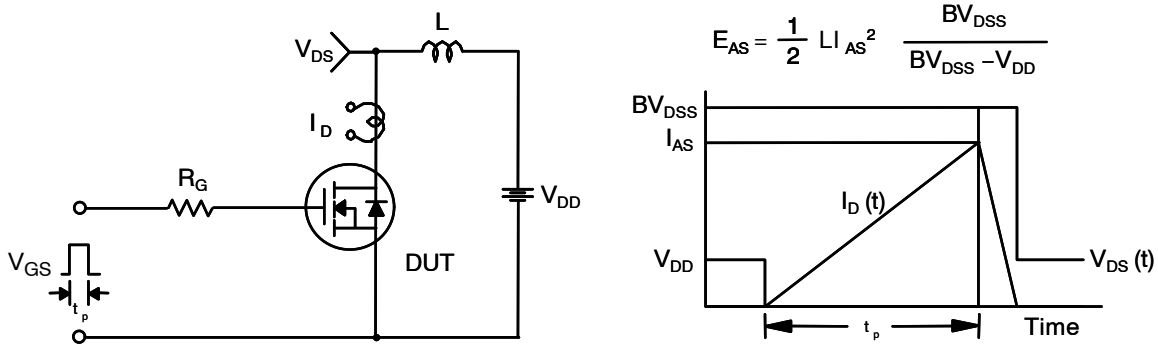


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

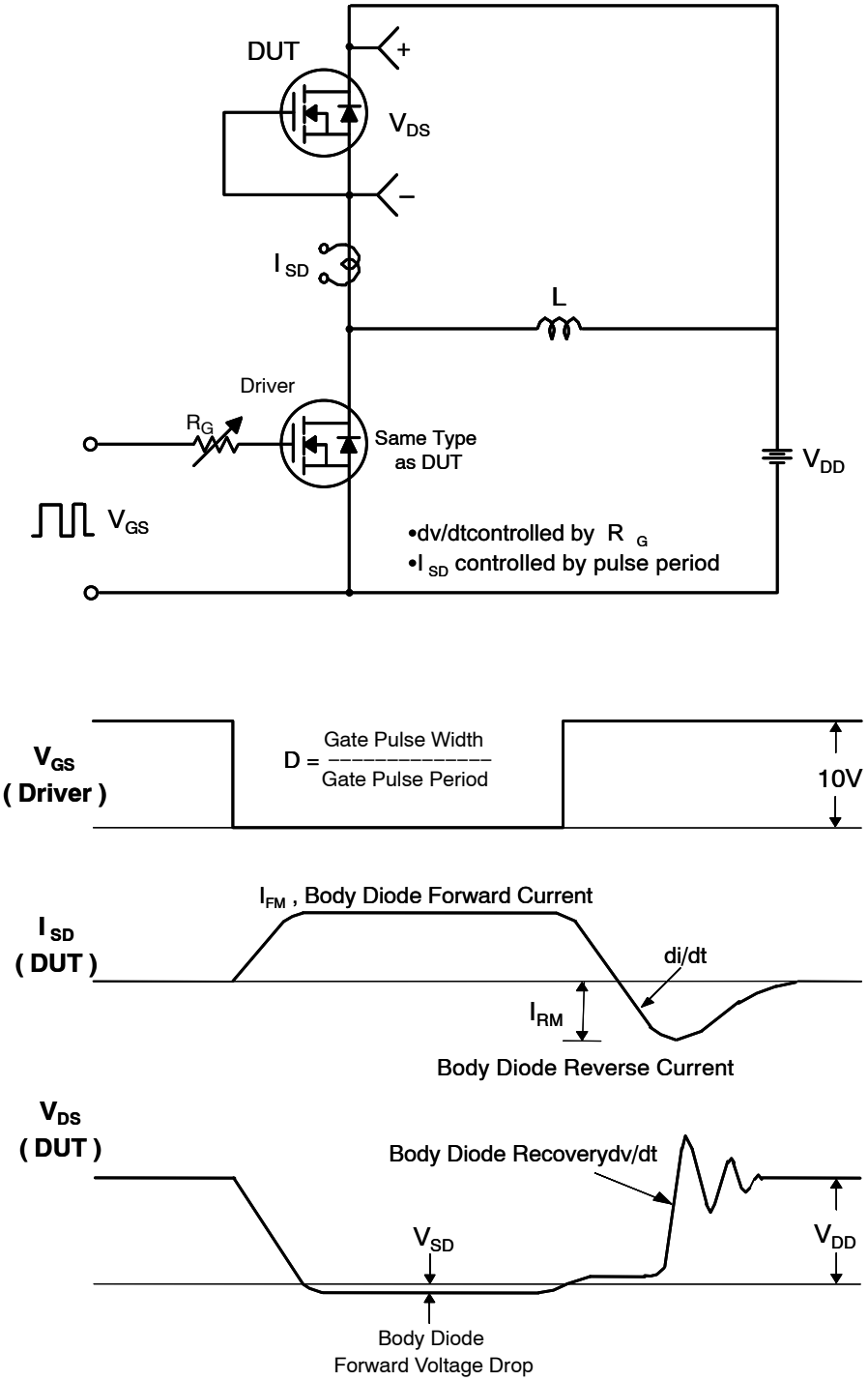
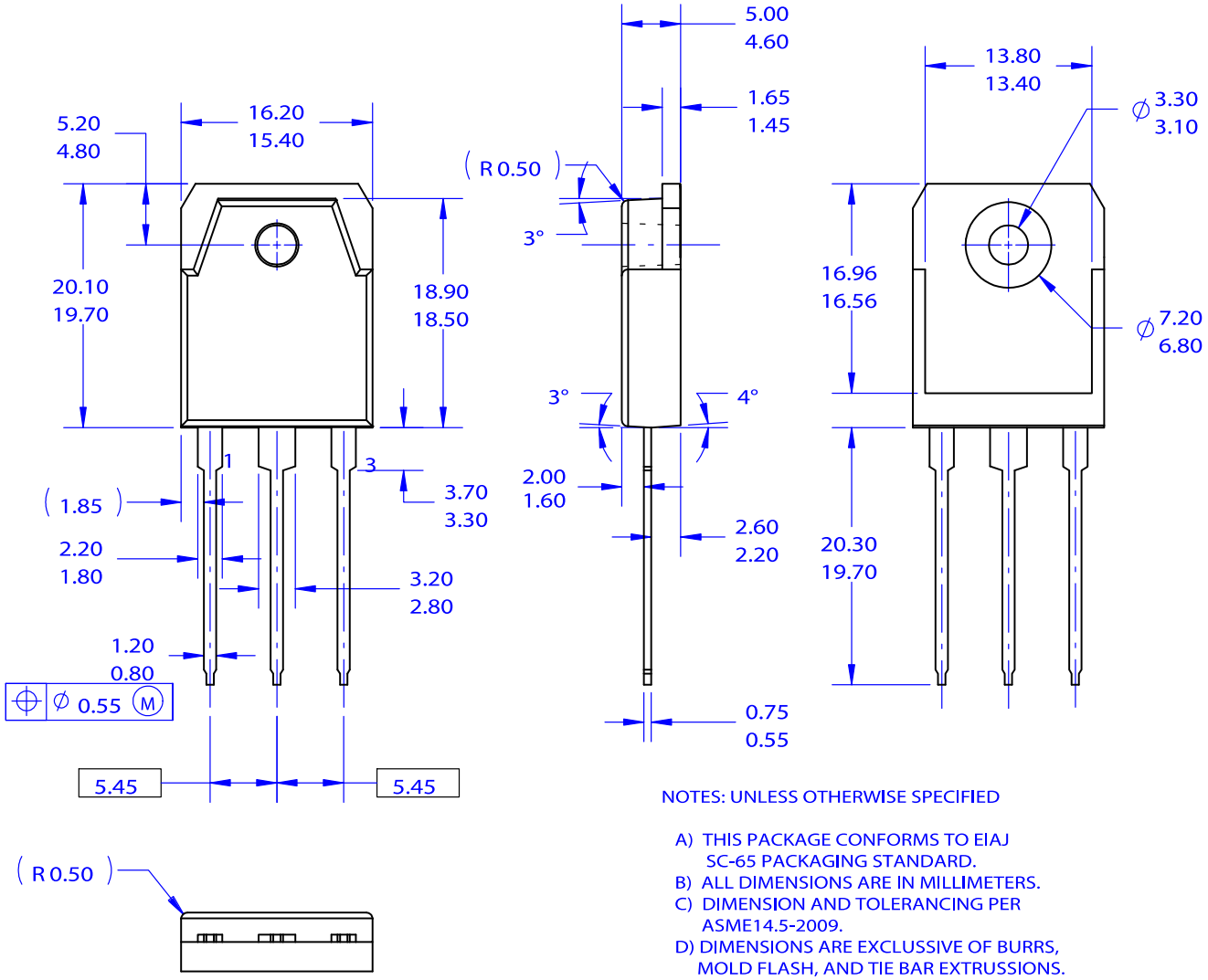


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

TO−3P−3LD / EIAJ SC−65, ISOLATED
CASE 340BZ
ISSUE O

DATE 31 OCT 2016



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