

MOSFET – N-Channel, QFET

100 V, 10 A, 180 mΩ

FQD13N10

Description

This N-Channel enhancement mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- 10 A, 100 V, $R_{DS(on)} = 180\text{ m}\Omega$ (Max.) @ $V_{GS} = 10\text{ V}$, $I_D = 5\text{ A}$
- Low Gate Charge (Typ. 12 nC)
- Low C_{rss} (Typ. 20 pF)
- 100% Avalanche Tested
- This is a Pb-Free Device

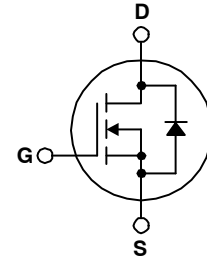
ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	100	V
I_D	Drain Current –Continuous ($T_C = 25^\circ\text{C}$) –Continuous ($T_C = 100^\circ\text{C}$)	10	A
		6.3	A
I_{DM}	Drain Current –Pulsed (Note 1)	40	A
V_{GSS}	Gate–Source Voltage	± 25	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	95	mJ
I_{AR}	Avalanche Current (Note 1)	10	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) Power Dissipation ($T_C = 25^\circ\text{C}$) –Derate Above 25°C	2.5	W
		40 0.32	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	300	°C

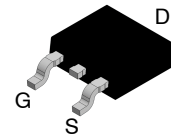
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse-width limited by maximum junction temperature.
2. $L = 1.43\text{ mH}$, $I_{AS} = 10\text{ A}$, $V_{DD} = 25\text{ V}$, $R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 12.8\text{ A}$, $di/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
100 V	180 mΩ @ 10 V	10 A

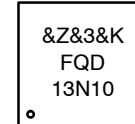


N-CHANNEL MOSFET



DPAK3 (TO-252 3 LD)
CASE 369AS

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FQD13N10	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

FQD13N10

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.13	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	
	Thermal Resistance, Junction to Ambient (*1 in ² Pad of 2-oz Copper), Max.	50	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	-	0.09	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 80\text{ V}, T_C = 125^\circ\text{C}$	-	-	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	-	-	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	-	-	-100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 5.0\text{ A}$	-	0.142	0.18	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 5.0\text{ A}$	-	6.3	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	345	450	pF
C_{oss}	Output Capacitance		-	100	130	pF
C_{rss}	Reverse Transfer Capacitance		-	20	25	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 12.8\text{ A},$ $R_G = 25\ \Omega$ (Note 4)	-	5	20	ns
t_r	Turn-On Rise Time		-	55	120	ns
$t_{d(off)}$	Turn-Off Delay Time		-	20	50	ns
t_f	Turn-Off Fall Time		-	25	60	ns
Q_g	Total Gate Charge	$V_{DS} = 80\text{ V}, I_D = 12.8\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4)	-	12	16	nC
Q_{gs}	Gate-Source Charge		-	2.5	-	nC
Q_{gd}	Gate-Drain Charge		-	5.1	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I_S	Maximum Continuous Drain-Source Diode Forward Current	-	-	10	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	-	-	40	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$	-	-	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 12.8\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$	-	72	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.17	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially Independent of Operating Temperature.

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TYPICAL CHARACTERISTICS

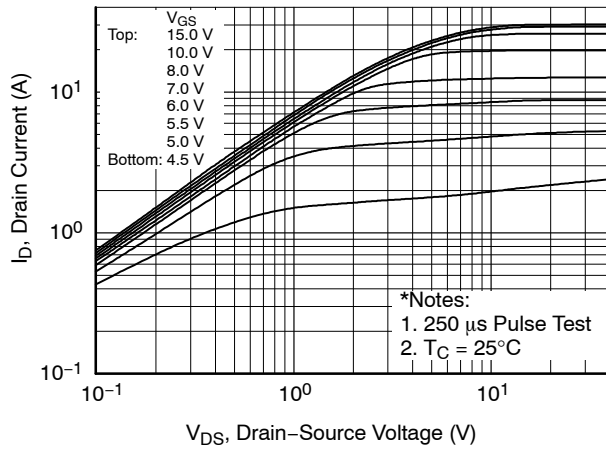


Figure 1. On-Region Characteristics

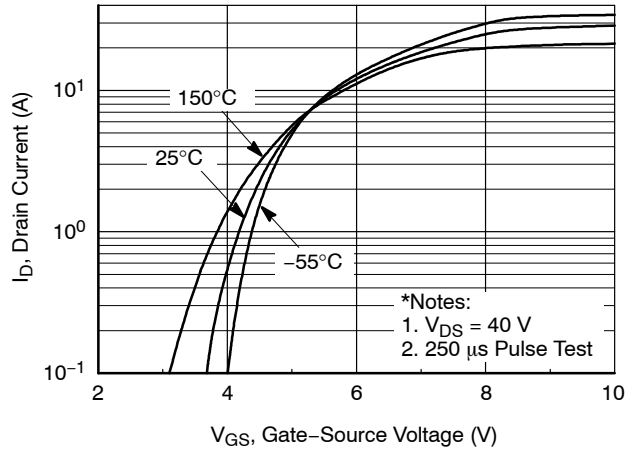


Figure 2. Transfer Characteristics

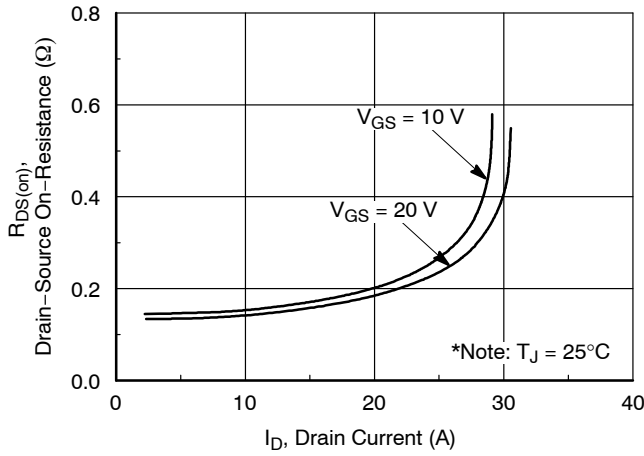


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

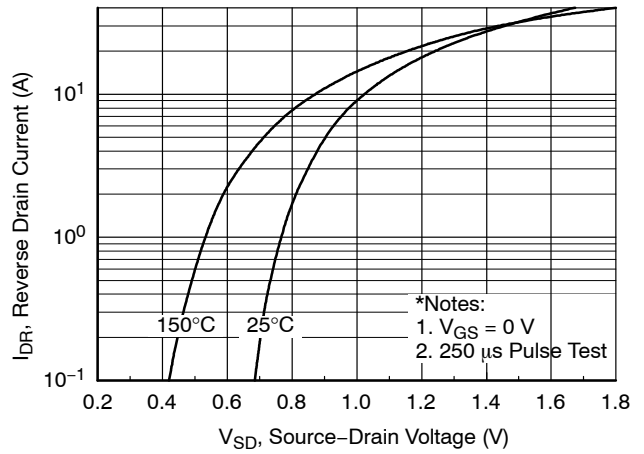


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

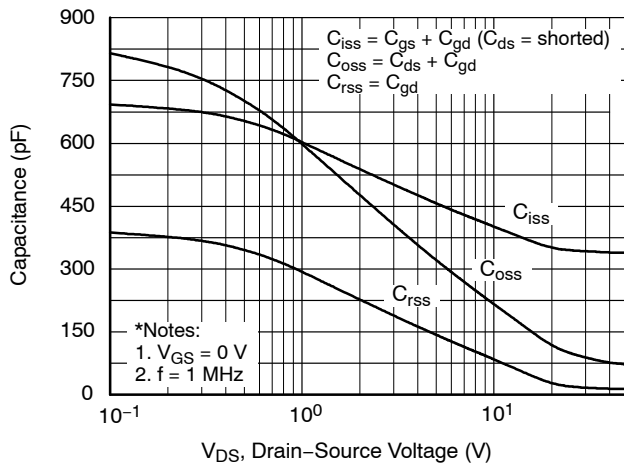


Figure 5. Capacitance Characteristics

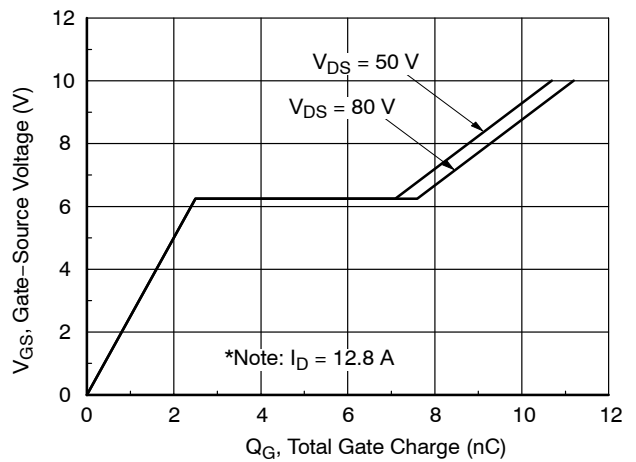


Figure 6. Gate Charge Characteristics

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TYPICAL CHARACTERISTICS (Continued)

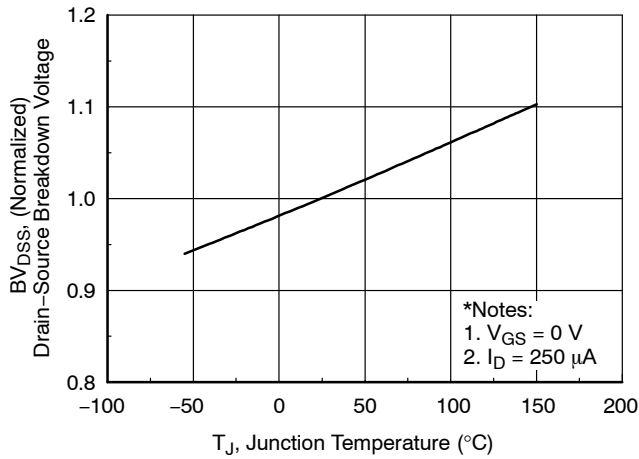


Figure 7. Breakdown Voltage Variation vs. Temperature

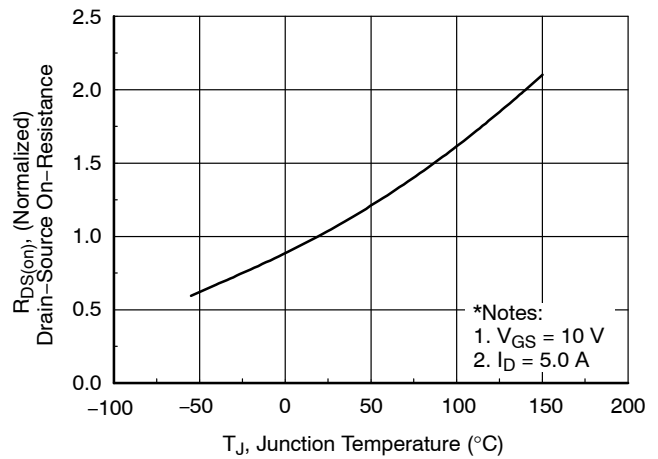


Figure 8. On-Resistance Variation vs. Temperature

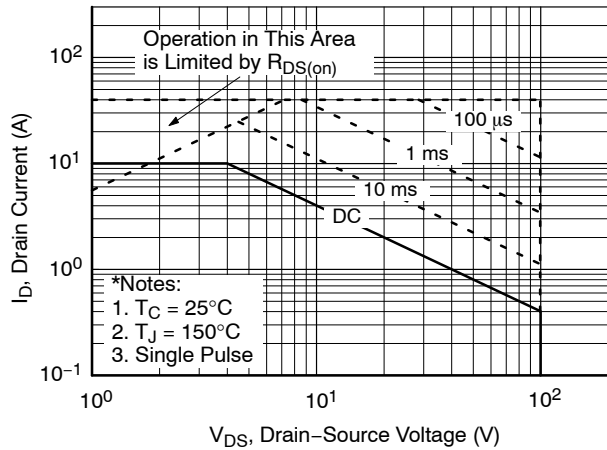


Figure 9. Maximum Safe Operating Area

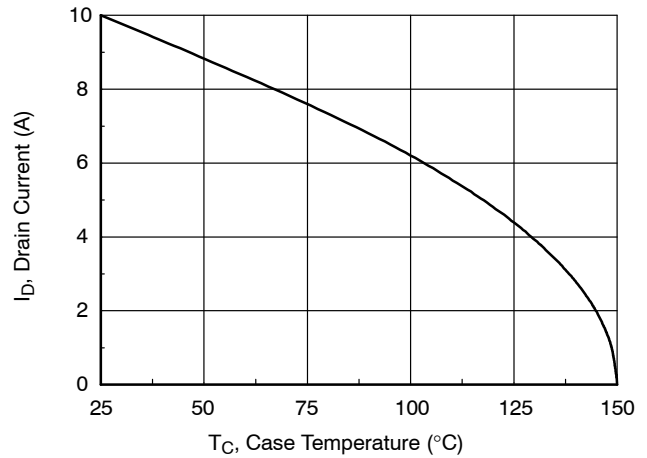


Figure 10. Maximum Drain Current vs. Case Temperature

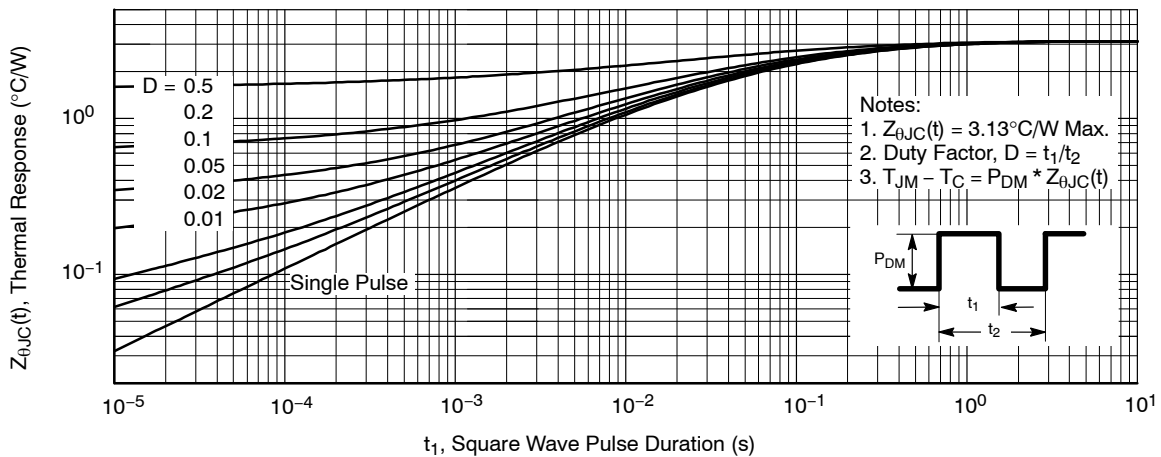


Figure 11. Transient Thermal Response Curve

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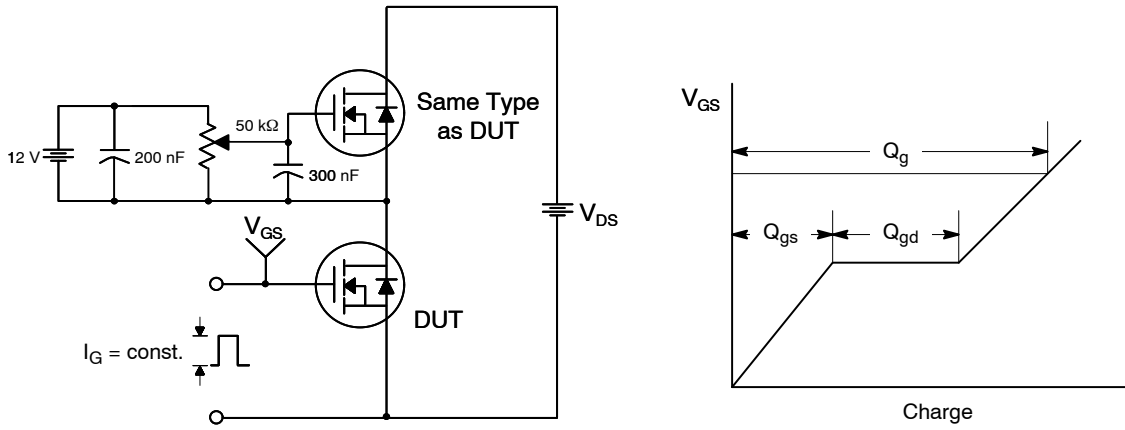


Figure 12. Gate Charge Test Circuit & Waveform

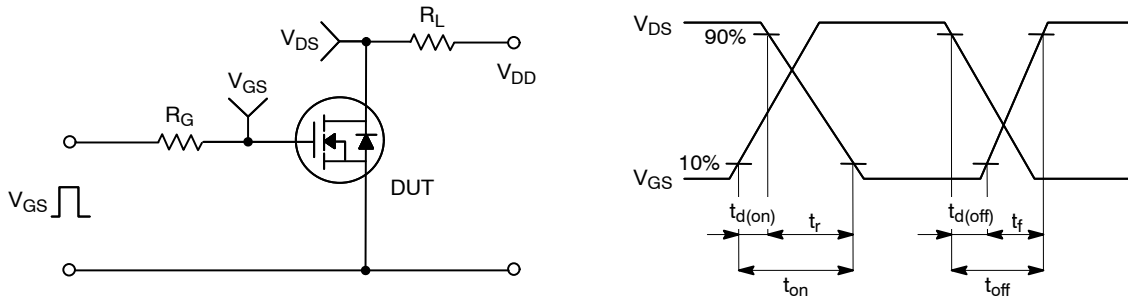


Figure 13. Resistive Switching Test Circuit & Waveforms

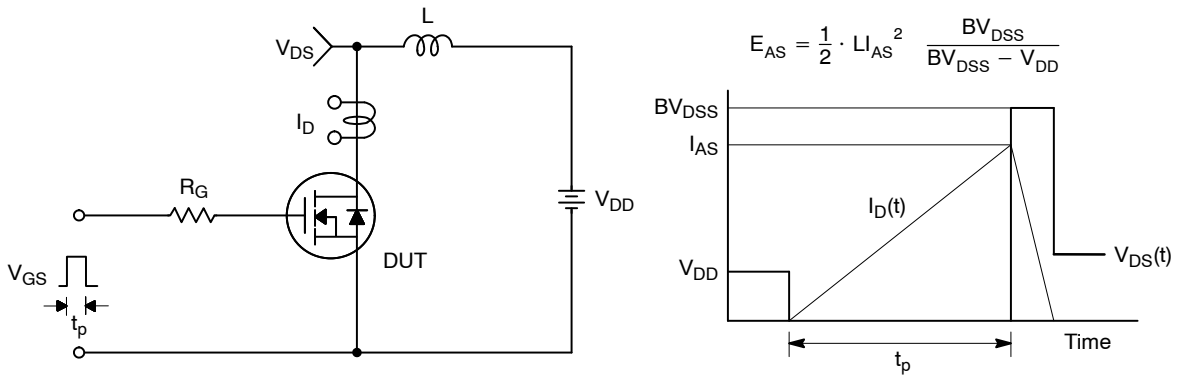


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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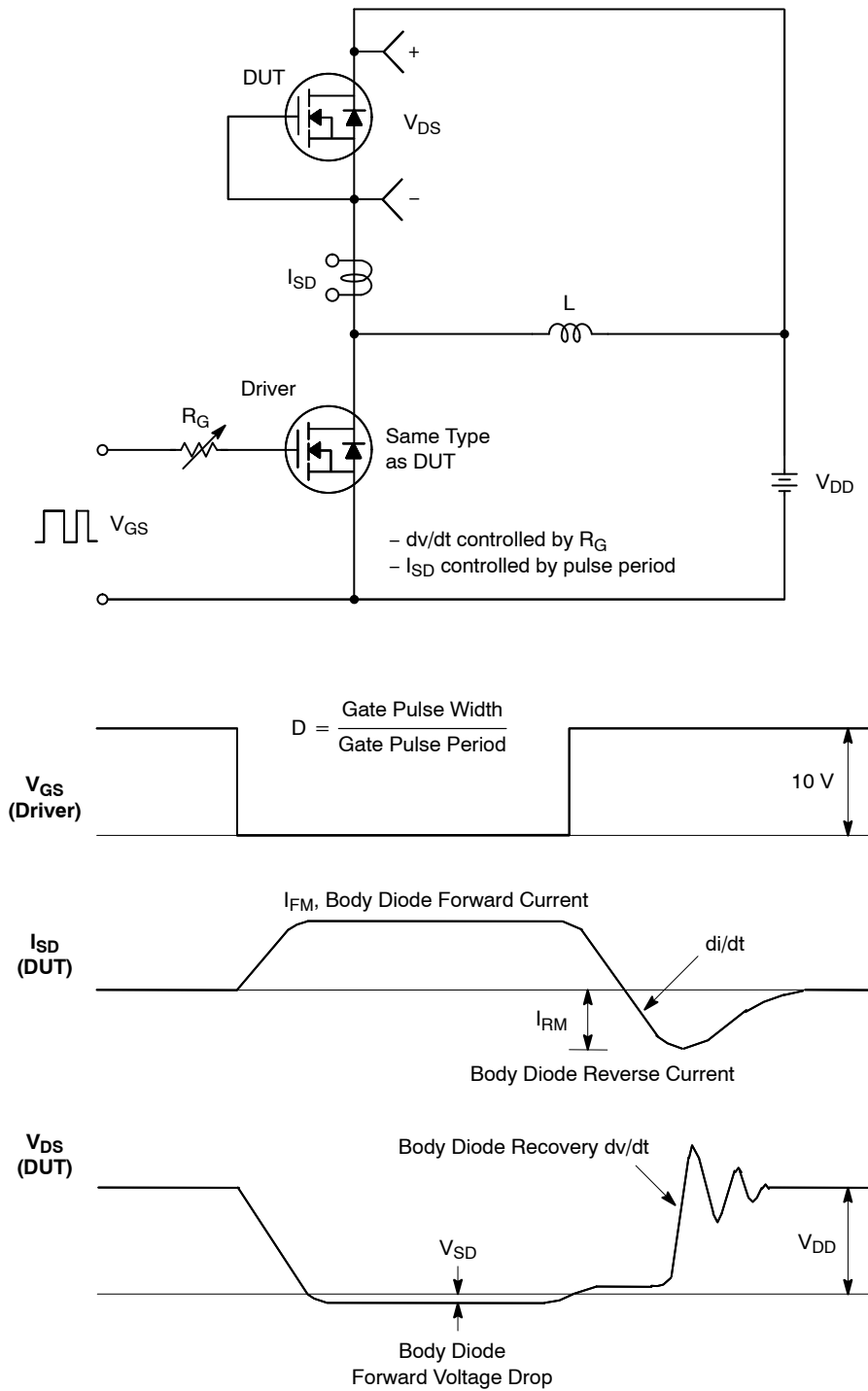
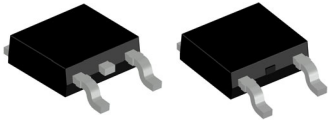


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

PACKAGE MARKING AND ORDERING INFORMATION

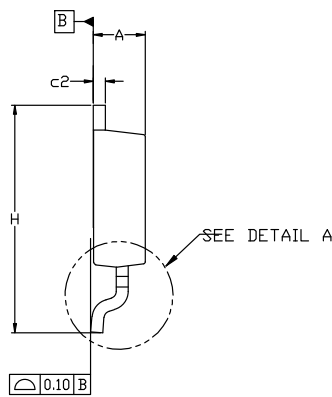
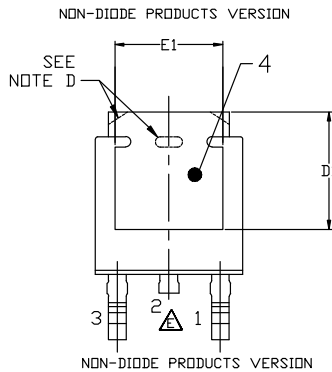
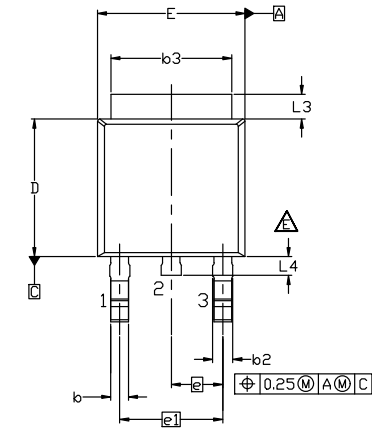
Part Number	Top Mark	Package	Reel Size	Tape Width	Shipping [†]
FQD13N10TM	FQD13N10	DPAK (Pb-Free)	330 mm	16 mm	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

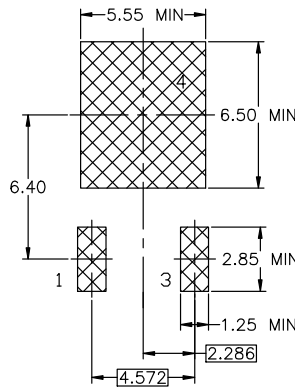
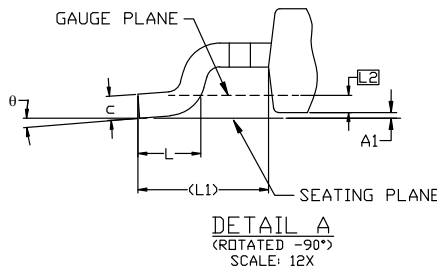


**DPAK3 6.10x6.54x2.29, 4.57P
CASE 369AS
ISSUE B**

DATE 20 DEC 2023



- NOTES: UNLESS OTHERWISE SPECIFIED
 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
 D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
 E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.
 F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TD228P991X239-3N.



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	---	---
E	6.35	6.54	6.73
E1	4.32	---	---
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	---	---	1.02
theta	0°	---	10°

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code

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DESCRIPTION:	DPAK3 6.10x6.54x2.29, 4.57P	PAGE 1 OF 1

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