

# FSA1153

## DP3T USB Type C Audio and UART Analog Switch with OVP

### Description

The FSA1153 is a bi-directional, low power, high speed USB2.0 Type-C, Audio and UART analog switch with overvoltage protection. It is configured as a Double-Pole, Triple Throw (DP3T) switch. The FSA1153s protection function prevents damage to Type-C USB 2.0 port pins caused by high voltage. It provides a receptacle side OVP function on the USB 2.0 data pins and will turn off the relative switch once the voltage level on DN\_L or DP\_R exceed the OV threshold. It can withstand up to 20.5 V DC.

### Features

- DP3T USB Type C Audio and UART Analog Switch
- $V_{DD}$ : 2.7 V to 5.5 V
- $I_{CC}$ : 35  $\mu$ A Typical
- USB Switch
  - ◆ -3 dB Bandwidth (Sdd21): 850 MHz
- Audio Switch:
  - ◆ Negative Rail Capability: -3 V to +3 V
  - ◆ Audio Path  $R_{ON} = 1 \Omega$  (Typ.) at 3.3 V
  - ◆ THD + N = -110 dB; 1  $V_{RMS}$ , 32  $\Omega$  Load;  $f = 20 \text{ Hz} \sim 20 \text{ kHz}$  with A-Weighted Filter
- UART Switch:
  - ◆  $R_{ON}$ : 5  $\Omega$  (Typ.) at 3.3 V
  - ◆ Signal Range: 0 – 4.4 V
- High Power Supply Ripple Rejection
- 20.5 V Overvoltage Protection on DN\_L/DP\_R
- 20.5 V Surge Protection on DN\_L/DP\_R

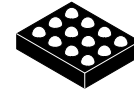
### Applications

- Mobile Phones
- Tablets
- Notebook PC
- Media Player



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)



WLCSP12  
CASE 567WM

### MARKING DIAGRAM



6G = Device Number  
KK = Assembly Lot  
X = Year  
Y = Work Week  
Z = Assembly Location

### ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

# FSA1153

## Typical Application

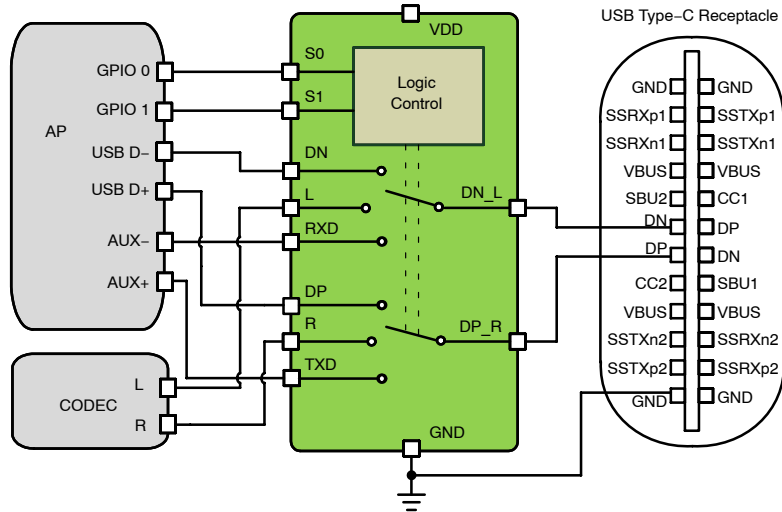


Figure 1. Typical Application

## Pin Definitions

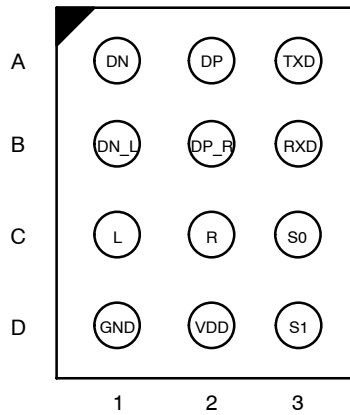


Figure 2. Top Through View

## PIN DESCRIPTION

Pin	Name	Description
A1	DN	USB Data (Differential -)
A2	DP	USB Data (Differential +)
A3	TXD	UART Transmit Data
B1	DN_L	USB/Audio/UART Common Connector
B2	DP_R	USB/Audio/UART Common Connector
B3	RXD	UART Receive Data
C1	L	Audio – Left Channel
C2	R	Audio – Right Channel
C3	S0	Data Switch Select
D1	GND	Chip Ground
D2	VDD	Power Supply (2.7 to 5.5 V)
D3	S1	Data Switch Select

# FSA1153

**Table 1. CONTROL LOGIC STATUS**

S1	S0	USB Switch	Audio Switch	UART Switch
0	0	ON	OFF	OFF
0	1	OFF	ON	OFF
1	0	OFF	OFF	ON
1	1	Disable	Disable	Disable

## ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Top Mark
FSA1153UCX	-40 to +85°C	12-Ball WLCSP, Non-JEDEC 1.45 mm x 1.615 mm, 0.4 mm Pitch	6G

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit		
VDD	Supply Voltage from VDD	-0.5	6.5	V		
V <sub>SW_C</sub>	V <sub>DP_R</sub> to GND, V <sub>DN_L</sub> to GND (Note 1)	-3.6	20.5	V		
V <sub>SW_USB</sub>	V <sub>DP</sub> to GND, V <sub>DN</sub> to GND (Note 1)	-0.5	6.5	V		
V <sub>SW_Audio</sub>	V <sub>L</sub> to GND, V <sub>R</sub> to GND (Note 1)	-3.6	6.5	V		
V <sub>SW_UART</sub>	V <sub>TXD</sub> to GND, V <sub>RXD</sub> to GND (Note 1)	-0.5	6.5	V		
V <sub>SW</sub>	Control Input Voltage: S1, S0 (Note 2)	-0.5	6.5	V		
I <sub>SW_Audio</sub>	Switch I/O Current, Audio path: R, L, DP_R, DN_L	-250	250	mA		
I <sub>SW_USB</sub>	Switch I/O Current, USB path; DP to DP_R, DN to DN_L	-	100	mA		
I <sub>SW_UART</sub>	Switch I/O Current, UART path; TXD to DP_R, RXD to DN_L	-	50	mA		
I <sub>IK</sub>	DC Input Diode Current	-50	-	mA		
ESD	Human Body Model, ANSI / ESDA / JEDEC JS-001-2012	Connector side and power pins: VDD, DP_R, DN_L	4	-	kV	
		Host side pins: The rest pins	2	-		
	Charged Device Model, JEDEC: JESD22-C101	1	-			
Surge	IEC 61000-4-5 System	Connector side pins: DP_R, DN_L		-20.5	+20.5	V
T <sub>A</sub>	Absolute Maximum Operating Temperature		-40	+85	°C	
T <sub>STG</sub>	Storage Temperature		-65	+150	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
2. V<sub>SW</sub> refers to analog data switch paths.

# FSA1153

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
<b>POWER</b>					
VDD	Supply Voltage	2.7	–	5.5	V
<b>USB SWITCH</b>					
V <sub>SW_USB</sub>	V <sub>DP</sub> to GND, V <sub>DN</sub> to GND, V <sub>DP_R</sub> to GND, V <sub>DN_L</sub> to GND	0	–	4.5	V
<b>AUDIO SWITCH</b>					
V <sub>SW_Audio</sub>	V <sub>DP_R</sub> to GND, V <sub>DN_L</sub> to GND, V <sub>L</sub> to GND, V <sub>R</sub> to GND,	–3.0	–	+3.0	V
<b>UART SWITCH</b>					
V <sub>SW_UART</sub>	V <sub>TXD</sub> to GND, V <sub>RXD</sub> to GND	0	–	4.4	V
<b>OPERATING TEMPERATURE</b>					
T <sub>A</sub>	Ambient Operating Temperature	–40	25	+85	°C
<b>CONTROL VOLTAGE (S1, S0)</b>					
V <sub>IH</sub>	Input Voltage High	1.3	–	VCC	V
V <sub>IL</sub>	Input Voltage Low	0	–	0.5	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# FSA1153

## DC AND TRANSIENT CHARACTERISTICS

(V<sub>DD</sub> = 2.7 V to 5.5 V, V<sub>DD</sub>(Typ.) = 3.3 V, T<sub>A</sub> = -40°C to 85°C, and T<sub>A</sub> (Typ.) = 25°C, unless otherwise specified)

Symbol	Parameter	Condition	Power	T <sub>A</sub> = -40°C to 85°C			Unit
				Min	Typ	Max	

### GENERAL DEVICE PINS

I <sub>CC</sub>	Supply current	For all switches	VDD: 2.7 to 5.5	-	-	35	μA
I <sub>CCZ</sub>	Quiescent current	S0, 1 = 1		-	-	3	
I <sub>CCT</sub>		V <sub>in</sub> = 1.5 V		-	10	-	μA

### COMMON PINS: DP\_R, DN\_L

I <sub>OZ</sub>	Off leakage current of Port DP_R and DN_L	DP_R, DN_L = -3 V to 4.0 V	VDD: 2.7 to 5.5	-3.0	0.1	3.0	μA
I <sub>OFF</sub>	Power-Off leakage current of Port DP_R and DN_L	DP_R, DN_L = 0 V to 4.0 V	Power off	-3.0	0.1	3.0	μA
V <sub>OV_TRIP</sub>	Input OVP Lockout	Sweep from 3 V to 6 V	VDD: 2.7 to 5.5	4.7	5.0	5.3	V
V <sub>OV_HYS</sub>	Input OVP Hysteresis		VDD: 2.7 to 5.5	0.2	0.3	0.4	V

### AUDIO SWITCH

I <sub>ON</sub>	On leakage current of Audio switch	DN_L, DP_R = -3 V to 3.0 V, R, L = Float	VDD: 2.7 to 5.5	-2.0	0.1	2.0	μA
I <sub>OZ</sub>	Off leakage current of	L / R = -3 V to 3.0 V	VDD: 2.7 to 5.5	-1	0.1	1	μA
I <sub>OFF</sub>	Input Leakage Current , Power off	L, R = 0 to 3 V, DP_R, DP_L = Float, (I <sub>SW</sub> = 0 mA)	Power off	-1.0	0.1	1.0	μA
R <sub>ON</sub>	Switch On Resistance	I <sub>SW</sub> = 100 mA, V <sub>SW</sub> = -3 V to 3 V	VDD: 2.7 to 5.5	-	1	2	Ω
ΔR <sub>ON</sub>	On Resistance Matching, Channel to Channel	I <sub>SW</sub> = 100 mA, V <sub>SW</sub> = -3 V to 3 V	VDD: 2.7 to 5.5	-	0.1	0.2	Ω
R <sub>FLAT</sub>	On Resistance Flatness	I <sub>SW</sub> = 100 mA, V <sub>SW</sub> = -3 V to 3 V	VDD: 2.7 to 5.5	-	10	-	mΩ

### USB SWITCH

I <sub>ON</sub>	On leakage current of USB switch	DN_L, DP_R = 0 V to 3.6 V, DP = DN = Float	VDD: 2.7 to 5.5	-3.0	0.1	5	μA
		DN_L, DP_R = 3.6 V to 4.5 V, DP = DN = Float		-5	-	15	
I <sub>OZ</sub>	Off leakage current of Port DP and DN	DN, DP = 0 V to 4.5 V	VDD: 2.7 to 5.5	-3.0	0.1	3.0	μA
I <sub>OFF</sub>	Power-Off leakage current of Port DP and DN	DN, DP = 0 V to 4.5 V	Power off	-3.0	0.1	3.0	μA
R <sub>ON_USB</sub>	Switch On Resistance	V <sub>SW</sub> = 0.4 V, I <sub>ON</sub> = -8 mA	VDD: 2.7 to 5.5	-	3	5	Ω
		V <sub>sw</sub> = 4.0 V, I <sub>ON</sub> = -8 mA		-	3	5	

### UART SWITCH

I <sub>ON</sub>	On leakage current of UART switch	DN_L, DP_R = 0 V to 4.4 V, UART = Float	VDD: 2.7 to 5.5	-3.0	0.1	15	μA
I <sub>OZ</sub>	Off leakage current of Port TXD and RXD	TXD/RXD = 0 V to 4.4 V,	VDD: 2.7 to 5.5	-3.0	0.1	3.0	μA
I <sub>OFF</sub>	Power-Off leakage current of Port TXD/RXD	TXD/RXD = 0 V to 4.4 V,	Power off	-3.0	0.1	3.0	μA
R <sub>ON_UART</sub>	UART Switch On Resistance	V <sub>SW</sub> = 0 to 4.4 V, I <sub>ON</sub> = -8 mA	VDD: 2.7 to 5.5	-	5	7	Ω

### S1, S0

V <sub>IH</sub>	Input Voltage High		VDD: 2.7 to 5.5	1.3	-	VDD	V
V <sub>IL</sub>	Input Voltage Low		VDD: 2.7 to 5.5	-	-	0.5	V
R <sub>PD</sub>	Internal Pull down resistor on S1,S0	S1, S0 = VDD	VDD: 2.7 to 5.5	-	3	-	MΩ

# FSA1153

## AC CHARACTERISTICS

( $V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{DD}(\text{Typ.}) = 3.3\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$ ,  $T_A(\text{Typ.}) = 25^\circ\text{C}$ , unless otherwise specified)

Symbol	Parameter	Condition	Power	$T_A = -40^\circ\text{C to }85^\circ\text{C}$			Unit
				Min	Typ	Max	

### AUDIO PATH SWITCH

$t_{ON}$	Turn On Time (Note 3)	DP/R = DN/L = 0 V $\rightarrow$ to 1 V, L, R = 32 $\Omega$ to GND		-	80	-	$\mu\text{s}$
$t_{OFF}$	Turn OFF Time (Note 3)	DP/R = DN/L = 1 V fall to GND, L, R = 32 $\Omega$ to GND		-	0.4	-	$\mu\text{s}$
$t_{BBM}$	Break Before Make (Note 3)	USB $\rightarrow$ Audio, DP/R = DN/L = 0 V $\rightarrow$ 1 V, L, R = 32 $\Omega$ to GND, DP, DN = 50 $\Omega$ to GND UART $\rightarrow$ Audio, UART = 50 $\Omega$		-	80	-	$\mu\text{s}$
$T_{EN}$	Enable Time (Note 3)	DP/R = DN/L = 1 V, L, R = 32 $\Omega$ to GND, S[1, 0] from 11 to 01		-	230	-	$\mu\text{s}$
$T_{Dis}$	Disable Time (Note 3)	DP/R = DN/L = 1 V, L, R = 32 $\Omega$ to GND, S[1, 0] from 01 to 11		-	0.3	-	$\mu\text{s}$
$t_{OVP}$	Response Time	$R_{LOAD} = 32\ \Omega$ , $V_{sw} = 3\text{ V to }6\text{ V}$ (slew rate $>10\text{ V}/1\ \mu\text{s}$ ), measure OV threshold to 90% OVP trigger level of output falling		-	0.2	1	$\mu\text{s}$
$O_{IRR}$	Off Isolation (Note 3)	$f = 1\text{ kHz}$ , $R_L = 50\ \Omega$ , $C_L = 0\text{ pF}$ , $V_{SW} = 1\text{ V}_{RMS}$		-	-100	-	dB
		$f = 1\text{ MHz}$ , $R_L = 50\ \Omega$ , $C_L = 0\text{ pF}$ , $V_{SW} = 1\text{ V}_{RMS}$		-	-65	-	
$X_{TALK}$	Cross Talk (Adjacent) (Note 3)	$f = 1\text{ kHz}$ , $R_L = 50\ \Omega$ , $V_{SW} = 1\text{ V}_{RMS}$		-	-120	-	dB
	Cross Talk (USB–Audio) (Note 3)	$f = 1\text{ kHz or }20\text{ kHz}$ , $R_L = 50\ \Omega$ , $V_{SW} = 1\text{ V}_{RMS}$ on DP or DN		-	-108	-	
BW	-3 dB Bandwidth (Note 3)	$R_L = 50\ \Omega$		-	500	-	MHz
PSRR	Power Supply Rejection Ratio (Note 3)	$V_{PSRR} = V_{DD} + 100\text{ mV}_{RMS}$ $R_L = 20\text{ k}\Omega\text{ or }32\ \Omega$ (at DP / R, DN / L), $f = 1\text{ kHz}$	$R_L = 32\ \Omega$	-	-119	-	dB
			$R_L = 20\text{ k}\Omega$	-	-105	-	
THD+N	Total Harmonic Distortion + Noise (Note 3)	$R_L = 16\ \Omega$ , $f = 20\text{ Hz} \sim 20\text{ kHz}$ , $V_{SW} = 0.5\text{ V}_{RMS}$	With A-weighted	-	-108	-	dB
			Non A-weighted	-	-105	-	
		$R_L = 32\ \Omega$ , $f = 20\text{ Hz} \sim 20\text{ kHz}$ , $V_{SW} = 1\text{ V}_{RMS}$	With A-weighted	-	-110	-	dB
			Non A-weighted	-	-105	-	
		$R_L = 20\text{ k}\Omega$ , $f = 20\text{ Hz} \sim 20\text{ kHz}$ , $V_{SW} = 0.3\text{ V}_{RMS}$	With A-weighted	-	-110	-	dB
			Non A-weighted	-	-105	-	

### USB SWITCH

$t_{ON}$	Turn-on time (Note 3)	DP/R = DN/L = 1.0 V, DP, DN = 50 $\Omega$ to GND		-	40	-	$\mu\text{s}$
$t_{OFF}$	Turn-off time (Note 3)	DP/R = DN/L = 1.0 V, DP, DN = 50 $\Omega$ to GND		-	0.35	-	$\mu\text{s}$
$T_{BBM}$	Break–Before–Make (Note 3)	Audio $\rightarrow$ USB; DP/R = DN/L = 1.5 V, L, R = 50 $\Omega$ to GND, DP, DN = 50 $\Omega$ to GND UART $\rightarrow$ USB: UART = 50 $\Omega$		-	40	-	$\mu\text{s}$
$T_{EN}$	Enable Time (Note 3)	DP/R = DN/L = 1 V, DP/DN = 50 $\Omega$ to GND, S[1, 0] from 11 to 00		-	200	-	$\mu\text{s}$
$T_{Dis}$	Disable Time (Note 3)	DP / R = DN / L = 1 V, DP / DN = 50 $\Omega$ to GND, S[1, 0] from 00 to 11		-	0.25	-	$\mu\text{s}$
BW	-3dB Bandwidth (Note 3)	$R_L = 50\ \Omega$ , Switch ON		-	0.85	-	GHz
$X_{TALK}$	Cross Talk (Adjacent) (Note 3)	$R_L = 50\ \Omega$ , Switch ON, $f = 240\text{ MHz}$		-	-40	-	dB
$O_{IRR}$	Off Isolation (Note 3)	$R_L = 50\ \Omega$ , Switch OFF, $f = 240\text{ MHz}$		-	-24	-	dB
$t_{OVP}$	Response Time	$R_{LOAD} = 50\ \Omega$ , $V_{sw} = 3\text{ V to }6\text{ V}$ (slew rate $>10\text{ V}/1\ \mu\text{s}$ ), measure OV threshold to 90% OVP trigger level of output falling		-	0.2	1	$\mu\text{s}$

# FSA1153

## AC CHARACTERISTICS (continued)

( $V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{DD}(\text{Typ.}) = 3.3\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$ ,  $T_A(\text{Typ.}) = 25^\circ\text{C}$ , unless otherwise specified) (continued)

Symbol	Parameter	Condition	Power	$T_A = -40^\circ\text{C to }85^\circ\text{C}$			Unit
				Min	Typ	Max	
<b>USB SWITCH</b>							
$t_{\text{Recovery}}$	Recovery Debounced time (Note 3)	$R_{\text{LOAD}} = 50\ \Omega$ , $V_{\text{sw}} = 6\text{ V to }3\text{ V}$ (slew rate $< 10\text{ V/1}\ \mu\text{s}$ ), measure OV threshold to 90% output rising		-	30	-	us
$t_{\text{PD}}$	Propagation Delay (Note 3)	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$		-	100	-	ps
$t_{\text{SK(P)}}$	Skew of Opposite Transitions of the Same Output (Note 3)	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$		-	10	-	ps
$t_J$	Total Jitter (Note 3)	$V_{\text{SW}} = 0.4\text{ VdiffPP}$ , $R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , $t_R = t_F = 500\ \text{ps}$ (10 – 90%) @ 480 Mbps (PBRS = $2^{15} - 1$ )		-	200	-	ps

## UART SWITCH

$t_{\text{ON}}$	Turn-on time (Note 3)	UART = 1.8 V, $R_{\text{load}} = 50\ \Omega$		-	50	-	$\mu\text{s}$
$t_{\text{OFF}}$	Turn-off time (Note 3)	UART = 1.8 V, $R_{\text{load}} = 50\ \Omega$		-	0.4	-	$\mu\text{s}$
$T_{\text{BBM}}$	Break-Before-Make (Note 3)	USB $\rightarrow$ UART, USB = $50\ \Omega$ , UART = $50\ \Omega$ Audio $\rightarrow$ UART		-	50	-	$\mu\text{s}$
$T_{\text{EN}}$	Enable Time (Note 3)	DP/R = DN/L = 1 V, DP/DN = $50\ \Omega$ to GND, S[1, 0] from 11 to 10		-	200	-	$\mu\text{s}$
$T_{\text{Dis}}$	Disable Time (Note 3)	DP/R = DN/L = 1 V, DP/DN = $50\ \Omega$ to GND, S[1, 0] from 10 to 11		-	300	-	$\mu\text{s}$
$t_{\text{OVP}}$	Response Time	$R_{\text{LOAD}} = 50\ \Omega$ , $V_{\text{sw}} = 3\text{ V to }6\text{ V}$ (slew rate $> 10\text{ V/1}\ \mu\text{s}$ ), measure OV threshold to 90% OVP trigger level of output falling		-	0.2	1	$\mu\text{s}$
BW	Bandwidth (Note 3)	$R_L = 50\ \Omega$		-	400	-	MHz

3. Guaranteed by characterization, not production tested.

## CAPACITANCE ( $V_{DD} = 2.7\text{ V to }5.5\text{ V}$ , $V_{DD}(\text{Typ.}) = 3.3\text{ V}$ , $T_A = -40^\circ\text{C to }85^\circ\text{C}$ , $T_A(\text{Typ.}) = 25^\circ\text{C}$ , unless otherwise specified)

Symbol	Parameter	Condition	Power	$T_A = -40^\circ\text{C to }85^\circ\text{C}$			Unit
				Min	Typ	Max	
<b>AUDIO PATH SWITCH</b>							
$C_{\text{ON\_USB/Audio/UART}}$	On Capacitance (Common Port) (Note 4)	$f = 1\text{MHz, }240\text{ MHz, }100\ \text{mV}_{\text{PK-PK}}, 100\ \text{mV DC bias}$	3.3	-	7	-	pF
$C_{\text{OFF\_USB/Audio/UART}}$	Off Capacitance (Common Port) (Note 4)	$f = 1\text{MHz, }240\text{MHz, }100\ \text{mV}_{\text{PK-PK}}, 100\ \text{mV DC bias}$	3.3	-	7	-	pF
$C_{\text{OFF\_USB}}$	Off Capacitance (Non-Common Ports) (Note 4)	$f = 240\ \text{MHz, }100\ \text{mV}_{\text{PK-PK}}, 100\ \text{mV DC bias}$	3.3	-	2.5	-	pF
$C_{\text{OFF\_Audio}}$	Off Capacitance (Non-Common Ports) (Note 4)	$f = 1\ \text{MHz, }100\ \text{mV}_{\text{PK-PK}}, 100\ \text{mV DC bias}$	3.3	-	3.5	-	pF
$C_{\text{OFF\_UART}}$	Off Capacitance (Non-Common Ports) (Note 4)	$f = 1\ \text{MHz, }100\ \text{mV}_{\text{PK-PK}}, 100\ \text{mV DC bias}$	3.3	-	3.5	-	pF
$C_{\text{IN}}$	EN,SEL Pin Capacitance (Note 4)	$f = 1\ \text{MHz, }100\ \text{mV}_{\text{PP}}, 100\ \text{mV DC bias}$	S1, S0	0	-	2.5	pF

4. Guaranteed by characterization, not production tested.

## Application Information

### Over-Voltage Protection

The FSA1153 features over-voltage protection (OVP) on the receptacle side pins DN\_L and DP\_R which will switch off the internal signal routing path if the input voltage

exceeds the OVP threshold. When an over voltage condition has occurred the switch will open immediately and remain open until the over voltage condition is removed.

Test Diagrams

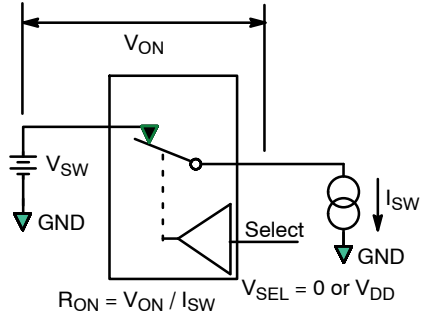


Figure 3. On Resistance

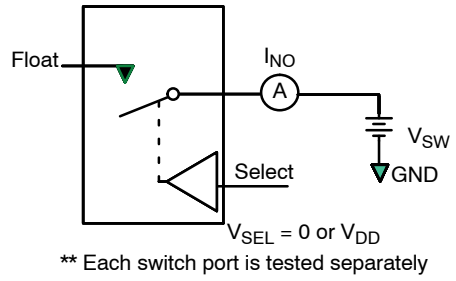


Figure 4. Off Leakage ( $I_{oz}$ )

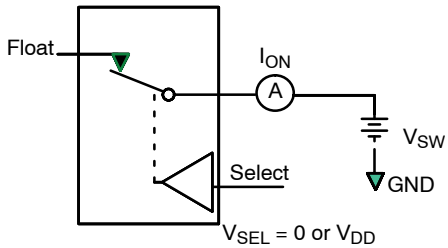


Figure 5. On Leakage

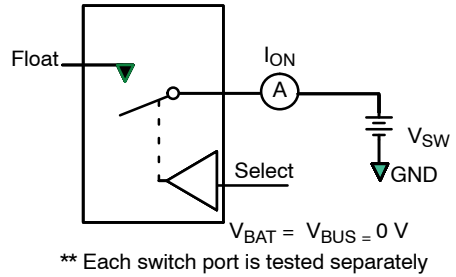


Figure 6. Power Off Leakage ( $I_{off}$ )

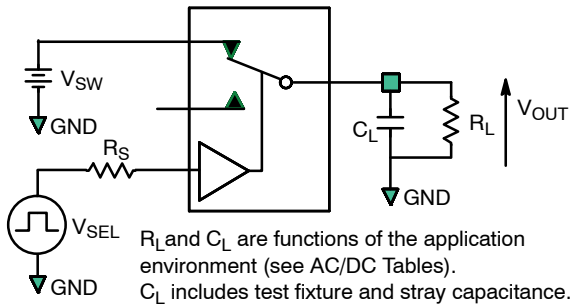


Figure 7. Test Circuit Load

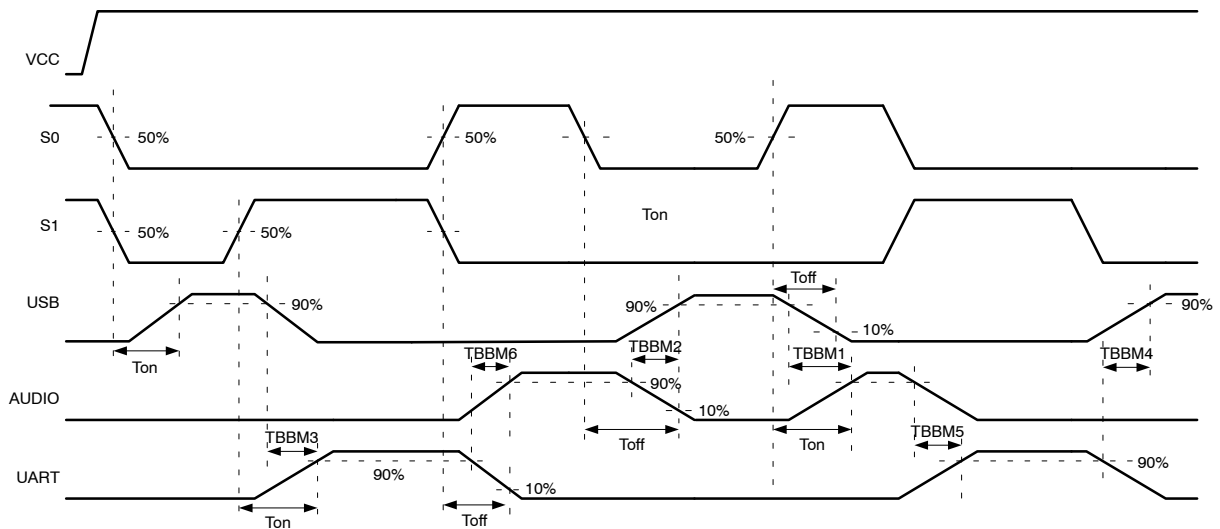


Figure 8. Timing Waveforms



Test Diagrams (continued)

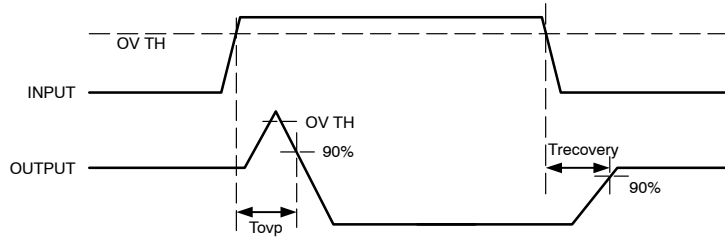


Figure 9. OVP Timing

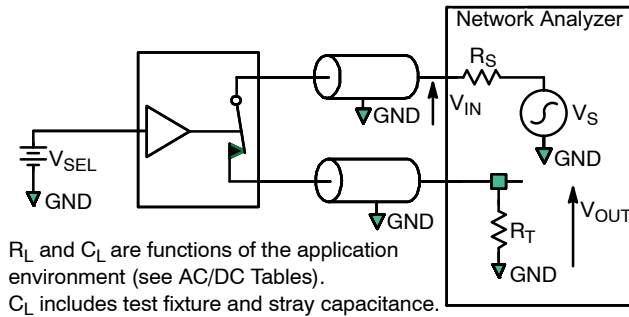


Figure 10. Bandwidth

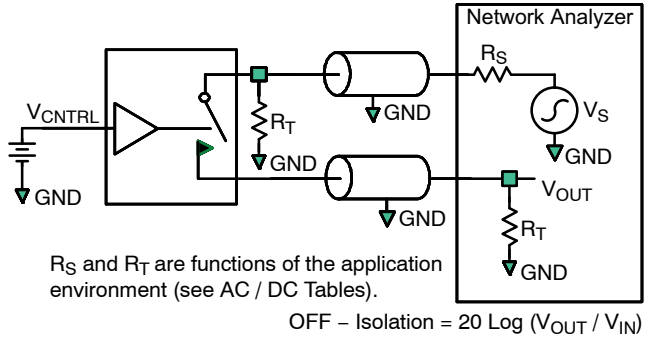


Figure 11. Channel Off Isolation

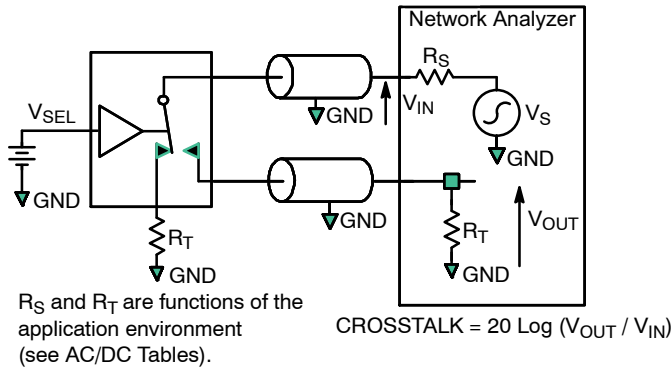


Figure 12. Adjacent Channel Crosstalk

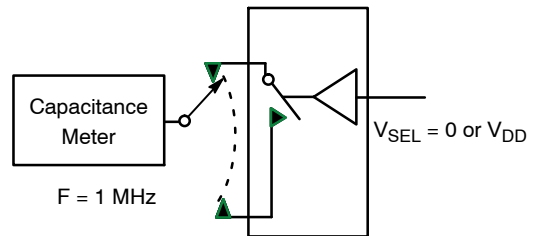


Figure 13. Channel Off Capacitance

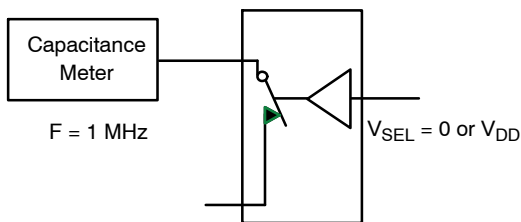


Figure 14. Channel On Capacitance

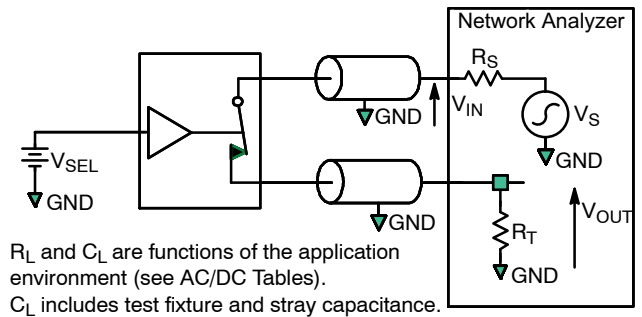


Figure 15. Total Harmonic Distortion (THD+N)



**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

---

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)