GigaDevice Semiconductor Inc.

GD32F190xx
ARM® Cortex®-M3 32-bit MCU

Datasheet

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1. General description

The GD32F190xx device belongs to the 5V value line of GD32 MCU family. It is a 32-bit general-purpose microcontroller based on the high performance ARM® Cortex®-M3 RISC core with best ratio in terms of processing power, reduced power consumption and peripheral set. The Cortex®-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The GD32F190xx device incorporates the ARM® Cortex®-M3 32-bit processor core operating at 72 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 64 KB on-chip Flash memory and up to 8 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to five general 16-bit timers, a general 32-bit timer, a basic timer, a PWM advanced timer, as well as standard and advanced communication interfaces: up to three SPIs, three I2Cs and two USARTs, two I2Ss, two CANs with a CAN PHY, and a segment LCD controller. Advanced analog peripherals including one 12-bit ADC, two 12-bit DACs, three OPAs and two comparators.

The device operates from a 2.5 to 5.5V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32F190xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, home appliances, E-bike and so on.

2. Device overview

2.1. Device information

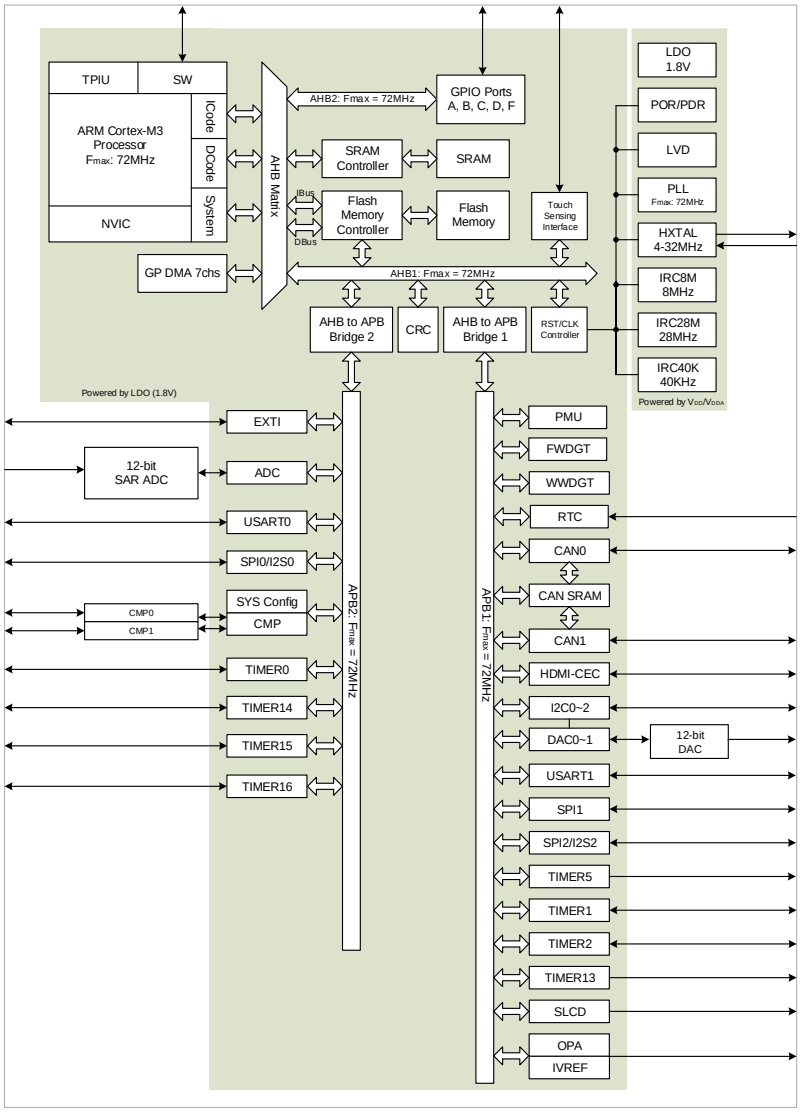
Table 2-1. GD32F190xx devices features and peripheral list

Part Number		GD32F190xx								
		T4	T6	T8	C4	C6	C8	R4	R6	R8
Flash (KB)		16	32	64	16	32	64	16	32	64
SRAM (KB)		4	6	8	4	6	8	4	6	8
Timers	General timer(32-bit)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)
	General timer(16-bit)	5 (2,13-16)	5 (2,13-16)	5 (2,13-16)	5 (2,13-16)	5 (2,13-16)	5 (2,13-16)	5 (2,13-16)	5 (2,13-16)	5 (2,13-16)
	Advanced timer(16-bit)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
	Basic timer (16-bit)	1 (5)	1 (5)	1 (5)	1 (5)	1 (5)	1 (5)	1 (5)	1 (5)	1 (5)
	SysTick	1	1	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1
Connectivity	USART	1 (0)	2 (0-1)	2 (0-1)	1 (0)	2 (0-1)	2 (0-1)	1 (0)	2 (0-1)	2 (0-1)
	I2C	1 (0)	1 (0)	3 (0-2)	1 (0)	1 (0)	3 (0-2)	1 (0)	1 (0)	3 (0-2)
	SPI	1 (0)	1 (0)	3 (0-2)	1 (0)	1 (0)	3 (0-2)	1 (0)	1 (0)	3 (0-2)
	I2S	1 (0)	1 (0)	2 (0,2)	1 (0)	1 (0)	2 (0,2)	1 (0)	1 (0)	2 (0,2)
	CAN	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)
	SLCD	0	0	0	4x18	4x18	4x18	8x32	8x32	8x32
GPIO		28	28	28	39	39	39	55	55	55
TSI (Channels)		14	14	14	17	17	17	18	18	18
OPA		2	2	2	2	2	2	3	3	3

Part Number		GD32F190xx								
		T4	T6	T8	C4	C6	C8	R4	R6	R8
CMP		2	2	2	2	2	2	2	2	2
EXTI		16	16	16	16	16	16	16	16	16
ADC	Units	1	1	1	1	1	1	1	1	1
	Channels (External)	10	10	10	10	10	10	16	16	16
	Channels (Internal)	3	3	3	3	3	3	3	3	3
DAC		2	2	2	2	2	2	2	2	2
Package		QFN36			LQFP48			LQFP64		

2.2. Block diagram

Figure 2-1. GD32F190xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32F190Rx LQFP64 pinouts

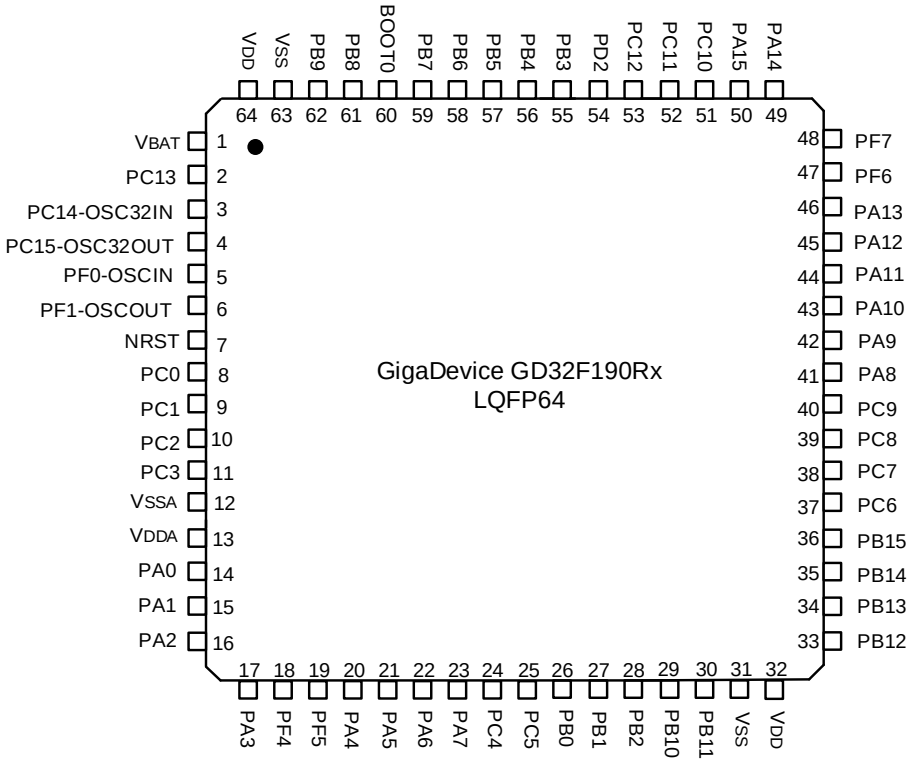


Figure 2-3. GD32F190Cx LQFP48 pinouts

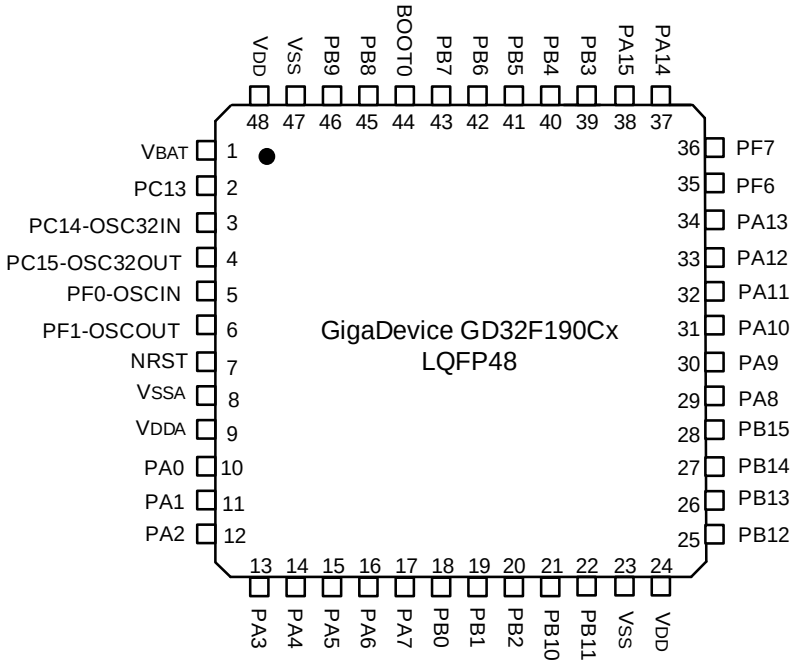
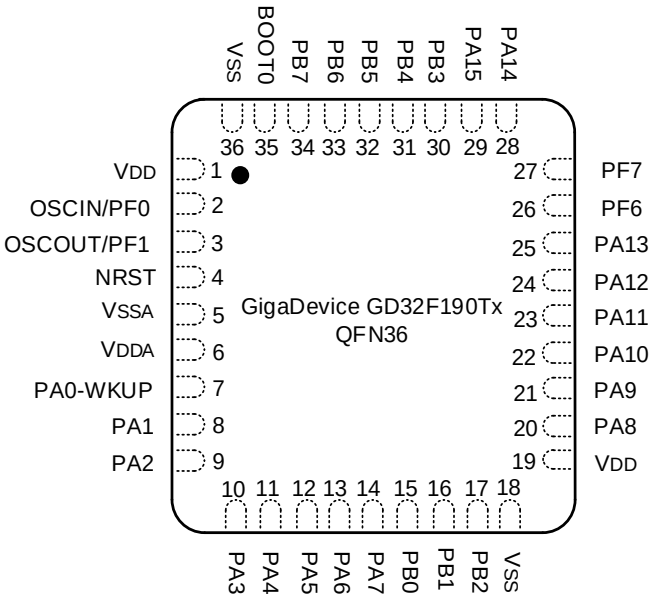


Figure 2-4. GD32F190Tx QFN36 pinouts



2.4. Memory map

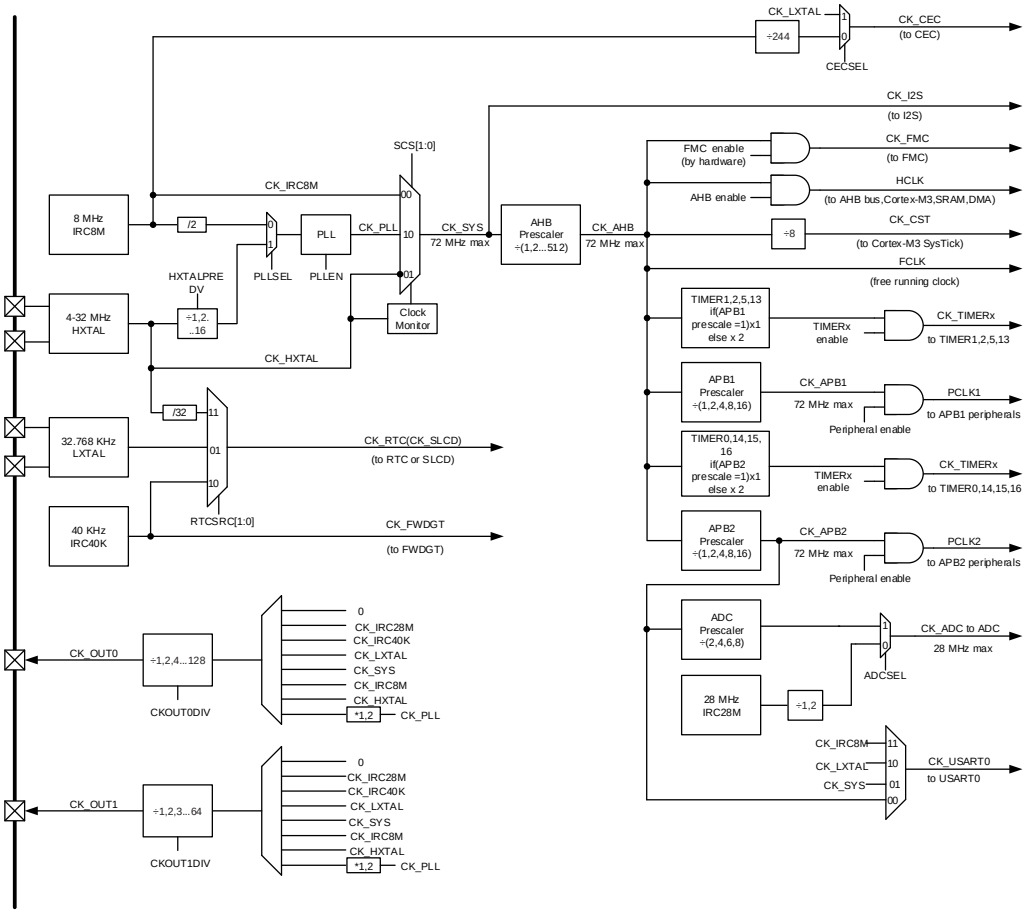
Table 2-2. GD32F190xx memory map

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0xE000 0000 - 0xE00F FFFF	Cortex-M3 internal peripherals
External Device		0xA000 0000 - 0xDFFF FFFF	Reserved
External RAM		0x6000 0000 - 0x9FFF FFFF	Reserved
Peripherals	AHB1	0x5000 0000 - 0x5FFF FFFF	Reserved
	AHB2	0x4800 1800 - 0x4FFF FFFF	Reserved
		0x4800 1400 - 0x4800 17FF	GPIOF
		0x4800 1000 - 0x4800 13FF	Reserved
		0x4800 0C00 - 0x4800 0FFF	GPIOD
		0x4800 0800 - 0x4800 0BFF	GPIOC
		0x4800 0400 - 0x4800 07FF	GPIOB
		0x4800 0000 - 0x4800 03FF	GPIOA
	AHB1	0x4002 4400 - 0x47FF FFFF	Reserved
		0x4002 4000 - 0x4002 43FF	TSI
		0x4002 3400 - 0x4002 3FFF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1400 - 0x4002 1FFF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0400 - 0x4002 0FFF	Reserved
		0x4002 0000 - 0x4002 03FF	DMA
	APB2	0x4001 4C00 - 0x4001 FFFF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER16
		0x4001 4400 - 0x4001 47FF	TIMER15
		0x4001 4000 - 0x4001 43FF	TIMER14
		0x4001 3C00 - 0x4001 3FFF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	Reserved
		0x4001 3000 - 0x4001 33FF	SPI0/I2S0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	Reserved
		0x4001 2400 - 0x4001 27FF	ADC
		0x4001 0800 - 0x4001 23FF	Reserved
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	SYSCFG+CMP
	APB1	0x4000 C400 - 0x4000 FFFF	Reserved
		0x4000 C000 - 0x4000 C3FF	I2C2

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0x4000 8000 - 0x4000 BFFF	Reserved
		0x4000 7C00 - 0x4000 7FFF	OPA+IVREF
		0x4000 7800 - 0x4000 7BFF	CEC
		0x4000 7400 - 0x4000 77FF	DAC0~1
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6C00 - 0x4000 6FFF	Reserved
		0x4000 6800 - 0x4000 6BFF	CAN1
		0x4000 6400 - 0x4000 67FF	CAN0
		0x4000 6000 - 0x4000 63FF	CAN SRAM
		0x4000 5C00 - 0x4000 5FFF	Reserved
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 4800 - 0x4000 53FF	Reserved
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	SPI2/I2S2
		0x4000 3800 - 0x4000 3BFF	SPI1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	SLCD
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 1400 - 0x4000 1FFF	Reserved
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0800 - 0x4000 0FFF	Reserved
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM		0x2000 5000 - 0x3FFF FFFF	Reserved
		0x2000 0000 - 0x2000 4FFF	SRAM
Code		0x1FFF F80F - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF F80E	Option bytes
		0x1FFF EC00 - 0x1FFF F7FF	System memory
		0x0800 FFFF - 0x1FFF EBFF	Reserved
		0x0800 0000 - 0x0800 FFFE	Main Flash memory
		0x0000 0000 - 0x07FF FFFF	Aliased to Flash or system memory

2.5. Clock tree

Figure 2-5. GD32F190xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillators

IRC40K: Internal 40K RC oscillator

IRC28M: Internal 28M RC oscillators

2.6. Pin definitions

2.6.1. GD32F190Rx LQFP64 pin definitions

Table 2-3. GD32F190Rx LQFP64 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{SLCD}/V_{BAT}	1	P		Default: V_{SLCD}/V_{BAT}
PC13-TAMPER-RTC	2	I/O		Default: PC13 Additional: RTC_TAMP0, RTC_TS, RTC_OUT, WKUP1
PC14-OSC32IN	3	I/O		Default: PC14 Additional: OSC32IN
PC15-OSC32OUT	4	I/O		Default: PC15 Additional: OSC32OUT
PF0-OSCIN	5	I/O	HVT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	6	I/O	HVT	Default: PF1 Additional: OSCOUT
NRST	7	I/O		Default: NRST
PC0	8	I/O		Default: PC0 Alternate: EVENTOUT, I2C2_SCL(5), SLCD_SEG18 Additional: ADC_IN10
PC1	9	I/O		Default: PC1 Alternate: EVENTOUT, I2C2_SDA(5), SLCD_SEG19 Additional: ADC_IN11, OPA2_VINP
PC2	10	I/O		Default: PC2 Alternate: EVENTOUT, I2C2_SMBA(5), SLCD_SEG20 Additional: ADC_IN12, OPA2_VINM
PC3	11	I/O		Default: PC3 Alternate: EVENTOUT Additional: ADC_IN13, OPA2_VOUT, SLCD_SEG21, I2C2_TXFRAME(5)
V_{SSA}	12	P		Default: V_{SSA}
V_{DDA}	13	P		Default: V_{DDA}
PA0-WKUP	14	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5), CMP0_OUT, TSI_G1_IO1 Additional: ADC_IN0, RTC_TAMP1, WKUP0, CMP0_IM6
PA1	15	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT, SLCD_SEG0, TSI_G0_IO1 Additional: ADC_IN1, CMP0_IP, OPA0_VINP

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PA2	16	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0, SLCD_SEG1, CMP1_OUT, TSC_G0_IO2, I2C1_SMBA(5) Additional: ADC_IN2, CMP1_IM6, OPA0_VINM
PA3	17	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1, SLCD_SEG2, TSI_G0_IO3, I2C1_TXFRAME(5) Additional: ADC_IN3, CMP1_IP, OPA0_VOUT
PF4	18	I/O	HVT	Default: PF4 Alternate: EVENTOUT, SLCD_SEG28
PF5	19	I/O	HVT	Default: PF5 Alternate: EVENTOUT, SLCD_SEG29
PA4	20	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5), I2S0_WS, TSI_G1_IO0, SPI2_NSS(5), I2S2_WS(5) Additional: ADC_IN4, CMP0_IM4, CMP1_IM4, DAC0_OUT
PA5	21	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI, I2S0_CK, CEC, TSI_G1_IO1 Additional: ADC_IN5, CMP0_IM5, CMP1_IM5, DAC1_OUT, CANH
PA6	22	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT, I2S0_MCK, CMP0_OUT, TSI_G1_IO2, SLCD_SEG3 Additional: ADC_IN6, OPA1_VINP, CANL
PA7	23	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT, I2S0_SD, CMP1_OUT, TSI_G1_IO3, SLCD_SEG4 Additional: ADC_IN7, OPA1_VINM
PC4	24	I/O		Default: PC4 Alternate: EVENTOUT, SLCD_SEG22 Additional: ADC_IN14
PC5	25	I/O		Default: PC5 Alternate: TSI_G2_IO0, SLCD_SEG23 Additional: ADC_IN15
PB0	26	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT TSI_G2_IO1, SPI2_NSS(5), I2S2_WS(5), SLCD_SEG5 Additional: ADC_IN8, VSLCD_Rail3, IREF,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				OPA1_VOUT
PB1	27	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5), TSI_G2_IO2, SLCD_SEG6 Additional: ADC_IN9, VREF
PB2	28	I/O	HVT	Default: PB2 Alternate: TSI_G2_IO3 Additional: VSLCD_Rail2
PB10	29	I/O	HVT	Default: PB10 Alternate: I2C1_SCL(5), CEC, TIMER1_CH2, TSITG, I2C0_SCL(3), SLCD_SEG10, SPI1_IO2(5)
PB11	30	I/O	HVT	Default: PB11 Alternate: I2C1_SDA(5), TIMER1_CH3, EVENTOUT, TSI_G5_IO0, I2C0_SDA(3), SLCD_SEG11, SPI1_IO3(5)
V_{SS}	31	P		Default: V_{SS}
V_{DD}	32	P		Default: V_{DD}
PB12	33	I/O	HVT	Default: PB12 Alternate: SPI0_NSS(3), SPI1_NSS(5), TIMER0_BRKIN, I2C1_SMBA(5), EVENTOUT, TSI_G5_IO1, SLCD_SEG12, CAN1_RX Additional: VSLCD_Rail1
PB13	34	I/O	HVT	Default: PB13 Alternate: SPI0_SCK(3), SPI1_SCK(5), TIMER0_CH0_ON, TSI_G5_IO2, SLCD_SEG13, I2C1_TXFRAME(5), CAN1_TX
PB14	35	I/O	HVT	Default: PB14 Alternate: SPI0_MISO(3), SPI1_MISO(5), TIMER0_CH1_ON, TIMER14_CH0 TSI_G5_IO3, SLCD_SEG14
PB15	36	I/O	HVT	Default: PB15 Alternate: SPI0_MOSI(3), SPI1_MOSI(5), TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1, SLCD_SEG15 Additional: RTC_REFIN
PC6	37	I/O	HVT	Default: PC6 Alternate: TIMER2_CH0, SLCD_SEG24, I2C2_TXFRAME(5)
PC7	38	I/O	HVT	Default: PC7 Alternate: TIMER2_CH1, I2C2_SCL(5), SLCD_SEG25
PC8	39	I/O	HVT	Default: PC8 Alternate: TIMER2_CH2, I2C2_SDA(5), SLCD_SEG26
PC9	40	I/O	HVT	Default: PC9

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: TIMER2_CH3, I2C2_SMBA(5), SLCD_SEG27, CK_OUT1
PA8	41	I/O	HVT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, USART1_TX(4), EVENTOUT, SLCD_COM0, I2C0_TXFRAME
PA9	42	I/O	HVT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL, TSI_G3_IO0, SLCD_COM1, SPI1_IO2(5)
PA10	43	I/O	HVT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA, TSI_G3_IO1, SLCD_COM2, SPI1_IO3(5)
PA11	44	I/O	HVT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT, CMP0_OUT, TSI_G3_IO2, CAN0_RX
PA12	45	I/O	HVT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT, CMP1_OUT, TSI_G3_IO3, CAN0_TX
PA13	46	I/O	HVT	Default: PA13/SWDIO Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5), I2C0_SMBA
PF6	47	I/O	HVT	Default: PF6 Alternate: I2C1_SCL(5), I2C0_SCL(3), SLCD_SEG30
PF7	48	I/O	HVT	Default: PF7 Alternate: I2C1_SDA(5), I2C0_SDA(3), SLCD_SEG31
PA14	49	I/O	HVT	Default: PA14/SWCLK Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	50	I/O	HVT	Default: PA15 Alternate: SPI0_NSS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS(5), EVENTOUT, I2S0_WS, SPI2_NSS(5), I2S2_WS(5), SLCD_SEG17, I2C0_SMBA
PC10	51	I/O	HVT	Default: PC10 Alternate: SPI2_SCK(5), I2S2_CK(5), SLCD_COM4, SLCD_SEG28
PC11	52	I/O	HVT	Default: PC11 Alternate: SPI2_MISO(5), I2S2_MCK(5), SLCD_COM5, SLCD_SEG29
PC12	53	I/O	HVT	Default: PC12 Alternate: SPI2_MOSI(5), I2S2_SD(5), SLCD_COM6, SLCD_SEG30
PD2	54	I/O	HVT	Default: PD2 Alternate: TIMER2_ETI, SLCD_COM7, SLCD_SEG31

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PB3	55	I/O	HVT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT, I2S0_CK, TSI_G4_IO0, SPI2_SCK(5), I2S2_CK(5), SLCD_SEG7, I2C0_TXFRAME
PB4	56	I/O	HVT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT, I2S0_MCK, TSI_G4_IO1, SPI2_MISO(5), I2S2_MCK(5), SLCD_SEG8, I2C2_SMBA(5)
PB5	57	I/O	HVT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1, I2S0_SD, SPI2_MOSI(5), I2S2_SD(5), SLCD_SEG9, I2C2_TXFRAME(5), CAN1_RX
PB6	58	I/O	HVT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON, TSI_G4_IO2, I2C2_SCL(5), CAN1_TX
PB7	59	I/O	HVT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON, TSI_G4_IO3, I2C2_SDA(5)
BOOT0	60	I		Default: BOOT0
PB8	61	I/O	HVT	Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0, CEC, TSITG, SLCD_SEG16, CAN0_RX
PB9	62	I/O	HVT	Default: PB9 Alternate: I2C0_SDA, IFRP_OUT, TIMER16_CH0, EVENTOUT, SLCD_COM3, CAN0_TX
V_{SS}	63	P		Default: V_{SS}
V_{DD}	64	P		Default: V_{DD}

Notes:

(1) cType: I = input, O = output, P = power.

(2) I/O Level: HVT = High Voltage Tolerant.

(3) Functions are available on GD32F190R4 devices only.

(4) Functions are available on GD32F190R8/6 devices.

(5) Functions are available on GD32F190R8 devices.

2.6.2. GD32F190Cx LQFP48 pin definitions

Table 2-4. GD32F190Cx LQFP48 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{SLCD}/V_{BAT}	1	P		Default: V_{SLCD}/V_{BAT}
PC13-TAMPER-RTC	2	I/O		Default: PC13 Additional: RTC_TAMP0, RTC_TS, RTC_OUT, WKUP1
PC14-OSC32IN	3	I/O		Default: PC14 Additional: OSC32IN
PC15-OSC32OUT	4	I/O		Default: PC15 Additional: OSC32OUT
PF0-OSCIN	5	I/O	HVT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	6	I/O	HVT	Default: PF1 Additional: OSCOUT
NRST	7	I/O		Default: NRST
V_{SSA}	8	P		Default: V_{SSA}
V_{DDA}	9	P		Default: V_{DDA}
PA0-WKUP	10	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5), CMP0_OUT, TSI_G1_IO1 Additional: ADC_IN0, RTC_TAMP1, WKUP0, CMP0_IM6
PA1	11	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT, SLCD_SEG0, TSI_G0_IO1 Additional: ADC_IN1, CMP0_IP, OPA0_VINP
PA2	12	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0, SLCD_SEG1, CMP1_OUT, TSC_G0_IO2, I2C1_SMBA(5) Additional: ADC_IN2, CMP1_IM6, OPA0_VINM
PA3	13	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1, SLCD_SEG2, TSI_G0_IO3, I2C1_TXFRAME(5) Additional: ADC_IN3, CMP1_IP, OPA0_VOUT
PA4	14	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5), I2S0_WS, TSI_G1_IO0, SPI2_NSS(5), I2S2_WS(5) Additional: ADC_IN4, CMP0_IM4, CMP1_IM4, DAC0_OUT
PA5	15	I/O		Default: PA5

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI, I2S0_CK, CEC, TSI_G1_IO1 Additional: ADC_IN5, CMP0_IM5, CMP1_IM5, DAC1_OUT, CANH
PA6	16	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT, I2S0_MCK, CMP0_OUT, TSI_G1_IO2, SLCD_SEG3 Additional: ADC_IN6, OPA1_VINP, CANL
PA7	17	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT, I2S0_SD, CMP1_OUT, TSI_G1_IO3, SLCD_SEG4 Additional: ADC_IN7, OPA1_VINM
PB0	18	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT, TSI_G2_IO1, SPI2_NSS(5), I2S2_WS(5), SLCD_SEG5 Additional: ADC_IN8, VSLCD_Rail3, IREF, OPA1_VOUT
PB1	19	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5), TSI_G2_IO2, SLCD_SEG6 Additional: ADC_IN9, VREF
PB2	20	I/O	HVT	Default: PB2 Alternate: TSI_G2_IO3 Additional: VSLCD_Rail2
PB10	21	I/O	HVT	Default: PB10 Alternate: I2C1_SCL(5), CEC, TIMER1_CH2, TSITG, I2C0_SCL(3), SLCD_SEG10, SPI1_IO2(5)
PB11	22	I/O	HVT	Default: PB11 Alternate: I2C1_SDA(5), TIMER1_CH3, EVENTOUT, TSI_G5_IO0, I2C0_SDA(3), SLCD_SEG11, SPI1_IO3(5)
V_{SS}	23	P		Default: V_{SS}
V_{DD}	24	P		Default: V_{DD}
PB12	25	I/O	HVT	Default: PB12 Alternate: SPI0_NSS(3), SPI1_NSS(5), TIMER0_BRKIN, I2C1_SMBA(5), EVENTOUT, TSI_G5_IO1, SLCD_SEG12, CAN1_RX Additional: VSLCD_Rail1
PB13	26	I/O	HVT	Default: PB13 Alternate: SPI0_SCK(3), SPI1_SCK(5), TIMER0_CH0_ON, TSI_G5_IO2, SLCD_SEG13, I2C1_TXFRAME(5), CAN1_TX
PB14	27	I/O	HVT	Default: PB14

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: SPI0_MISO(3), SPI1_MISO(5), TIMER0_CH1_ON, TIMER14_CH0, TSI_G5_IO3, SLCD_SEG14
PB15	28	I/O	HVT	Default: PB15 Alternate: SPI0_MOSI(3), SPI1_MOSI(5), TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1, SLCD_SEG15 Additional: RTC_REFIN
PA8	29	I/O	HVT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, USART1_TX(4), EVENTOUT, SLCD_COM0, I2C0_TXFRAME
PA9	30	I/O	HVT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL, TSI_G3_IO0, SLCD_COM1, SPI1_IO2(5)
PA10	31	I/O	HVT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA, TSI_G3_IO1, SLCD_COM2, SPI1_IO3(5)
PA11	32	I/O	HVT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT, CMP0_OUT, TSI_G3_IO2, CAN0_RX
PA12	33	I/O	HVT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT, CMP1_OUT, TSI_G3_IO3, CAN0_TX
PA13	34	I/O	HVT	Default: PA13/SWDIO Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5), I2C0_SMBA
PF6	35	I/O	HVT	Default: PF6 Alternate: I2C1_SCL(5), I2C0_SCL(3), SLCD_SEG30
PF7	36	I/O	HVT	Default: PF7 Alternate: I2C1_SDA(5), I2C0_SDA(3), SLCD_SEG31
PA14	37	I/O	HVT	Default: PA14/SWCLK Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	38	I/O	HVT	Default: PA15 Alternate: SPI0_NSS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS(5), EVENTOUT, I2S0_WS, SPI2_NSS(5), I2S2_WS(5), SLCD_SEG17, I2C0_SMBA
PB3	39	I/O	HVT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT, I2S0_CK, TSI_G4_IO0, SPI2_SCK(5), I2S2_CK(5), SLCD_SEG7, I2C0_TXFRAME

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PB4	40	I/O	HVT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT, I2S0_MCK, TSI_G4_IO1, SPI2_MISO(5), I2S2_MCK(5), SLCD_SEG8, I2C2_SMBA(5)
PB5	41	I/O	HVT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1, I2S0_SD, SPI2_MOSI(5), I2S2_SD(5), SLCD_SEG9, I2C2_TXFRAME(5), CAN1_RX
PB6	42	I/O	HVT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON, TSI_G4_IO2, I2C2_SCL(5), CAN1_TX
PB7	43	I/O	HVT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON, TSI_G4_IO3, I2C2_SDA(5)
BOOT0	44	I		Default: BOOT0
PB8	45	I/O	HVT	Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0, CEC, TSITG, SLCD_SEG16, CAN0_RX
PB9	46	I/O	HVT	Default: PB9 Alternate: I2C0_SDA, IFRP_OUT, TIMER16_CH0, EVENTOUT, SLCD_COM3, CAN0_TX
V_{SS}	47	P		Default: V_{SS}
V_{DD}	48	P		Default: V_{DD}

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: I/O Level: HVT = High Voltage Tolerant.

(3) Functions are available on GD32F190C4 devices only.

(4) Functions are available on GD32F190C8/6 devices.

(5) Functions are available on GD32F190C8 devices.

2.6.3. GD32F190Tx QFN36 pin definitions

Table 2-5. GD32F190Tx QFN36 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
V_{DD}	1	P		Default: V_{DD}
PF0-OSCIN	2	I/O	HVT	Default: PF0 Additional: OSCIN
PF1-OSCOUT	3	I/O	HVT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{SSA}	5	P		Default: V_{SSA}
V_{DDA}	6	P		Default: V_{DDA}
PA0-WKUP	7	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, I2C1_SCL(5), CMP0_OUT, TSI_G1_IO1 Additional: ADC_IN0, RTC_TAMP1, WKUP0, CMP0_IM6
PA1	8	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, I2C1_SDA(5), EVENTOUT, SLCD_SEG0, TSI_G0_IO1 Additional: ADC_IN1, CMP0_IP, OPA0_VINP
PA2	9	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0, SLCD_SEG1, CMP1_OUT, TSC_G0_IO2, I2C1_SMBA(5) Additional: ADC_IN2, CMP1_IM6, OPA0_VINM
PA3	10	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1, SLCD_SEG2, TSI_G0_IO3, I2C1_TXFRAME(5) Additional: ADC_IN3, CMP1_IP, OPA0_VOUT
PA4	11	I/O		Default: PA4 Alternate: SPI0_NSS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5), I2S0_WS, TSI_G1_IO0, SPI2_NSS(5), I2S2_WS(5) Additional: ADC_IN4, CMP0_IM4, CMP1_IM4, DAC0_OUT
PA5	12	I/O		Default: PA5 Alternate: SPI0_SCK, TIMER1_CH0, TIMER1_ETI, I2S0_CK, CEC, TSI_G1_IO1 Additional: ADC_IN5, CMP0_IM5, CMP1_IM5, DAC1_OUT, CANH
PA6	13	I/O		Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN,

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				TIMER15_CH0, EVENTOUT, I2S0_MCK, CMP0_OUT, TSI_G1_IO2, SLCD_SEG3 Additional: ADC_IN6, OPA1_VINP, CANL
PA7	14	I/O		Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT, I2S0_SD, CMP1_OUT, TSI_G1_IO3, SLCD_SEG4 Additional: ADC_IN7, OPA1_VINM
PB0	15	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(4), EVENTOUT, TSI_G2_IO1, SPI2_NSS(5), I2S2_WS(5), SLCD_SEG5 Additional: ADC_IN8, VSLCD_Rail3, IREF, OPA1_VOUT
PB1	16	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5), TSI_G2_IO2, SLCD_SEG6 Additional: ADC_IN9, VREF
PB2	17	I/O	HVT	Default: PB2 Alternate: TSI_G2_IO3 Additional: VSLCD_Rail2
V_{SS}	18	P		Default: V_{SS}
V_{DD}	19	P		Default: V_{DD}
PA8	20	I/O	HVT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, USART1_TX(4), EVENTOUT, SLCD_COM0, I2C0_TXFRAME
PA9	21	I/O	HVT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, I2C0_SCL, TSI_G3_IO0, SLCD_COM1, SPI1_IO2(5)
PA10	22	I/O	HVT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA, TSI_G3_IO1, SLCD_COM2, SPI1_IO3(5)
PA11	23	I/O	HVT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT, CMP0_OUT, TSI_G3_IO2, CAN0_RX
PA12	24	I/O	HVT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT, CMP1_OUT, TSI_G3_IO3, CAN0_TX
PA13	25	I/O	HVT	Default: PA13/SWDIO Alternate: IFRP_OUT, SWDIO,SPI1_MISO(5), I2C0_SMBA
PF6	26	I/O	HVT	Default: PF6

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: I2C1_SCL(5), I2C0_SCL(3), SLCD_SEG30
PF7	27	I/O	HVT	Default: PF7 Alternate: I2C1_SDA(5), I2C0_SDA(3), SLCD_SEG31
PA14	28	I/O	HVT	Default: PA14/SWCLK Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)
PA15	29	I/O	HVT	Default: PA15 Alternate: SPI0_NSS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS(5), EVENTOUT, I2S0_WS, SPI2_NSS(5), I2S2_WS(5), SLCD_SEG17, I2C0_SMBA
PB3	30	I/O	HVT	Default: PB3 Alternate: SPI0_SCK, TIMER1_CH1, EVENTOUT, I2S0_CK, TSI_G4_IO0, SPI2_SCK(5), I2S2_CK(5), SLCD_SEG7, I2C0_TXFRAME
PB4	31	I/O	HVT	Default: PB4 Alternate: SPI0_MISO, TIMER2_CH0, EVENTOUT, I2S0_MCK, TSI_G4_IO1, SPI2_MISO(5), I2S2_MCK(5), SLCD_SEG8, I2C2_SMBA(5)
PB5	32	I/O	HVT	Default: PB5 Alternate: SPI0_MOSI, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1, I2S0_SD, SPI2_MOSI(5), I2S2_SD(5), SLCD_SEG9, I2C2_TXFRAME(5), CAN1_RX
PB6	33	I/O	HVT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON, TSI_G4_IO2, I2C2_SCL(5), CAN1_TX
PB7	34	I/O	HVT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON, TSI_G4_IO3, I2C2_SDA(5)
BOOT0	35	I		Default: BOOT0
V_{SS}	36	P		Default: V_{SS}

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: HVT = High Voltage Tolerant.

(3) Functions are available on GD32F190T4 devices only.

(4) Functions are available on GD32F190T8/6 devices.

(5) Functions are available on GD32F190T8 devices.

2.6.4. GD32F190xx pin alternate functions

Table 2-6. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF9	AF11
PA0		USART0_CTS(1) USART1_CTS(2)	TIMER1_CH0, TIMER1_ETI	TSI_G0_IO0	I2C1_SCL(3)			CMP0_OUT		
PA1	EVENTOUT	USART0_RTS(1) USART1_RTS(2)	TIMER1_CH1	TSI_G0_IO1	I2C1_SDA(3)					SLCD_SEG0
PA2	TIMER14_CH0	USART0_TX(1) USART1_TX(2)	TIMER1_CH2	TSI_G0_IO2	I2C1_SMBA(3)			CMP1_OUT		SLCD_SEG1
PA3	TIMER14_CH1	USART0_RX(1) USART1_RX(2)	TIMER1_CH3	TSI_G0_IO3	I2C1_TXFRAME(3)					SLCD_SEG2
PA4	SPI0_NSS I2S0_WS	USART0_CK(1) USART1_CK(2)		TSI_G1_IO0	TIMER13_CH0	SPI2_NSS/ I2S2_WS(3)	SPI1_NSS(3)			
PA5	SPI0_SCK I2S0_CK	CEC	TIMER1_CH0, TIMER1_ETI	TSI_G1_IO1						
PA6	SPI0_MISO I2S0_MCK	TIMER2_CH0	TIMER0_BRKIN	TSI_G1_IO2		TIMER15_CH0	EVENTOUT	CMP0_OUT		SLCD_SEG3
PA7	SPI0_MOSI I2S0_SD	TIMER2_CH1	TIMER0_CH0_ON	TSI_G1_IO3	TIMER13_CH0	TIMER16_CH0	EVENTOUT	CMP1_OUT		SLCD_SEG4
PA8	CK_OUT0	USART0_CK	TIMER0_CH0	EVENTOUT	USART1_TX(2)	I2C1_TXFRAME(3)				SLCD_COM0
PA9	TIMER14_BRKIN	USART0_TX	TIMER0_CH1	TSI_G3_IO0	I2C0_SCL		SPI1_IO2(3)			SLCD_COM1

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF9	AF11
PA10	TIMER16_BRKIN	USART0_RX	TIMER0_CH2	TSI_G3_IO1	I2C0_SDA		SPI1_IO3(3)			SLCD_COM2
PA11	EVENTOUT	USART0_CTS	TIMER0_CH3	TSI_G3_IO2				CMP0_OUT	CAN0_RX	
PA12	EVENTOUT	USART0_RTS	TIMER0_ETI	TSI_G3_IO3				CMP1_OUT	CAN0_TX	
PA13	SWDIO	IFRP_OUT				I2C0_SMBA	SPI1_MISO(3)			
PA14	SWCLK	USART0_TX(1) USART1_TX(2)					SPI1_MOSI(3)			
PA15	SPI0_NSS I2S0_WS	USART0_RX(1) USART1_RX(2)	TIMER1_CH0, TIMER1_ETI	EVENTOUT	I2C0_SMBA	SPI2_NSS/ I2S2_WS(3)	SPI1_NSS(3)			SLCD_SEG17

Notes:

(1) Functions are available on GD32F190x4 devices only.

(2) Functions are available on GD32F190x8/6 devices.

(3) Functions are available on GD32F190x8 devices.

Table 2-7. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF9	AF11
PB0	EVENTOUT	TIMER2_CH2	TIMER0_CH1_ON	TSI_G2_IO1	USART1_RX(2)	SPI2_NSS/ I2S2_WS(3)				SLCD_SEG5
PB1	TIMER13_CH0	TIMER2_CH3	TIMER0_CH2_ON	TSI_G2_IO2			SPI1_SCK(3)			SLCD_SEG6
PB2				TSI_G2_IO3						
PB3	SPI0_SCK I2S0_CK	EVETOUT	TIMER1_CH1	TSI_G4_IO0	I2C0_TXFRAME	SPI2_SCK/ I2S2_CK(3)				SLCD_SEG7
PB4	SPI0_MISO I2S0_MCK	TIMER2_CH0	EVENTOUT	TSI_G4_IO1	I2C2_SMBA(3)	SPI2_MISO/ I2S2_MCK(3)				SLCD_SEG8
PB5	SPI0_MOSI I2S0_SD	TIMER2_CH1	TIMER15_BRKIN	I2C0_SMBA	I2C2_TXFRAME(3)	SPI2_MOSI/ I2S2_SD(3)			CAN1_RX	SLCD_SEG9
PB6	USART0_TX	I2C0_SCL	TIMER15_CH0_ON	TSI_G4_IO2	I2C2_SCL(3)				CAN1_TX	
PB7	USART0_RX	I2C0_SDA	TIMER16_CH0_ON	TSI_G4_IO3	I2C2_SDA(3)					
PB8	CEC	I2C0_SCL	TIMER15_CH0	TSITG					CAN0_RX	SLCD_SEG16
PB9	IFRP_OUT	I2C0_SDA	TIMER16_CH0	EVENTOUT					CAN0_TX	SLCD_COM3
PB10	CEC	I2C0_SCL(1) I2C1_SCL(3)	TIMER1_CH2	TSITG			SPI1_IO2(3)			SLCD_SEG10
PB11	EVENTOUT	I2C0_SDA(1) I2C1_S	TIMER1_CH3	TSI_G5_IO0			SPI1_IO3(3)			SLCD_SEG11

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF9	AF11
		DA(3)								
PB12	SPI0_NSS(1) SPI1_NSS(3)	EVENTOUT	TIMER0_BRKIN	TSI_G5_IO1	I2C1_SMBA(3)				CAN1_RX	SLCD_SEG12
PB13	SPI0_SCK(1) SPI1_SCK(3)		TIMER0_CH0_ON	TSI_G5_IO2	I2C1_TXFRAME(3)				CAN1_TX	SLCD_SEG13
PB14	SPI0_MISO(1) SPI1_MISO(3)	TIMER14_CH0	TIMER0_CH1_ON	TSI_G5_IO3						SLCD_SEG14
PB15	SPI0_MOSI(1) SPI1_MOSI(3)	TIMER14_CH1	TIMER0_CH2_ON	TIMER14_CH0_ON						SLCD_SEG15

Notes:

(1) Functions are available on GD32F190x4 devices only.

(2) Functions are available on GD32F190x8/6 devices.

(3) Functions are available on GD32F190x8 devices.

Table 2-8. Port C & D & F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF9	AF11
PC0	EVENTOUT	I2C2_SCL(2)								SLCD_SEG18
PC1	EVENTOUT	I2C2_SDA(2)								SLCD_SEG19
PC2	EVENTOUT	I2C2_SMBA(2)								SLCD_SEG20
PC3	EVENTOUT	I2C2_TXFRAME(2)								SLCD_SEG21
PC4	EVENTOUT									SLCD_SEG22
PC5	TSI_G2_IO0									SLCD_SEG23
PC6	TIMER2_CH0	I2C2_TXFRAME(2)								SLCD_SEG24
PC7	TIMER2_CH1	I2C2_SCL(2)								SLCD_SEG25
PC8	TIMER2_CH2	I2C2_SDA(2)								SLCD_SEG26
PC9	TIMER2_CH3	I2C2_SMBA(2)		CK_OUT1						SLCD_SEG27
PC10	SPI2_SCK/ I2S2_CK(2)									SLCD_COM4, SLCD_SEG28
PC11	SPI2_MISO/ I2S2_MCK(2)									SLCD_COM5, SLCD_SEG29
PC12	SPI2_MOSI/ I2S2_SD(2)									SLCD_COM6, SLCD_SEG30
PD2	TIMER2_ETI									SLCD_COM7, SLCD_SEG31
PF4	EVENTOUT									SLCD_SEG28
PF5	EVENTOUT									SLCD_SEG29

PF6	I2C0_SCL(1) I2C1_SCL(2)									SLCD_SEG30
PF7	I2C0_SDA(1) I2C1_SDA(2)									SLCD_SEG31

Notes:

(1) Functions are available on GD32F190x4 devices only.

(2) Functions are available on GD32F190x8 devices.

3. Functional description

3.1. ARM® Cortex®-M3 core

The Cortex®-M3 processor is the latest generation of ARM® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

- 32-bit ARM® Cortex®-M3 processor core
- Up to 72 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

3.2. On-chip memory

- Up to 64 Kbytes of Flash memory
- Up to 8 Kbytes of SRAM with hardware parity checking

The ARM® Cortex®-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 64 Kbytes of inner Flash and 8 Kbytes of inner SRAM at most is available for storing programs and data, both accessed (R/W) at CPU clock speed with zero wait states. The ***Table 2-2. GD32F190xx memory map*** shows the memory map of the GD32F190xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator

- Integrated system clock PLL
- 2.5 to 5.5 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB and two APB domains is 72 MHz. See ***Figure 2-5. GD32F190xx clock tree*** for details on the clock tree.

GD32F1x0 Reset Control includes the control of three kinds of reset: power reset, system reset and backup domain reset. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller and the Backup domain. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.95V and down to 1.9V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.5 to 5.5 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{DDA} range: 2.5 to 5.5 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.8 to 5.5 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10) or USART1 (PA2 and PA3, PA14 and PA15).

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance

between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In deep-sleep mode, all clocks in the 1.8V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, the CMP0&1 output, the RTC tamper and Timestamp, the USART0 wakeup and the CEC wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.
- **Standby** mode
  In standby mode, the whole 1.8V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pin.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC engine with up to 2 MSPS conversion rate
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Conversion range: V_{SSA} to V_{DDA} (3.0 to 5.5 V)
- Temperature sensor

A 12-bit 2 MSPS multi-channel ADC are integrated in the device. It is a total of up to 16 multiplexed external channels with 2 internal channels for temperature sensor and voltage reference measurement. The conversion range is between 3.0 V < V_{DDA} < 5.5 V. An on-chip 16-bit hardware oversample scheme improves performances while off-loading the related computational burden from the MCU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages.

The ADC can be triggered from the events generated by the general timers (TIMERx=1,2,14) and the advanced timer (TIMER0) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

3.7. Digital to analog converter (DAC)

- Two 12-bit DACs converter of independent output channel
- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC channel is used to generate variable analog outputs. The DAC is designed with integrated resistor strings structure. The DAC channels can be triggered by the timer update outputs or EXTI with DMA support. The maximum output value of the DAC is V_{REF+}.

3.8. DMA

- 7 channel DMA controller
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs, DAC, I2Ss

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9. General-purpose inputs/outputs (GPIOs)

- Up to 55 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 55 general purpose I/O pins (GPIO) in GD32F190xx, named PA0 ~ PA15 and PB0 ~ PB15, PC0 ~ PC15, PD2, PF0, PF1, PF4-PF7 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.10. Timers and PWM generation

- One 16-bit advanced timer (TIMER0), one 32-bit general timer (TIMER1), five 16-bit general timers (TIMER2, TIMER13 ~ TIMER16), and one 16-bit basic timer (TIMER5)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, compare match output, generation of PWM waveform (edge-aligned and center-aligned Mode) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER13 ~ TIMER16 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5, is mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F190xx provides two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and a 8-bit prescaler, It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in stop and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11. Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with five 32-bit backup registers
- Calendar with sub-seconds, seconds, minutes, hours, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 1 ppm resolution for compensation of quartz crystal inaccuracy

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.

3.12. Inter-integrated circuit (I2C)

- Up to three I2Cs bus interfaces can support both master and slave mode with a frequency up to 400 KHz
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode
- Hardware support specifications of secure access and control module interface applied in validation for resident ID cards

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides transfer rate of up to 100 KHz in standard mode and up to 400 KHz in fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.13. Serial peripheral interface (SPI)

- Up to three SPIs interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking
- Quad wire configuration available in master mode (SPI1)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is only supported in SPI1.

3.14. Universal synchronous asynchronous receiver transmitter (USART)

- Up to two USARTs with operating frequency up to 9 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.15. Inter-IC sound (I2S)

- Up to two I2Ss bus Interfaces with sampling frequency from 8 KHz to 192 KHz, multiplexed with SPI0 and SPI2
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32F190xx contain a I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI0 and SPI2. The audio sampling frequency from 8 KHz to 192 KHz is supported with less than 0.5% accuracy error.

3.16. HDMI CEC

- Hardware support Consumer Electronics Control (CEC) protocol (HDMI standard rev1.4)

The CEC protocol provides high-level control functions between the audiovisual products linked with HDMI cables. GD32F190xx contain a HDMI-CEC controller which has an independent clock domain and can wake up the MCU from deep-sleep mode on data reception.

3.17. Touch sensing interface (TSI)

- Transfer sequence fully controlled by hardware
- 6 fully parallel groups implemented
- 18 IOs configurable for capacitive sensing Channel Pins and 6 for Sample Pins
- Configurable transfer sequence frequency
- Possible to implement the user specific transfer sequences
- Sequence end and error flags / configurable interrupts
- Spread spectrum function implemented

Capacitive sensing technology can be used for the detection of a finger (or any conductive object) presence near an electrode. The capacitive variation of the electrode introduced by the finger can be measured by charging and detecting the voltage across the sampling capacitor. GD32F190xx contain a hardware touch sensing interface (TSI) and only requires few external components to operate. The sensing channels are distributed over 6 analog I/O groups including: Group0 (PA0 ~ PA3), Group1 (PA4 ~ PA7), Group2 (PC5, PB0 ~ PB2), Group3 (PA9 ~ PA12), Group4 (PB3, PB4, PB6, PB7) and Group5 (PB11 ~ PB14).

3.18. Comparators (CMP)

- Two fast rail-to-rail low-power comparators with software configurable
- Programmable reference voltage (internal, external I/O or DAC output pin)

Two Comparators (CMP) are implemented within the devices. Both comparators can wake up from deep-sleep mode to generate interrupts and breaks for the timers and also can be combined as a window comparator. The internal voltage reference is also connected to ADC_IN17 input channel of the ADC.

3.19. Operational amplifiers (OPA)

- Rail-to-rail input and output voltage range
- Low input bias current, offset voltage and low power mode

GD32F190xx provides two operational amplifiers with external or internal follower routing

capability (or even amplifier and filter capability with external components). When one operational amplifier is selected, one external ADC channel is used to enable output measurement.

3.20. Segment LCD controller (SLCD)

- Configurable frame frequency
- Blinking of individual segments or all segments
- Double buffer up to 8x32 bits registers for SLCD_DATAx storage
- The contrast can also be adjusted by configuring dead time
- VSLCD rails decoupling capability

The SLCD controller directly drives LCD displays by creating the AC segment and common voltage signals automatically. It can drive the monochrome passive liquid crystal display (LCD) which composed of a plurality of segments (pixels or complete symbols) that can be converted to visible or invisible. The SLCD controller can support up to 32 segments and 8 commons.

3.21. Controller area network (CAN)

- Two CANs interface with communication frequency up to 1 Mbit/s
- Internal main PLL for USB CLK compliantly
- A hardware CAN PHY integrated (CAN0)

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 28 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others. The integrated hardware CAN PHY can be enabled by register setting and this mode only used for CAN0.

3.22. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.23. Package and operation temperature

- LQFP64 (GD32F190Rx), LQFP48 (GD32F190Cx) and QFN36 (GD32F190Tx)
- Operation temperature range: -40°C to +85°C (industrial level)

4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range	V_{SS} - 0.3	V_{SS} + 5.5	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 5.5	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 5.5	V
V_{IN}	Input voltage on 5V tolerant pin	V_{SS} - 0.3	V_{SS} + 7.5	V
	Input voltage on other I/O	V_{SS} - 0.3	5.5	V
I_{IO}	Maximum current for GPIO pins	—	25	mA
T_A	Operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C

4.2. Recommended DC characteristics

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	—	2.5	5.0	5.5	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.5	5.0	5.5	V
V_{BAT}	Battery supply voltage	—	2.0	—	5.5	V

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-3. Power consumption characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current (Run mode)	V_{DD}=V_{DDA}=5.0V, HXTAL=8MHz, System clock=72 MHz, All peripherals enabled	—	59.23	—	mA
		V_{DD}=V_{DDA}=5.0V, HXTAL=8MHz, System clock =72 MHz, All peripherals disabled	—	38.71	—	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		V_{DD}=V_{DDA}=5.0V, HXTAL=8MHz, System clock =48 MHz, All peripherals enabled	-—	40.46	—	mA
		V_{DD}=V_{DDA}=5.0V, HXTAL=8MHz, System Clock =48 MHz, All peripherals disabled	—	26.72	—	mA
	Supply current (Sleep mode)	V_{DD}=V_{DDA}=5.0V, HXTAL=8MHz, CPU clock off, System clock=72MHz, All peripherals enabled	—	35.17	—	mA
		V_{DD}=V_{DDA}=5.0V, HXTAL=8MHz, CPU clock off, System clock=72MHz, All peripherals disabled	—	13.00	—	mA
	Supply current (Deep-Sleep mode)	V_{DD}=V_{DDA}=5.0V, Regulator in run mode,IRC40K on, RTC on, All GPIOs analog mode	—	119.81	—	µA
		V_{DD}=V_{DDA}=5.0V, Regulator in low power mode,IRC40K on, RTC on, All GPIOs analog mode	—	105.35	—	µA
	Supply current (Standby mode)	V_{DD}=V_{DDA}=5.0V, LXTAL off,IRC40K on, RTC on	—	11.08	—	µA
		V_{DD}=V_{DDA}=5.0V, LXTAL off,IRC40K on, RTC off	—	10.56	—	µA
		V_{DD}=V_{DDA}=5.0V, LXTAL off,IRC40K off, RTC off	—	8.54	—	µA
I_{BAT}	Battery supply current	V_{DD} not available, V_{BAT}=5.5 V, LXTAL on with external crystal, RTC on, Higher driving	—	2.30	—	µA
		V_{DD} not available, V_{BAT}=5.0 V, LXTAL on with external crystal, RTC on, Higher driving	—	2.06	—	µA
		V_{DD} not available, V_{BAT}=3.3 V, LXTAL on with external crystal, RTC on, Higher driving	—	1.56	—	µA
		V_{DD} not available, V_{BAT}=2.5 V, LXTAL on with external crystal, RTC on, Higher driving	—	1.41	—	µA
		V_{DD} not available, V_{BAT}=5.0 V, LXTAL on with external crystal, RTC on, Lower driving	—	1.32	—	µA
		V_{DD} not available, V_{BAT}=3.3 V, LXTAL on with external crystal, RTC on, Lower driving	—	0.88	—	µA
		V_{DD} not available, V_{BAT}=2.5 V, LXTAL on with external crystal, RTC on, Lower driving	—	0.75	—	µA

4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in ***Table 4-4. EMS characteristics***, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-4. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = 5.0 V, T_A = +25 °C conforms to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	V_{DD} = 5.0 V, T_A = +25 °C conforms to IEC 61000-4-4	4A

EMI (Electromagnetic Interference) emission testing result is given in ***Table 4-5. EMI characteristics***, compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 4-5. EMI characteristics

Symbol	Parameter	Conditions	Tested frequency band	Conditions		Unit
				24M	48M	
S_{EMI}	Peak level	V_{DD} = 5.0 V, T_A = +25 °C, compliant with IEC 61967-2	0.1 to 2 MHz	<0	<0	dBµV
			2 to 30 MHz	-3.9	-2.8	
			30 to 130 MHz	-7.2	-8	
			130 MHz to 1GHz	-7	-7	

4.5. Power supply supervisor characteristics

Table 4-6. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold	—	1.87	1.94	2.01	V
V_{PDR}	Power down reset threshold		1.82	1.89	1.96	V
V_{HYST}	PDR hysteresis		—	0.05	—	V
$T_{RSTTEMP}$	Reset temporization		—	2	—	ms

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-7. ESD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25 °C; JESD22-A114	—	—	7000	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=25 °C; JESD22-C101	—	—	1000	V

Table 4-8. Static latch-up characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A=25 °C; JESD78	—	—	±200	mA
	V_{supply} over voltage		—	—	8.25	V

4.7. External clock characteristics

Table 4-9. High speed crystal oscillator (HXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	High Speed External oscillator (HXTAL) frequency	V_{DD}=5.0V	4	8	32	MHz
C_{HXTAL}	Recommended load capacitance on OSC_IN and OSC_OUT	—	—	20	30	pF
R_{FHXTAL}	Recommended external feedback resistor between XTALIN and XTALOUT	—	—	200	—	KΩ
D_{HXTAL}	HXTAL oscillator duty cycle	—	30	50	70	%
$I_{DDHXTAL}$	HXTAL oscillator operating current	V_{DD}=5.0V, T_A=25°C	—	1.7	—	mA
$t_{SUHXTAL}$	HXTAL oscillator startup time	V_{DD}=5.0V, T_A=25°C	—	2	—	ms

Table 4-10. Low speed crystal oscillator (LXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Low Speed External oscillator (LXTAL) frequency	V_{DD}=V_{BAT}=5.0V	—	32.768	1000	KHz
C_{LXTAL}	Recommended load capacitance on OSC32_IN and OSC32_OUT	—	—	—	15	pF
D_{LXTAL}	LXTAL oscillator duty cycle	—	30	50	70	%
$I_{DDLXTAL}$	LXTAL oscillator operating current	LXTALDRV[1:0]=00	—	0.7	—	µA
		LXTALDRV[1:0]=01	—	0.8	—	
		LXTALDRV[1:0]=10	—	1.1	—	
		LXTALDRV[1:0]=11	—	1.4	—	
$t_{SULXTAL}$	LXTAL oscillator startup time	V_{DD}=V_{BAT}=5.0V	—	3	—	s

4.8. Internal clock characteristics

Table 4-11. Internal 8M RC oscillators (IRC8M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	High Speed Internal Oscillator (IRC8M) frequency	V_{DD}=5.0V	—	8	—	MHz
ACC_{IRC8M}	IRC8M oscillator Frequency accuracy, Factory-trimmed	V_{DD}=5.0V, T_A=-40°C ~+105°C	-3.5	—	+3.0	%
		V_{DD}=5.0V, T_A=0°C ~ +85°C	-2.0	—	+2.0	%
		V_{DD}=5.0V, T_A=25°C	-1.0	—	+1.0	%
D_{IRC8M}	IRC8M oscillator duty cycle	V_{DD}=5.0V, f_{IRC8M}=8MHz	48	50	52	%
$I_{DDIRC8M}$	IRC8M oscillator operating current	V_{DD}=5.0V, f_{IRC8M}=8MHz	—	80	100	μA
$t_{SUIRC8M}$	IRC8M oscillator startup time	V_{DD}=5.0V, f_{IRC8M}=8MHz	1	—	2	us

Table 4-12. Voltage values and corresponding IRC8M standard

Value	Standard
5.5V	8.29 MHz ±1%
5V	8.00 MHz ±1%
3.3V	7.52 MHz ±1%
3V	7.54 MHz ±1%
2.5V	7.57 MHz ±1%

Note:

GD32F190 IRC8M was trimmed in 5V, if other voltage value is needed to use in ***Table 4-12. Voltage values and corresponding IRC8M standard***, please calibrate the IRC8M value by manual.

Table 4-13. Internal 40K RC oscillator (IRC40K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC40K}	Low Speed Internal oscillator (IRC40K) frequency	V_{DD}=V_{BAT}=5.0V, T_A=-40°C ~ +85°C	30	40	60	KHz
$I_{DDIRC40K}$	IRC40K oscillator operating current	V_{DD}=V_{BAT}=5.0V, T_A=25°C	—	1	2	μA
$t_{SUIRC40K}$	IRC40K oscillator startup time	V_{DD}=V_{BAT}=5.0V, T_A=25°C	—	—	80	μs

4.9. PLL characteristics

Table 4-14. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency	—	1	8	25	MHz
f_{PLL}	PLL output clock frequency	—	16	—	72	MHz
t_{LOCK}	PLL lock time	—	—		200	μs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Jitter_{PLL}$	Cycle to cycle Jitter	—			300	ps

4.10. Memory characteristics

Table 4-15. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A=-40°C ~ +85°C	100	—	—	kcycles
t_{RET}	Data retention time	T_A=125°C	20	—	—	years
t_{PROG}	Word programming time	T_A=-40°C ~ +85°C	200	—	400	us
t_{ERASE}	Page erase time	T_A=-40°C ~ +85°C	60	100	450	ms
t_{MERASE}	Mass erase time	T_A=-40°C ~ +85°C	3.2	—	9.6	s

4.11. GPIO characteristics

Table 4-16. I/O port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage	V_{DD}=2.5V	—	—	0.83	V
		V_{DD}=3.3V	—	—	1.24	
		V_{DD}=5.0V	—	—	1.97	
		V_{DD}=5.5V	—	—	2.22	
	High Voltage tolerant IO Low level input voltage	V_{DD}=2.5V	—	—	0.65	V
		V_{DD}=3.3V	—	—	0.93	
		V_{DD}=5.0V	—	—	1.46	
		V_{DD}=5.5V	—	—	1.66	
V_{IH}	Standard IO High level input voltage	V_{DD}=2.5V	1.67	—	—	V
		V_{DD}=3.3V	2.01	—	—	
		V_{DD}=5.0V	2.91	—	—	
		V_{DD}=5.5V	3.13	—	—	
	High Voltage tolerant IO High level input voltage	V_{DD}=2.5V	1.42	—	—	V
		V_{DD}=3.3V	1.70	—	—	
		V_{DD}=5.0V	2.38	—	—	
		V_{DD}=5.5V	2.54	—	—	
V_{OL}	Low level output voltage	V_{DD}=2.5V, I_{IO}=8mA	—	—	0.29	V
		V_{DD}=3.3V, I_{IO}=8mA	—	—	0.22	
		V_{DD}=5.0V, I_{IO}=8mA	—	—	0.17	
		V_{DD}=5.5V, I_{IO}=8mA	—	—	0.16	
		V_{DD}=2.5V, I_{IO}=20mA	—	—	1.10	
		V_{DD}=3.3V, I_{IO}=20mA	—	—	0.59	
		V_{DD}=5.0V, I_{IO}=20mA	—	—	0.42	
		V_{DD}=5.5V, I_{IO}=20mA	—	—	0.40	
V_{OH}	High level output voltage	V_{DD}=2.5V, I_{IO}=8mA	2.24	—	—	V
		V_{DD}=3.3V, I_{IO}=8mA	3.12	—	—	
		V_{DD}=5.0V, I_{IO}=8mA	4.87	—	—	
		V_{DD}=5.5V, I_{IO}=8mA	5.37	—	—	
		V_{DD}=2.5V, I_{IO}=20mA	1.68	—	—	
		V_{DD}=3.3V, I_{IO}=20mA	2.80	—	—	
		V_{DD}=5.0V, I_{IO}=20mA	4.64	—	—	
		V_{DD}=5.5V, I_{IO}=20mA	5.17	—	—	
R_{PU}	Internal pull-up resistor	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Internal pull-down resistor	V_{IN}=V_{DD}	30	40	50	kΩ

4.12. ADC characteristics

Table 4-17. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	3.0	5.0	5.5	V
V_{IN}	ADC input voltage range	—	0	—	V_{DDA}	V
f_{ADC}	ADC clock	—	0.1	—	28	MHz
f_S	Sampling rate	12-bit	0.007	—	2	MSPS
		10-bit	0.008	—	2.3	
		8-bit	0.01	—	2.8	
		6-bit	0.013	—	3.5	
V_{IN}	Analog input voltage	16 external;3 internal	0	—	V_{DDA}	V
V_{REF+}	Positive Reference Voltage	—	—	V_{DDA}	—	V
V_{REF-}	Negative Reference Voltage	—	—	0	—	V
R_{AIN}	External input impedance	See ***Equation 1***	—	—	38	kΩ
R_{ADC}	Input sampling switch resistance	—	—	—	0.5	kΩ
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	—	5.2	—	pF
t_{CAL}	Calibration time	f_{ADC}=28MHz	—	3	—	μs
t_s	Sampling time	f_{ADC}=28MHz	0.053	—	9.554	μs
t_{CONV}	Total conversion time (including sampling time)	12-bit	—	14	—	1/ f_{ADC}
		10-bit	—	12	—	
		8-bit	—	10	—	
		6-bit	—	8	—	
t_{SU}	Startup time	—	—	—	1	μs

Equation 1: R_{AIN} max formula $$R_{AIN} < \frac{T_S}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N=12 (from 12-bit resolution).

Table 4-18. ADC R_{AIN} max for f_{ADC}=28MHz

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (KΩ)
1.5	0.0536	0.5
7.5	0.2679	4.8
13.5	0.4821	9
28.5	1.018	19
41.5	1.482	28
55.5	1.982	38
71.5	2.554	N/A

T_S (cycles)	t_S (us)	$R_{AIN\ max}$ (KΩ)
239.5	8.554	N/A

Note: Guaranteed by design, not tested in production.

4.13. DAC characteristics

Table 4-19. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.5	5.0	5.5	V
R_{LOAD}	Resistive load	Resistive load with buffer ON	5	—	—	kΩ
R_O	Impedance output	Impedance output with buffer OFF	—	—	15	kΩ
C_{LOAD}	Capacitive load	Capacitive load with buffer ON	—	—	50	pF
DAC_OUT_{min}	Lower DAC_OUT voltage	Lower DAC_OUT voltage with buffer ON	0.2	—	—	V
		Lower DAC_OUT voltage with buffer OFF	0.5	—	—	mV
DAC_OUT_{max}	Higher DAC_OUT voltage	Higher DAC_OUT voltage with buffer ON	—	—	V_{DDA}-0.2	V
		Higher DAC_OUT voltage with buffer OFF	—	—	V_{DDA}-1LSB	V
I_{DDA}	DC current consumption in quiescent mode with no load	Middle code on the input	—	—	797	μA
		Worst code on the input	—	—	1237	
DNL	Differential non linearity	—	—	±2	—	LSB
INL	Integral non linearity	—	—	±4	—	LSB
Gain error	Gain error	—	—	±0.5	—	%
$T_{SETTLING}$	Settling time	C_{LOAD}≤50pF, R_{LOAD}≥5kΩ	—	0.6	0.8	μs
Update rate	Max frequency for a correct DAC_OUT change from code i to i±1LSB	C_{LOAD}≤50pF, R_{LOAD}≥5kΩ	—	—	4	MS/s
T_{WAKEUP}	Wakeup time from off state	C_{LOAD}≤50pF, R_{LOAD}≥5kΩ	—	0.8	1	μs
PSRR	Power supply rejection ratio	No R_{Load}, C_{LOAD}=50pF	—	-85	-75	dB

4.14. SPI characteristics

Table 4-20. Standard SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	30	MHz
$TSI_{K(H)}$	SCK clock high time	—	19	—	—	ns
$TSI_{K(L)}$	SCK clock low time	—	19	—	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	25	ns
$t_{H(MO)}$	Data output hold time	—	2	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	5	—	—	ns
$t_{H(MI)}$	Data input hold time	—	5	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	f_{PCLK}=54MHz	74	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	f_{PCLK}=54MHz	37	—	—	ns
$t_{A(SO)}$	Data output access time	f_{PCLK}=54MHz	0	—	55	ns
$t_{DIS(SO)}$	Data output disable time	—	3	—	10	ns
$t_{V(SO)}$	Data output valid time	—	—	—	25	ns
$t_{H(SO)}$	Data output hold time	—	15	—	—	ns
$t_{SU(SI)}$	Data input setup time	—	5	—	—	ns
$t_{H(SI)}$	Data input hold time	—	4	—	—	ns

4.15. I2C characteristics

Table 4-21. I2C characteristics

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	—	0	100	0	400	KHz
$TSI_{L(H)}$	SCL clock high time	—	4.0	—	0.6	—	ns
$TSI_{L(L)}$	SCL clock low time	—	4.7	—	1.3	—	ns

4.16. USART characteristics

Table 4-22. USART characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	36	MHz
$TSI_{K(H)}$	SCK clock high time	—	13	—	—	ns
$TSI_{K(L)}$	SCK clock low time	—	13	—	—	ns

4.17. Operational amplifier characteristics

Table 4-23. OP-AMP characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.5	5.0	5.5	V
V_{CM}	Common mode voltage range	V_{DDA}=5.0	0.05	—	4.95	V
I_{DD}	Operating current	Normal mode	330	370	383	μA
		Low power mode	170	190	197	
I_{Load}	Drive current	Normal mode	0.2	22	33	mA
		Low power mode	0.6	24	34	
$V_{os\_cal\_range}$	V_{os} calibration range	—	—	—	±14	mV
V_{os_cal}	V_{os} after calibration	Normal/Low power mode	—	—	±1.2	mV
T_{wakeup}	Wakeup time	Normal mode	2.7	2.9	3.0	μS
		Low power mode	4.1	4.4	4.8	μS
SR	Slew rate	Normal, R_L=10kΩ, C_L=47pF	2	2.5	3.33	V/μS
		Low power mode	1.43	1.67	2	
CMRR	Common mode rejection ratio	Normal mode	—	93.9	—	dB
		Low power mode	—	90.4	—	
PSRR	Power supply rejection ratio	Normal mode	—	63.4	—	dB
		Low power mode	—	81.7	—	
GBW	Gain bandwidth	Normal, R_L=10kΩ, C_L=47pF	—	10.2	—	MHz
		Low power mode	—	5.0	—	
A0	Open-loop gain	Normal, 10kΩ<R_L<50kΩ	—	94.14	—	dB
		Low power mode	—	94	—	

4.18. Comparators characteristics

Table 4-24. CMP characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.5	5.0	5.5	V
V_{IN}	Input voltage range	—	0	—	V_{DDA}	V
V_{BG}	Scaler input voltage	—	—	1.2	—	V
V_{SC}	Scaler offset voltage	—	—	±5	±10	mV
t_D	Propagation delay for 200mv step with 100mV overdrive	Ultra low power mode	—	0.91	1.06	μS
		Low power mode	—	0.45	0.53	μS
		Medium power mode	—	0.16	0.20	μS
		High speed power mode	—	30	41	nS
	Propagation delay for full range step with 100mV overdrive	Ultra low power mode	—	1.47	1.64	μS
		Low power mode	—	0.77	0.87	μS
		Medium power mode	—	0.28	0.32	μS
		High speed power mode	—	42	54	nS
I_{DD}	Current consumption	Ultra low power mode	—	1.8	2.1	μA
		Low power mode	—	2.85	3.20	
		Medium power mode	—	7.40	7.99	
		High speed power mode	—	65.9	68.3	
V_{offset}	Offset error	—	—	±5	±10	mV
V_{hys}	No hysteresis	—	—	0	—	mV
	Low hysteresis	High speed power mode	7	8	11	
		All other power modes	5	8	14	
	Medium hysteresis	High speed power mode	13	16	21	
		All other power modes	11	16	30	
	High hysteresis	High speed power mode	26	32	43	
		All other power modes	20	32	60	

5. Package information

5.1. QFN package outline dimensions

Figure 5-1. QFN package outline

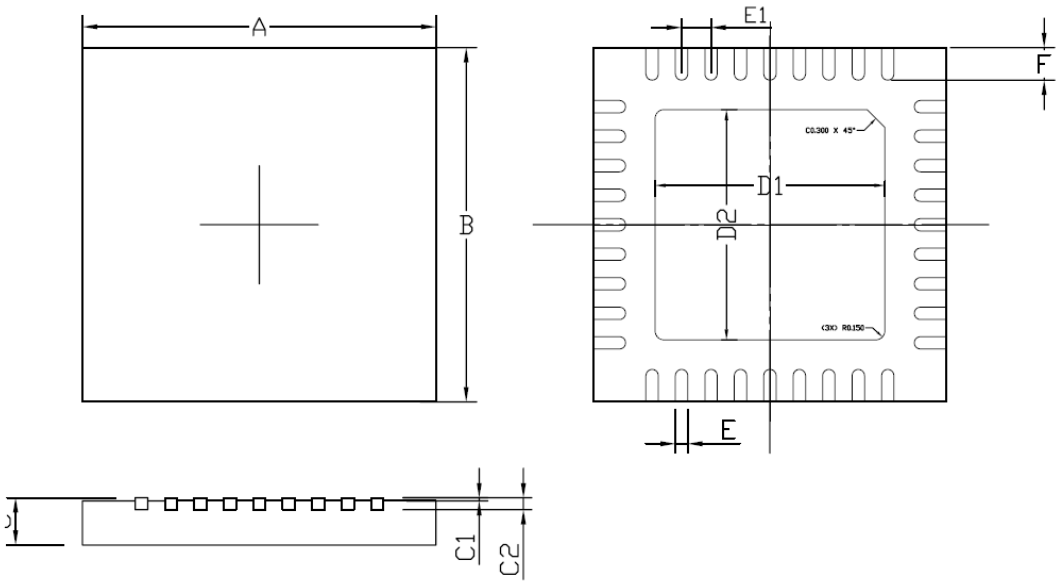


Table 5-1. QFN package dimensions

Symbol	QFN36		Symbol	QFN36	
	min	max		min	max
A	6.0 ± 0.1		D1	3.90 Typ	
B	6.0 ± 0.1		D2	3.90 Typ	
C	0.85	0.95	E	0.210 ± 0.025	
C1	0～0.050		E1	0.500 Typ	
C2	0.203 Typ		F	0.550 Typ	

(Original dimensions are in millmeters)

Note:

(1) Formed lead shall be planar with respect to one another within 0.004 inches.

(2) Both package length and width do not include mold flash and metal burr.

5.2. LQFP package outline dimensions

Figure 5-2. LQFP package outline

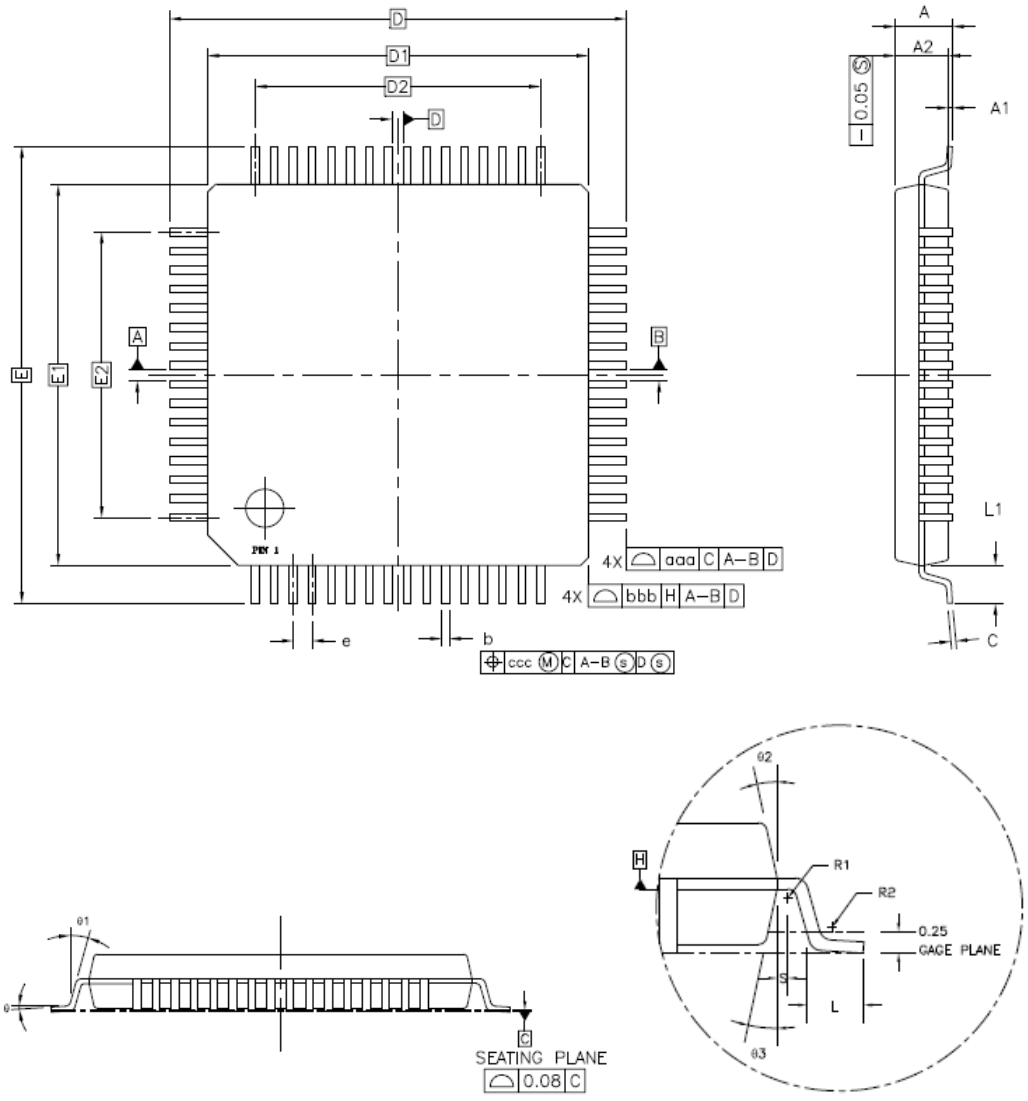


Table 5-2. LQFP package dimensions

Symbol	LQFP48			LQFP64		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.20	-	-	1.60
A1	0.05	-	0.15	0.05	-	0.15
A2	0.95	1.00	1.05	1.35	1.40	1.45
D	-	9.00	-	-	12.00	-
D1	-	7.00	-	-	10.00	-
E	-	9.00	-	-	12.00	-
E1	-	7.00	-	-	10.00	-
R1	0.08	-	-	0.08	-	-
R2	0.08	-	0.20	0.08	-	0.20
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	-	0.20	0.09	-	0.20
L	0.45	0.60	0.75	0.45	0.60	0.75
L1	-	1.00	-	-	1.00	-
S	0.20	-	-	0.20	-	-
b	0.17	0.22	0.27	0.17	0.20	0.27
e	-	0.50	-	-	0.50	-
D2	-	5.50	-	-	7.50	-
E2	-	5.50	-	-	7.50	-
aaa	0.20			0.20		
bbb	0.20			0.20		
ccc	0.08			0.08		

(Original dimensions are in millmeters)

6. Ordering information

Table 6-1. Part ordering code for GD32F190xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F190T4U6	16	QFN36	Green	Industrial -40°C to +85°C
GD32F190T6U6	32	QFN36	Green	Industrial -40°C to +85°C
GD32F190T8U6	64	QFN36	Green	Industrial -40°C to +85°C
GD32F190C4T6	16	LQFP48	Green	Industrial -40°C to +85°C
GD32F190C6T6	32	LQFP48	Green	Industrial -40°C to +85°C
GD32F190C8T6	64	LQFP48	Green	Industrial -40°C to +85°C
GD32F190R4T6	16	LQFP64	Green	Industrial -40°C to +85°C
GD32F190R6T6	32	LQFP64	Green	Industrial -40°C to +85°C
GD32F190R8T6	64	LQFP64	Green	Industrial -40°C to +85°C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jan.8, 2016
2.0	Adapt To New Name Convention	Jan 24, 2018