

## Mask Set Errata for Mask 1N36S

This report applies to mask 1N36S for these products:

- MKE1xZ256VLL7
- MKE1xZ256VLH7
- MKE1xZ128VLL7
- MKE1xZ128VLH7

**Table 1. Errata and Information Summary**

Erratum ID	Erratum Title
e9380	FlexIO: Reading FlexIO register when FlexIO functional clock is disabled results in a bus hang
e10364	LPI2C sends STOP condition if transmit FIFO is empty on completion of a master-receive transfer
e10527	LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters
e10355	PWT : Read/write reserved address (40056008~40056fff) won't result in hard fault interrupt
e10536	WDOG: After getting RCS assertion by polling, 4 LPO clock-time delay is the minimum requirement before the next block

**Table 2. Revision History**

Revision	Changes
0	Initial revision
1	The following errata were added. <ul style="list-style-type: none"><li>• e10355</li></ul>



**e9380: FlexIO: Reading FlexIO register when FlexIO functional clock is disabled results in a bus hang**

**Description:** Accessing a FlexIO register when the FlexIO functional clock is disabled (the clock source configured to 0 in PCC\_FLEXIO0[PCS], or the selected clock source is disabled) will hang the bus and the access will stall forever.

**Workaround:** Always enable the FlexIO functional clock before accessing any FlexIO register.

**e10364: LPI2C sends STOP condition if transmit FIFO is empty on completion of a master-receive transfer**

**Description:** If the transmit FIFO is empty at the end of a master receive transfer when AUTOSTOP=0, the LPI2C master will send a STOP condition before the next (repeated) START condition.

**Workaround:** Ignore

**e10527: LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters**

**Description:** When the LPUART transmitter is idle (LPUART\_STAT[TC]=1), two break characters may be sent when using LPUART\_CTRL[SBK] to send one break character. Even when LPUART\_CTRL[SBK] is set to 1 and cleared (set to 0) immediately.

**Workaround:** To queue a single break character via the transmit FIFO, set LPUART\_DATA[FRETSC]=1 with data bits LPUART\_DATA[T9:T0]=0.

**e10355: PWT : Read/write reserved address (40056008~40056fff) won't result in hard fault interrupt**

**Description:** PWT : Read/write reserved address (40056008~40056fff) won't result in hard fault interrupt

**Workaround:** Not writing to reserved address (40056008~40056fff).

**e10536: WDOG: After getting RCS assertion by polling, 4 LPO clock-time delay is the minimum requirement before the next block**

**Description:** WDOG cannot be unlocked if the unlock magic word are executed immediately after the RCS assert.

**Workaround:** After getting RCS assertion by polling, 4 LPO clock-time delay is the minimum requirement before next block.

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