Mask Set Errata for Mask 1N86K

This report applies to mask 1N86K for these products:

- KL03Z

Errata ID	Errata Title
8060	ROM: Bytes sent from host over I2C and SPI interfaces may be lost
8058	ROM: COP can't be re-enabled in application code due to being disabled by ROM boot code
8086	ROM: Fail to setup connection by UART interface if RX pin is low after POR
8059	ROM: Using UART at 57600 bits/s or greater with a core clock of 8 MHz may cause lost bytes
8068	RTC: Fail to enter low power mode if RTC time invalid flag (TIF) is not cleared after POR
8085	TPM: Writing the TPMx_MOD or TPMx_CnV registers more than once may fail when the timer is disabled

e8060: ROM: Bytes sent from host over I2C and SPI interfaces may be lost

Errata type: Errata
Description: Ping packet byte to the I2C and SPI loss occurs occasionally when the target is out of reset.

Workaround: 1. Run the I2C/SPI interface at 48 MHz core clock.

2. Insert a delay of at least 1 ms between the two bytes of the initial ping packet sent from the host to the device

3. If no response from the device is received, the host should re-send the ping packet

e8058: ROM: COP can't be re-enabled in application code due to being disabled by ROM boot code

Errata type: Errata
Description: COP is disabled by ROM boot code, and can't be re-enabled in application code. If the MCU boots up from ROM and then jumps into flash code, the flash code will fail to enable COP again.

Workaround: To use the COP watchdog in an application, write 00b to FOPT[BOOTSRC_SEL] bit to boot from flash out of reset.

e8086: ROM: Fail to setup connection by UART interface if RX pin is low after POR

Errata type: Errata
Description: If LPUART0_RX pin is low after POR, the ROM bootloader auto-baud althgorithm can't get the correct baud rate, and hence it fails to comunicate via LPUART interface.

Workaround: If user want to use ROM boot loader via LPUART interface, keep LPUART0_RX pin high before communication. One pull-up resistor is recommended.

e8059: ROM: Using UART at 57600 bits/s or greater with a core clock of 8 MHz may cause lost bytes

Errata type: Errata
Description: When using default 8 MHz as the core clock, it may cause lost bytes if LPUART bit rate is configured to 57600 bits/s or higher.

Workaround: Run the LPUART at a maximum baud rate of 38,400 or lower with default 8 MHz core clock. Or configure core clock higher than 8 MHz.

e8068: RTC: Fail to enter low power mode if RTC time invalid flag (TIF) is not cleared after POR

Errata type: Errata
Description: After POR, time invalid flag of RTC is set, RTC_SR[TIF]=1. If this flag is not cleared, the MCU fails to enter low power mode.

Workaround: Clear time invalid flag of RTC before entering low power mode. This bit is cleared by writing the RTC_TSR register when the time counter is disabled.

e8085: TPM: Writing the TPMx_MOD or TPMx_CnV registers more than once may fail when the timer is disabled

Errata type: Errata
Description: If writing the modulo register (TPMx_MOD) or channel value register (TPMx_CnV) more than once when the timer counter is disabled, and writes occur at a frequency faster than the TPM asynchronous clock, the registers may not update correctly.

This issue occurs when the register is written an even number of times but does not appear when the register is written an odd number of times.

If the TPM asynchronous clock is running at a higher frequency than the frequency of the writes, there are no issues writing these registers.

Workaround: When the TPMx_MOD or TPMx_CnV registers are written at a higher frequency than the TPM asynchronous clock there are two possible workarounds:

1) Do not write the TPMx_MOD or TPMx_CnV registers more than once before the timer counter is enabled.

2) If you need to update the TPMx_MOD or TPMx_CnV registers after they have been written once, before the timer counter is enabled, the new value must be written twice each time it is updated. This ensures that the registers are written an odd number of times.

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