

# LPC55S6x

Errata sheet LPC55S6x

Rev. 1.2 — July 22, 2019

Errata sheet

## Document information

Info	Content
<b>Keywords</b>	LPC55S69JBD100, LPC55S69JEV98, LPC55S66JBD100, LPC55S66JEV98,LPC55S66JBD64, LPC55S69JBD64
<b>Abstract</b>	LPC55S6x errata



**Revision history**

Rev	Date	Description
1.2	20190710	Added USB.1, USB.2, ADC.1, ADC.2, ADC.3, GPIO.1, I2S.1, AES.1, Powerquad.1, Powerquad.2
1.1	20190221	Updated device markings
1.0	20181204	Initial version

**Contact information**

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 1. Product identification

The LPC55S6x VFBGA98 package has the following top-side marking:

- First line: LPC55S6x
- Second line: JEV98
- Third line: xxxxxxxx
- Fourth line: zzzyywwxR
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 1B

The LPC55S6x HLQFP100 package has the following top-side marking:

- First line: LPC55S6x
- Second line: xxxxxxxx
- Third line: zzzyywwxR
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 0A or Device revision 1B

## 2. Errata overview

**Table 1. Functional problems table**

Functional problems	Short description	Revision identifier	Detailed description
ROM.1	For PRINCE encrypted region, partial erase cannot be performed.	0A	<a href="#">Section 3.1</a>
ROM.2	For PUF based key provisioning, a reset must be performed.	0A	<a href="#">Section 3.2</a>
ROM.3	Unprotected sub regions in PRINCE defined regions cannot be used.	0A	<a href="#">Section 3.3</a>
ROM.4	Last page of image is erased when simultaneously programming the signed image and CFPA region.	0A	<a href="#">Section 3.4</a>
VDD.1	The minimum operating voltage is 1.85 V.	0A	<a href="#">Section 3.5</a>
CMP.1	The hysteresis on the comparator cannot be enabled.	0A	<a href="#">Section 3.6</a>
USB.1	USB HS host fails when connecting to an LS device (mouse).	0A	<a href="#">Section 3.7</a>
USB.2	USB PHY does not auto-power down in suspend mode.	0A	<a href="#">Section 3.8</a>
ADC.1	Async interrupts with resume not supported.	0A, 1B	<a href="#">Section 3.9</a>
ADC.2	Request for offset calibration function bit (CALOFS) is not cleared after completion of offset calibration function.	0A	<a href="#">Section 3.10</a>
ADC.3	Sign-extend calibration results for averaging is not supported.	0A	<a href="#">Section 3.11</a>
GPIO.1	During power-up, an unexpected glitch (low pulse) can occur on port pins (PIO0_28, PIO1_1, PIO1_18, PIO1_30).	0A	<a href="#">Section 3.12</a>

**Table 1. Functional problems table ...continued**

Functional problems	Short description	Revision identifier	Detailed description
I2S.1	I2S signal sharing is not functional.	0A	<a href="#">Section 3.13</a>
AES.1	AES keys are not available when Cortex-M33 is running a security level less than 3.	0A	<a href="#">Section 3.14</a>
Powerquad.1	Format issue in matrix scale function.	0A	<a href="#">Section 3.15</a>
Powerquad.2	Floating Point to integer converter scaling issue.	0A	<a href="#">Section 3.16</a>

**Table 2. AC/DC deviations table**

AC/DC deviations	Short description	Product version(s)	Detailed description
n/a	n/a	n/a	n/a

**Table 3. Errata notes**

Errata notes	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

### 3. Functional problems detail

---

#### 3.1 ROM.1: For PRINCE encrypted region, partial erase cannot be performed

##### Introduction

The LPC55S6x devices supports real-time encryption and decryption for on-chip flash using the PRINCE encryption algorithm. The PRINCE module supports three flash memory regions for real-time encryption and decryption, referred to as crypto regions. Each crypto region resides at a 256 kB address boundary within the flash and are divided into 8 kB sub-regions which can be individually enabled.

##### Problem

For the LPC55S6x, when an erase operation is performed with a size less than 8 kB for a PRINCE encrypted region, a return error is returned and subsequent ISP commands do not respond.

##### Work-around

When a region is marked as a PRINCE encrypted region, a full erase of the PRINCE encrypted region must be performed.

This issue is fixed on device revision 1B.

#### 3.2 ROM.2: For PUF based key provisioning, a reset must be performed

##### Introduction

On the LPC55S6x, the Key Management module supports storing three 128-bit PRINCE Keys (KEY1, KEY2, and KEY3) used for the decryption process.

##### Problem

After PUF based key provisioning, the PRINCE module cannot perform the decryption process without performing a reset.

##### Work-around

Perform a reset via the external reset pin or power cycle the device for a successful decryption process when using a PUF key.

This issue is fixed on device revision 1B.

#### 3.3 ROM.3: Title recreate

##### Introduction

The LPC55S6x devices support real-time encryption and decryption for on-chip flash using the PRINCE encryption algorithm. The PRINCE module supports three flash memory regions for real-time encryption and decryption, referred to as crypto regions. Each crypto region resides at a 256 kB address boundary within the flash and is divided into 8 kB sub-regions which can be individually enabled.

**Problem**

Unprotected (non PRINCE encrypted) sub flash in PRINCE defined regions cannot be written after an erase operation. Any non PRINCE encrypted sub regions in the PRINCE defined regions cannot be used.

**Work-around**

There is no work-around.

This issue is fixed on device revision 1B.

**3.4 ROM.4: Last page of image is erased when simultaneously programming the signed image and CFPA region****Introduction**

On the LPC55S6x, the protected flash region (PFR) supports a Customer Field Programmable Area (CFPA) which can be used for Monotonic counters, Key revocation, and PRINCE IV codes. Also, the ROM supports secure boot using a signed image.

**Problem**

When simultaneously programming the signed image and the CFPA via the Secure Binary (SB2 file) image format, the last page of the image is erased.

**Work-around**

The signed image and the CFPA need to be programmed one a time to prevent the last page of the image from being erased.

This issue is fixed on device revision 1B.

**3.5 VDD.1: The minimum operating voltage is 1.85 V****Introduction**

The LPC55S6x operating voltage range specification is from 1.80 V to 3.6 V.

**Problem**

On the LPC55S6x rev 0A, the minimum operating range is 1.85 V.

**Work-around**

There is no work-around.

This issue is fixed on device revision 1B.

**3.6 CMP.1: The hysteresis on the comparator cannot be enabled****Introduction**

On the LPC55S6x, the analog comparator control register (COMP) provides an option to enable and disable the hysteresis.

**Problem**

On the LPC55S6x, the hysteresis feature of the comparator cannot be enabled.

**Work-around**

There is no work-around.

This issue will be fixed in the next silicon revision 1B.

**3.7 USB.1: HS host fails when connecting with the LS device (mouse)****Introduction**

The USB1 high-speed controller is available on select LPC55S6x devices and provides a plug-and-play connection of peripheral devices to a host with three different data speeds:

- high-speed with a data rate of 480Mbps.
- full-speed with a data rate of 12 Mbps.
- low-speed with a data rate of 1.5 Mbps.

Many portable devices can benefit from the ability to communicate with each other over the USB interface without intervention of a host PC.

**Problem**

USB HS host fails when connecting with an LS device (mouse).

**Work-around**

To support Full-Speed and Low-Speed applications, it is recommended to use the USB0 Full-Speed port and the USB1 High-speed port for Device or Host. In addition, should an application require support of Low-Speed USB devices with a USB High-Speed Host, this can be accomplished by inserting a USB Hub between the USB1 High-speed port and external USB devices.

This issue is fixed on device revision 1B.

**3.8 USB.2: PHY does not auto-power down in suspend mode****Introduction**

The USB1 High-Speed Physical Layer (PHY) is available on LPC55S6x devices that include USB high-speed controllers.

A device will go into the L2 suspend state if there is no activity on the USB bus for more than three ms.

The USB protocol requires power management by the USB device.

**Problem**

The device does not auto-power down properly in suspend states, which impacts power consumption in the PHY.

**Work-around**

This issue is fixed on device revision 1B.

### 3.9 ADC.1: Async interrupts with resume not supported

#### Introduction

The ADC controller is available on all LPC55S6x devices. Trigger detect with up to 16 trigger sources is supported with priority level configuration. A software or hardware trigger option is provided for each.

#### Problem

The following problems are all related to the restart after interrupt feature:

- Low priority trigger executes twice when resumed.
- Trigger can't restart when it is configured to do so.
- Incorrect trigger resumed after exception.

#### Work-around

There is no work-around.

The async interrupts with resume is not supported on device revisions 0A and 1B.

### 3.10 ADC.2: Request for offset calibration function bit (CALOFS) is not cleared after completion of offset calibration function

#### Introduction

The ADC controller is available on all LPC55S6x devices and supports a calibration step where the ADC is configured to perform a calibration operation to determine the value needed in the OFSTRIM register. The CALOFS bit is set to determine the value for the OFSTRIM register which automatically begins a sequence that calculates the value. Once the sequence has completed, the OFSTRIM register is updated with a signed value between -16 and 15. This value is used to minimize offset during normal operation

#### Problem

The CALOFS bit is written a 1 by software with a bus access to initiate the calibration offset function implemented in hardware. The CALOFS control bit is supposed to be cleared by hardware upon completion of the offset calibration function, but the clock used for the CALOFS bit is only active when the ADC registers are being accessed by software and the hardware clearing mechanism does not work except when an ADC bus access is in progress on the exact cycle that hardware is trying to clear the CALOFS bit. In the failing case where CALOFS does not clear after the offset calibration function, the ADC logic begins the calibration offset function again. This results in an indefinite loop that can only be terminated by a system reset or some form of polling of the ADC registers that coincides with the successful clearance of the CALOFS bit.

#### Work-around

To clear the OFSTRIM-request, read the register STATUS (poll for the CAL\_RDY bit in the STATUS register). The polling for the bit is enough to ensure that the request is cleared.

This issue is fixed on device revision 1B.



### 3.11 ADC.3: Sign-extend calibration results for averaging is not supported

#### Introduction

The ADC controller is available on all LPC55S6x devices.

The ADC module includes offset and linearity calibration logic. A request for calibration should be made any time upon reset or power up. Each SAR conversion will utilize calibration data calculated during the auto-calibration routine.

#### Problem

Sign-extend calibration values for averaging is not supported (averaging of negative numbers in the offset calibration).

#### Work-around

Software-based averaging can be used as a work-around.

This issue is fixed on device revision 1B.

### 3.12 GPIO.1: During power-up, an unexpected glitch (low pulse) could occur on port pins (PIO0\_28, PIO1\_1, PIO1\_18, PIO1\_30).

#### Introduction

To wake up from reduced power modes, the wake-up source must be properly configured. Each reduced power mode supports its own wake-up sources and needs to be configured accordingly.

#### Problem

An unexpected glitch (low pulse for around 200 us) could occur on port pins (PIO0\_28, PIO1\_1, PIO1\_18, PIO1\_30) as the VDD supply ramps up. This glitch does not occur when device wakes up from sleep, deep-sleep, power-down, and deep power-down modes.

#### Work-around

There is no work-around.

This issue is fixed in the silicon revision 1B.

### 3.13 I2S.1: I2S signal sharing is not functional

#### Introduction

Signal sharing allows more than one on-chip I2S interface to be connected to a clock, WS, and input data on the same pins without the need for any external board wiring. I2S signal sharing allows the use of multiple I2S that function together in a single TDM stream thus reducing the number of pins that are required for a particular application.

#### Problem

The I2S signal sharing feature is not functional.

### Work-around

There is no work-around.

This issue is fixed in device revision 1B.

## 3.14 AES.1: Keys are not available when Cortex-M33 is running a security level less than 3

### Introduction

The security system on LPC55S6x has a set of hardware blocks and ROM code to implement the security features provided by the device. The hardware consists of an AES, SHA, and PRINCE engine, a random number generator, and a key storage block that can wrap user provided keys and derive device unique keys from an SRAM based PUF (Physically Unclonable Function). The wrapped keys and derived keys are exported by PUF to firmware in key codes (encrypted data) through the SET\_KEY and GEN\_KEY commands.

During key code generation, the KEY\_INDEX parameter can be specified, which determines the output path of the unwrapped plain key values. Keys wrapped with KEY\_INDEX set to 0 are only provided to hardware engines (AES & PRINCE) through a secret bus; these keys are also referred to as secret keys. All other keys with KEY\_INDEX set from 1 to 15 are provided through the registers interface. Also, when you choose not to use the TrustZone mechanism, you cannot use the secret keys (KEY\_INDEX = 0) with the AES engine. Instead, you have to use the software supplied key.

### Problem

Hardware logic makes all secret keys passed from PUF to the AES engine unusable unless firmware running on the Cortex-M33 accesses the HashCrypt engine at secure-privilege level 3. Thus, firmware should be written to make sure the Cortex-M33 uses the appropriate secure-privilege mode before configuring the AES engine to use secret keys. In addition, the TrustZone mechanism must be enabled to use secret keys (KEY\_INDEX = 0) with the AES engine.

### Work-around

To use secret keys with the AES engine, firmware should make sure that the Cortex-M33 is at secure-privilege level 3 before configuring the AES engine registers. User applications which disable the TrustZone mechanism cannot use secret keys.

There is no workaround.

This issue is fixed in device revision 1B.

## 3.15 Powerquad.1: Format issue in matrix scale function

### Introduction

A PowerQuad DSP Coprocessor and Accelerator are available on all LPC55S6x devices. A matrix operation (Add, Sub, Dot, Prod, Mult, Inverse, Transpose, and Scale) is provided for the DSP.

**Problem**

When using the matrix scale operation, in floating number to fixed one conversion, every 8th number is wrong.

**Work-around**

Do not mix fixed and float operands. As long as all operands and results are either fixed or float, then there is no issue.

This issue is fixed in device revision 1B.

**3.16 Powerquad.2: Floating point to integer converter scaling issue****Introduction**

A PowerQuad DSP Coprocessor and Accelerator is available on all LPC55S6x devices. For each co-processor output, and for AHB data converter for streaming operations write back, a floating point to fixed point conversion can be performed, while allowing the user to adjust the floating point's numbers exponent value before the conversion. As a result, a scaling by  $2^N$  of the floating-point value can occur when it gets converted. In the case of co-processor opcodes, this feature is useful in order to 'upscale' by taking numbers which have a fractional component and multiplying them by a power of two to increase the resolution in the resulting integer. In the case of AHB data writeback, it is possible to 'upscale' or 'downscale' the floating-point number.

**Problem**

When performing a downscale, the result for a floating-point value of 0 is an overflow of the exponent field, resulting in saturation. This is not the appropriate behavior since a 0, whether down-scaled or up-scaled, should result in 0.

When performing an upscale, results are correct, except in the case where a very large number's exponent combined with the up-scaling exceeds  $2^{127}$ . In this case, the overflow detection may not work, and saturation may not be correctly engaged due to the overflow in the exponent field. A negative prescaler ( $2^x$  prescaler where x is negative) cannot be used.

**Work-around**

Use floating numbers if fractional numbers are needed.

This issue is fixed in device revision 1B.

#### **4. AC/DC deviations detail**

---

No known errata.

#### **5. Errata notes detail**

---

No known errata.

## 6. Legal information

### 6.1 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

### 6.2 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

### 6.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 7. Contents

<b>1</b>	<b>Product identification</b>	<b>3</b>		
<b>2</b>	<b>Errata overview</b>	<b>3</b>		
<b>3</b>	<b>Functional problems detail</b>	<b>5</b>		
3.1	ROM.1: For PRINCE encrypted region, partial erase cannot be performed.	5	3.10	ADC.2: Clearing of CALOFS
	Introduction	5		Introduction
	Problem	5		Problem
	Work-around	5		Work-around
3.2	ROM.2: For PUF based key provisioning, a reset must be performed	5	3.11	ADC.3: Sign-extend calibration results for averaging
	Introduction	5		Introduction
	Problem	5		Problem
	Work-around	5		Work-around
3.3	ROM.3: Title recreate	5	3.12	GPIO.1: During power-up, an unexpected glitch (low pulse) could occur on port pins (PIO0_28, PIO1_1, PIO1_18, PIO1_30).
	Introduction	5		Introduction
	Problem	6		Problem
	Work-around	6		Work-around
3.4	ROM.4: Last page of image is erased when simultaneously programming the signed image and CFPA region	6	3.13	I2S.1: I2S signal sharing is not functional
	Introduction	6		Introduction
	Problem	6		Problem
	Work-around	6		Work-around
3.5	VDD.1: The minimum operating voltage is 1.85 V	6	3.14	AES.1: Keys are not available when Cortex-M33 is running a security level less than 3
	Introduction	6		Introduction
	Problem	6		Problem
	Work-around	6		Work-around
3.6	CMP.1: The hysteresis on the comparator cannot be enabled	6	3.15	Powerquad.1: Format issue in matrix scale function
	Introduction	6		Introduction
	Problem	6		Problem
	Work-around	7		Work-around
3.7	USB.1: HS host fails when connecting with the LS device (mouse)	7	3.16	Powerquad.2: Floating point to integer converter scaling issue
	Introduction	7		Introduction
	Problem	7		Problem
	Work-around	7		Work-around
3.8	US.2: PHY does not auto-power down in suspend mode	7		
	Introduction	7		
	Problem	7		
	Work-around	7		
3.9	ADC.1: Async interrupts with resume not supported	8	<b>4</b>	<b>AC/DC deviations detail</b>
	Introduction	8	<b>5</b>	<b>Errata notes detail</b>
	Problem	8	<b>6</b>	<b>Legal information</b>
	Work-around	8	6.1	Definitions
			6.2	Disclaimers
			6.3	Trademarks
			<b>7</b>	<b>Contents</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.