ES_LPC81xM

Errata sheet LPC81xM

Rev. 3.2 — 3 April 2018 **Errata sheet**

Document information

Info	Content
Keywords	LPC810M021FN8; LPC811M001JDH16; LPC812M101JDH16; LPC812M101JD20; LPC812M101JDH20, LPC812M101JTB16, LPC81xM errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
3.2	20180403	• Added VDD.1
3.1	20140401	• Added details on how to determine revision identifier for TSSOP16.
3	20130827	• Added CMP.1.
2	20130530	• Added revision 4C. • Updated SYSOSC.1. • Added CMP.1.
1	20130307	• Initial version

Contact information

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1. Product identification

The LPC81xM devices typically have the following top-side marking:

LPC81x

xxxxx

xxxxxxxx

xxYWWxR[x]

The last two letters in the last line (field ‘xR’) identify the boot code version and device revision.

Table 1. Device revision table

Revision identifier (xR)	Revision description
‘1A’	Initial device revision with boot code version 13.1
‘2A’	Second device revision with boot code version 13.2
‘4C’	Third device revision with boot code version 13.4

Field ‘Y’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

Remark: On the TSSOP16 package, the last line includes only the date code xxYWW. In order to determine the revision identifier, use the ISP command Read Boot code version (for more details, refer to Chapter 21 of the LPC81x user manual (UM10601)).

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
CMP.1	On the LPC810M021FN8 revision A device, the comparator is not functional.	‘1A’, ‘2A’	Section 3.1
DPD.1	In Deep Power-down mode, the current consumption can be higher than anticipated	‘1A’, ‘2A’	Section 3.2
FLASHCFG.1	The flash access time must be set to 2 system clocks before performing In-System/In-Application programming calls, and power profile API calls.	‘1A’, ‘2A’	Section 3.3
I2C.1	In I2C slave mode, the SLVPENDING bit does not clear when the slave function is disabled.	‘1A’, ‘2A’	Section 3.4
PD.1	Reset wake-up sources cannot be used to wake up the device from power-down mode.	‘1A’, ‘2A’	Section 3.5
SYSOSC.1	When using an external crystal oscillator, the V_{DD} supply voltage must be 1.9 V or above for device revision 4C, and 2.3 V or above for device revisions 1A and 2A.	‘1A’, ‘2A’, ‘4C’	Section 3.6
VDD.1	The minimum wait time of the power supply ramp must be minimum 2 ms.	‘1A’, ‘2A’, ‘4C’	Section 3.7

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Detailed description
n/a	n/a	n/a

Table 4. Errata notes

Note	Short description	Detailed description
n/a	n/a	n/a

3. Functional problems detail

3.1 CMP.1

Introduction:

The LPC810M021FN8 part features a comparator which can be used to compare voltage levels on external pins and internal voltages.

Problem:

On the LPC810M021FN8 revision A only, the comparator is not functional.

Work-around:

None. This errata is fixed on the LPC810M021FN8 revision C.

3.2 DPD.1

Introduction:

The LPC800 supports four low-power modes: sleep, deep-sleep, power-down, and deep power-down modes. The LPC800 datasheet specifies 220 nA typical deep power-down current (wake-up timer disabled) at 25 °C, and 1 µA typical deep power-down current (wake-up timer enabled) at 25 °C.

Problem:

The deep power-down current can be approximately 30 µA higher than the specified typical values in the datasheet.

Work-around:

None.

3.3 FLASHCFG.1

Introduction:

On the LPC800, access to the flash memory can be configured with various access times by writing to the FLASHCFG register. The user can write a value of 0x0 (1 system clock flash access time) or a value of 0x1 (2 system clocks flash access time) in the FLASHCFG register. The default value is set to 0x1. The LPC800's ROM supports flash In-System Programming (ISP)/In-Application Programming (IAP) calls, and power profile API calls.

Problem:

If the user application is using 1 system clock flash access time (FLASHCFG register set to 0x0), the In-System/In-Application Programming calls and power profile API calls will not always operate correctly with this setting.

Work-around:

Before performing the In-System/In-Application programming calls, and/or power profile API calls, the user must ensure that the FLASHCFG register is set to 2 system clocks flash access time. The user can use 1 system clock flash access time when these API calls are not performed.

3.4 I2C.1

Introduction:

The I2C peripheral on the LPC800 supports independent Master, Slave, and Monitor functions. In the I2C slave mode, the slave function internally resets when the slave function is disabled. This is controlled using the SLVEN bit in the I2C Configuration register (CFG).

The SLVPENDING bit in the I2C status register (STAT) indicates whether the slave function is waiting to continue communication and needs software service. If the SLVPENDING bit is read as '0', the slave function does not need service, and if read as '1', the slave function needs service and an interrupt can be generated.

The SLVPENDING bit in the I2C status register (STAT) automatically clears when a '1' is written to the SLVCONTINUE bit in the Slave Control register (SLVCTL) or when the slave function is disabled via the SLVEN bit in the I2C Configuration register (CFG).

Problem:

When the slave function is disabled, the SLVPENDING bit in the I2C status register (STAT) does not clear, and as a result, an interrupt will be generated when the I2C slave function is re-enabled.

Work-around:

After disabling the slave function, the SLVPENDING bit in the I2C status register (STAT) should be cleared by writing a '1' to the SLVCONTINUE bit in the Slave Control register (SLVCTL).

3.5 PD.1

Introduction:

The LPC800 supports four low-power modes: sleep, deep-sleep, power-down, and deep power-down modes. In power-down mode, the LPC800 can wake up from the following wake-up sources:

1. Interrupts from USARTs, SPI, I2C
2. Pin interrupts
3. Brown-Out Detect (BOD) interrupt and reset
4. Windowed Watchdog Timer (WWDT) interrupt and reset
5. External Reset Pin
6. Self Wake-Up Timer (WKT)

Problem:

The BOD reset, WWDT reset, and the external reset pin wake-up sources cannot be used to wake up the device from power-down mode.

Work-around:

Use the other wake-sources (mentioned above) to wake up the device from power-down mode.

3.6 SYSOSC.1

Introduction:

On the LPC800, the V_{DD} supply voltage range is from 1.8 V to 3.6 V. The LPC800 has various clock sources such as the internal oscillator (IRC), system oscillator, CLKIN, and watchdog oscillator.

An external crystal oscillator can be connected between the XTALIN and XTALOUT pins to use the system oscillator as a clock source. The system oscillator can also be bypassed by setting the BYPASS bit in the SYSOSCCTRL register, and an external clock source can be fed directly to the XTALIN pin.

Problem:

An external crystal oscillator connected to the system oscillator does not function when the V_{DD} power supply is below 1.9 V for device revision 4C, and below 2.3 V for device revisions 1A and 2A.

Work-around:

The V_{DD} supply voltage must be 1.9 V or above for device revision 4C, and 2.3 V or above for device revisions 1A and 2A when connecting an external crystal oscillator to the system oscillator. If the V_{DD} supply voltage is below 1.9 V for device revision 4C, and below 2.3 V for device revisions 1A and 2A, an external clock source can be fed to the XTALIN by bypassing the system oscillator or the other clock sources mentioned above can be used.

3.7 VDD.1

Introduction:

On the LPC81x, the V_{DD} supply voltage range is from 1.8 V to 3.6 V. The LPC81x datasheet specifies a power-up ramp condition for the user application. Before ramping up, the minimum wait time (t_{wait}) of the power supply on the V_{DD} pin (200 mV or below) is 12 μs.

Problem:

The device might not always start-up if the minimum wait time (t_{wait}) is 12 μs. The required minimum time (t_{wait}) specification is 2 ms.

Work-around:

None.

4. AC/DC deviations detail

n/a

5. Errata notes

5.1 Note.1

n/a

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