

MC14008B

4-Bit Full Adder

The MC14008B 4-bit full adder is constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high-speed operation when used with other adders in a system.

Features

- Look-Ahead Carry Output
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4008B
- This Device is Pb-Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	-55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating: "D/DW" Package: -7.0 mW/°C From 65°C To 125°C

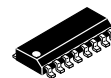
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



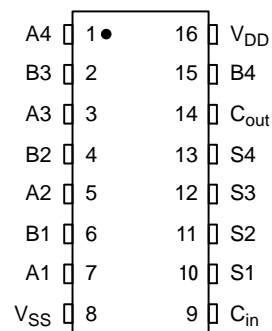
ON Semiconductor®

<http://onsemi.com>

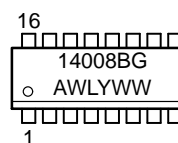


SOIC-16
D SUFFIX
CASE 751B

PIN ASSIGNMENT



MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Indicator

ORDERING INFORMATION

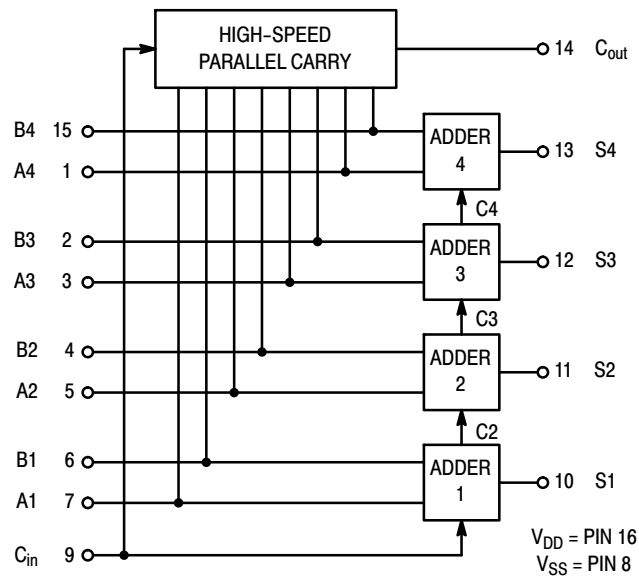
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC14008B

TRUTH TABLE (One Stage)

C _{in}	B	A	C _{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping [†]
MC14008BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC14008B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	-	0.05	-	0	0.05	-	0.05	Vdc	
		10	-	0.05	-	0	0.05	-	0.05		
15		-	0.05	-	0	0.05	-	0.05			
V _{in} = 0 or V _{DD}	"1" Level V _{OH}	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc	
		10	9.95	-	9.95	10	-	9.95	-		
		15	14.95	-	14.95	15	-	14.95	-		
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level V _{IL}	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc	
		10	-	3.0	-	4.50	3.0	-	3.0		
		15	-	4.0	-	6.75	4.0	-	4.0		
	(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"1" Level V _{IH}	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
			10	7.0	-	7.0	5.50	-	7.0	-	
			15	11	-	11	8.25	-	11	-	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc	
		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-		
		10	-1.6	-	-1.3	-2.25	-	-0.9	-		
		15	-4.2	-	-3.4	-8.8	-	-2.4	-		
	(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
			10	1.6	-	1.3	2.25	-	0.9	-	
15			4.2	-	3.4	8.8	-	2.4	-		
Input Current	I _{in}	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	-	5.0	-	0.005	5.0	-	150	μAdc	
		10	-	10	-	0.010	10	-	300		
		15	-	20	-	0.015	20	-	600		
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.7 μA/kHz) f + I _{DD} I _T = (3.4 μA/kHz) f + I _{DD} I _T = (5.0 μA/kHz) f + I _{DD}							μAdc	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

MC14008B

SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time Sum in to Sum Out t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 127 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$ Sum In to Carry Out t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 220 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 112 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 85 \text{ ns}$ Carry In to Sum Out t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 290 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 122 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$ Carry In to Carry Out t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 85 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 30 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	– – –	400 160 115 305 145 110 375 155 115 170 75 55	800 320 230 610 290 220 750 310 230 340 150 110	ns

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

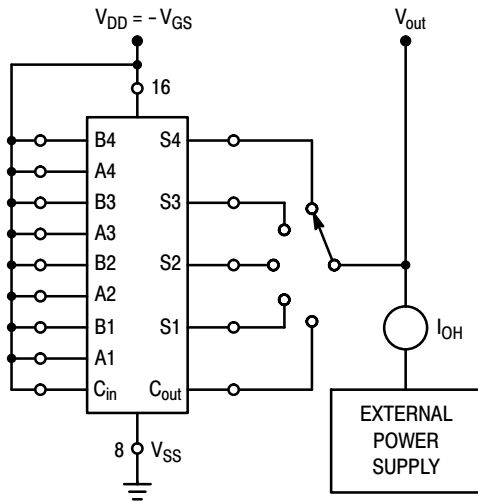


Figure 1. Typical Source Current Characteristics Test Circuit

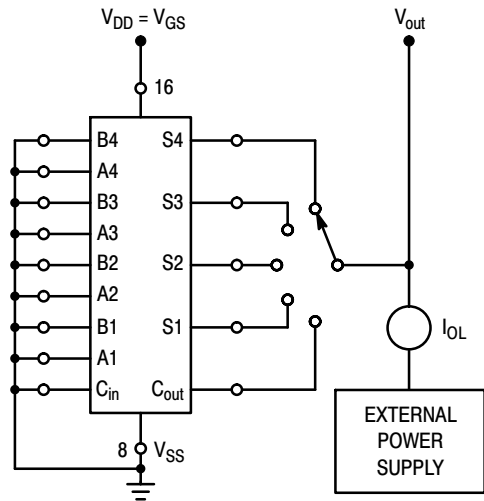


Figure 2. Typical Sink Current Characteristics Test Circuit

MC14008B

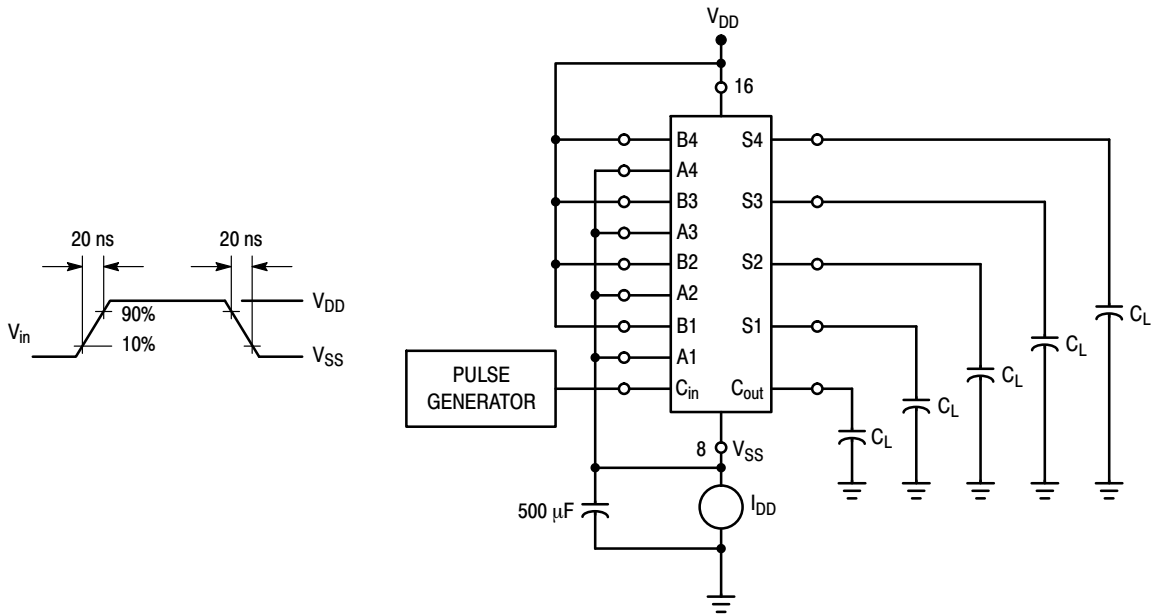


Figure 3. Dynamic Power Dissipation Test Circuit and Waveform

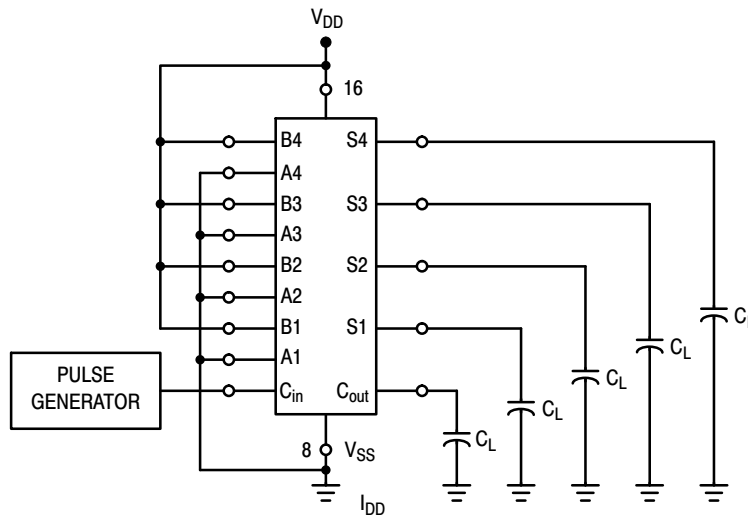


Figure 4. Switching Time Test Circuit and Waveforms

MC14008B

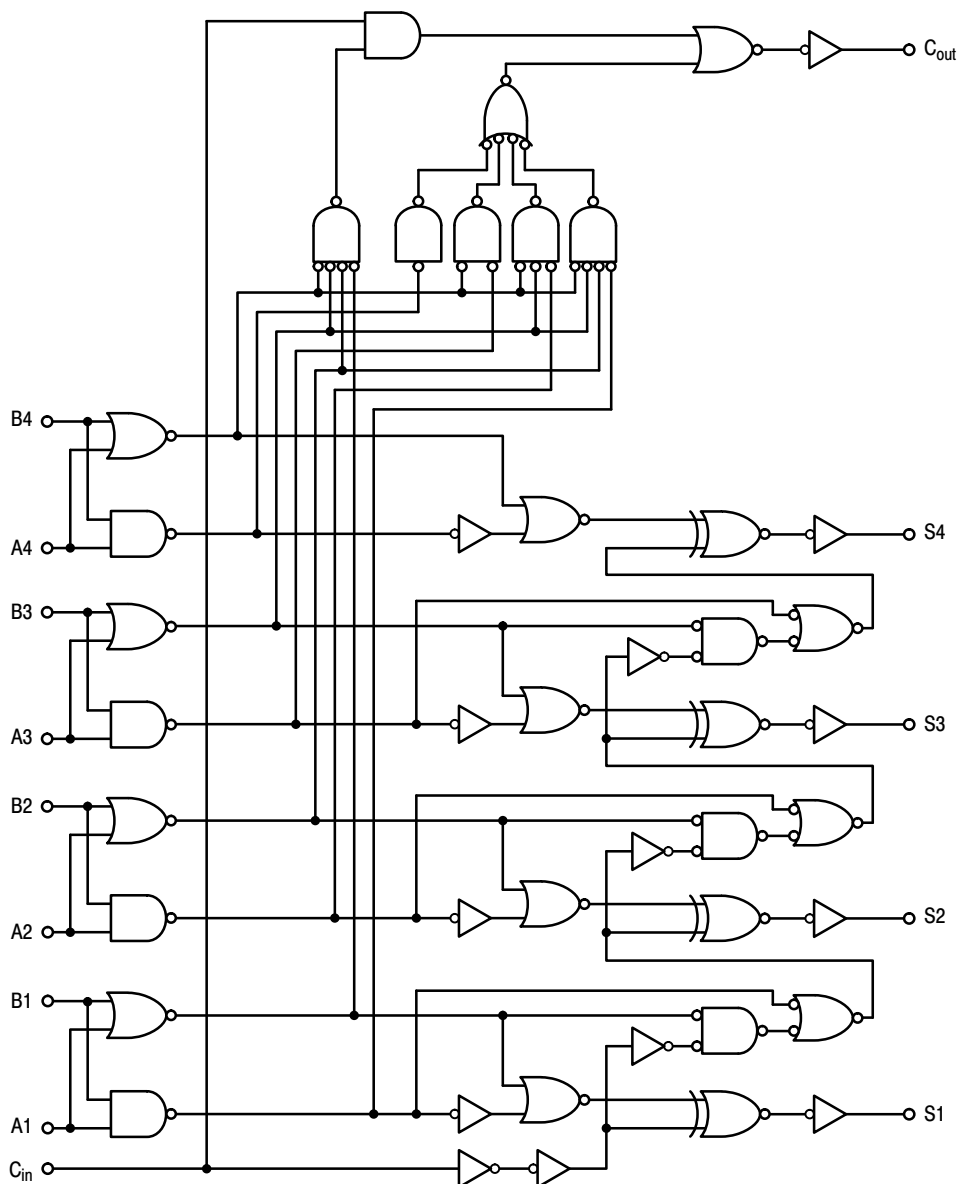
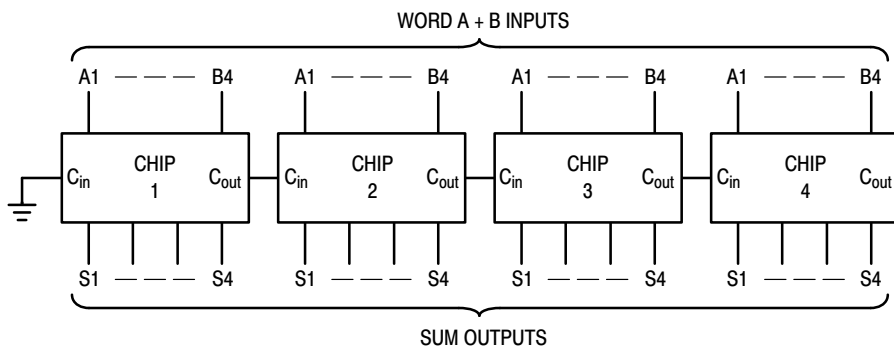


Figure 5. Logic Diagram

TYPICAL APPLICATION



Calculation of 16-bit adder speed:

$$t_p \text{ total} = t_p (\text{Sum to Carry}) + t_p (\text{Carry to Sum}) + 2 t_p (\text{Carry to Carry})$$

The guaranteed 16-bit adder speed at 10 V, 25°C, $C_L = 50 \text{ pF}$ is:

$$t_p \text{ total} = 290 + 310 + 300 = 900 \text{ ns}$$

Figure 6. Using the MC14008B in a 16-Bit Adder Configuration

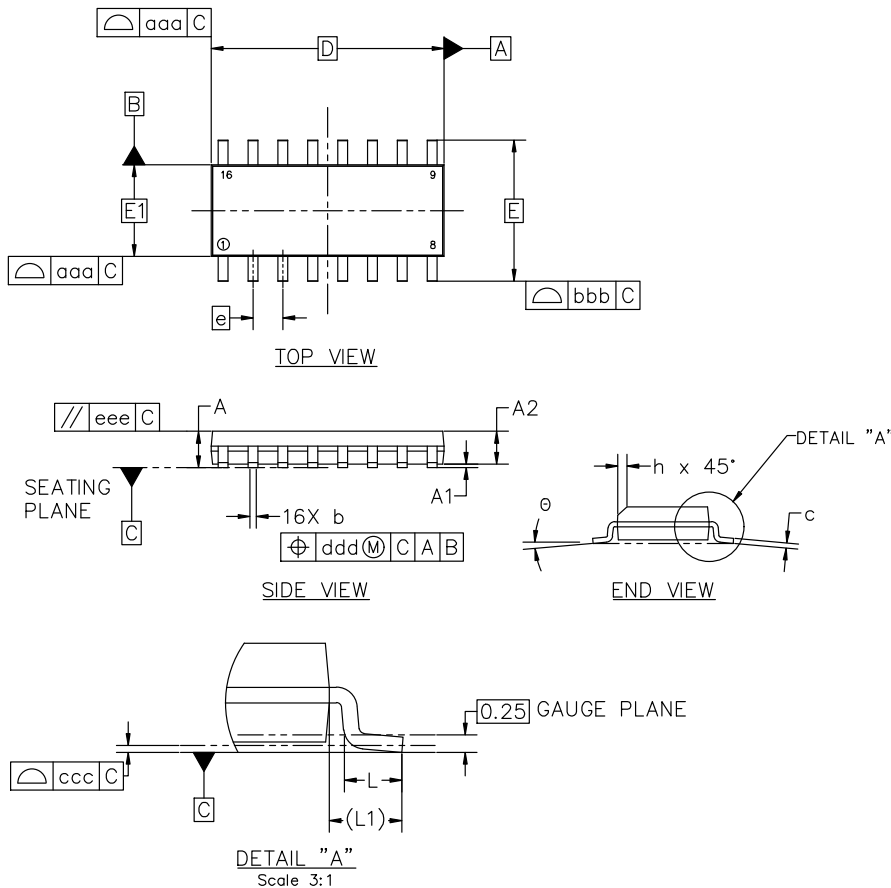


SOIC-16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

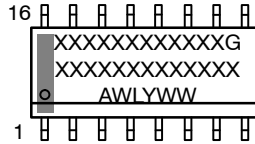
DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-16 9.90X3.90X1.50 1.27P	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

<p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p>	<p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p>	<p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p>	<p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p>
<p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p>	<p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p>	<p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p>	

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-16 9.90X3.90X1.50 1.27P	PAGE 2 OF 2

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales