12-Bit Binary Counter

MC14040B

The MC14040B 12−stage binary counter is constructed with MOS P−Channel and N−Channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple−carry binary counter. The device advances the count on the negative−going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency−driving circuits.

Features

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Common Reset Line
- Pin−for−Pin Replacement for CD4040B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

SOIC−16
D SUFFIX
CASE 751B

TSSOP−16
DT SUFFIX
CASE 948F

PIN ASSIGNMENT

Q12	1 ●	16	V_{DD}
Q6	2	15	Q11
Q5	3	14	Q10
Q7	4	13	Q8
Q4	5	12	Q9
Q3	6	11	R
Q2	7	10	C
V_{SS}	8	9	Q1

MARKING DIAGRAMS

16
14040BG
AWLYWW
1
SOIC−16
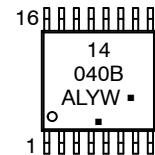
16
14
040B
ALYW ▪
1
TSSOP−16

A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Temperature Derating: "D/DW" Packages: −7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

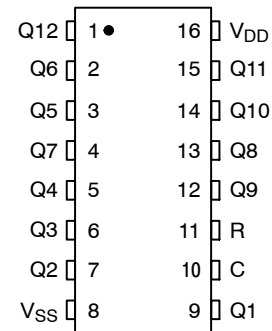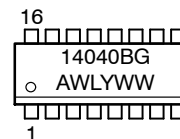## ORDERING INFORMATION

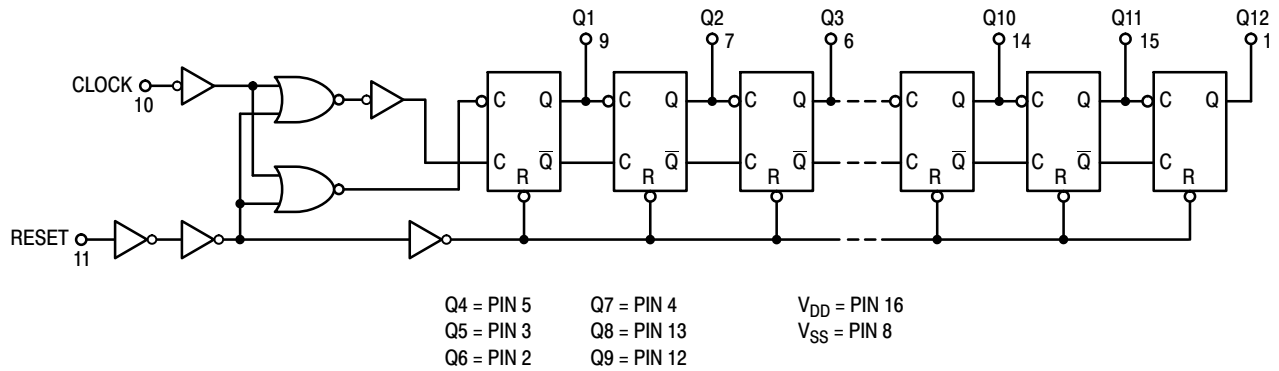See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC14040B

TRUTH TABLE

Clock	Reset	Output State
⌐	0	No Change
⌐	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM

Q4 = PIN 5   Q7 = PIN 4 V_{DD} = PIN 16
Q5 = PIN 3   Q8 = PIN 13 V_{SS} = PIN 8
Q6 = PIN 2   Q9 = PIN 12

ORDERING INFORMATION

Device	Package	Shipping[†]
MC14040BDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14040BDR2G	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
NLV14040BDR2G*	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
MC14040BDTR2G	TSSOP−16 (Pb−Free)	2500 Units / Tape & Reel
NLV14040BDTR2G*	TSSOP−16 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MC14040B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V$_{SS}$)

Characteristic	Symbol	V$_{DD}$ Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V$_{in}$ = V$_{DD}$ or 0	V$_{OL}$	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V$_{in}$ = 0 or V$_{DD}$	V$_{OH}$	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level (V$_O$ = 4.5 or 0.5 Vdc) (V$_O$ = 9.0 or 1.0 Vdc) (V$_O$ = 13.5 or 1.5 Vdc)	V$_{IL}$	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level (V$_O$ = 0.5 or 4.5 Vdc) (V$_O$ = 1.0 or 9.0 Vdc) (V$_O$ = 1.5 or 13.5 Vdc)	V$_{IH}$	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11	–	11	8.25	–	11	–	
Output Drive Current (V$_{OH}$ = 2.5 Vdc) Source (V$_{OH}$ = 4.6 Vdc) (V$_{OH}$ = 9.5 Vdc) (V$_{OH}$ = 13.5 Vdc)	I$_{OH}$	5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	mAdc
		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V$_{OL}$ = 0.4 Vdc) Sink (V$_{OL}$ = 0.5 Vdc) (V$_{OL}$ = 1.5 Vdc)	I$_{OL}$	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	
		15	4.2	–	3.4	8.8	–	2.4	–	
Input Current	I$_{in}$	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V$_{in}$ = 0)	C$_{in}$	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I$_{DD}$	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C$_L$ = 50 pF on all outputs, all buffers switching)	I$_T$	5.0	— I$_T$ = (0.42 μA/kHz) f + I$_{DD}$							μAdc
		10	I$_T$ = (0.85 μA/kHz) f + I$_{DD}$							
		15	I$_T$ = (1.43 μA/kHz) f + I$_{DD}$							

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I$_T$ is in μA (per package), C$_L$ in pF, V = (V$_{DD}$ − V$_{SS}$) in volts, f in kHz is input frequency, and k = 0.001.

MC14040B

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time T_{TLH}, T_{THL} = (1.5 ns/pF) C_L + 25 ns T_{TLH}, T_{THL} = (0.75 ns/pF) C_L + 12.5 ns T_{TLH}, T_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	 5.0 10 15	 – – –	 100 50 40	 200 100 80	ns
Propagation Delay Time Clock to Q1 t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 95 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 – – –	 260 115 80	 520 230 160	ns
Clock to Q12 t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 2415 ns t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 867 ns t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 475 ns		 5.0 10 15	 – – –	 1625 720 500	 3250 1440 1000	ns
Propagation Delay Time Reset to Q_n t_{PHL} = (1.7 ns/pF) C_L + 485 ns t_{PHL} = (0.86 ns/pF) C_L + 182 ns t_{PHL} = (0.5 ns/pF) C_L + 145 ns	t_{PHL}	 5.0 10 15	 – – –	 370 155 115	 740 310 230	ns
Clock Pulse Width	t_{WH}	5.0 10 15	385 150 115	140 55 38	– – –	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	– – –	2.1 7.0 10.0	1.5 3.5 4.5	MHz
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15		No Limit		ns
Reset Pulse Width	t_{WH}	5.0 10 15	960 360 270	320 120 80	– – –	ns
Reset Removal Time	t_{rem}	5.0 10 15	130 50 30	65 25 15	– – –	ns

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
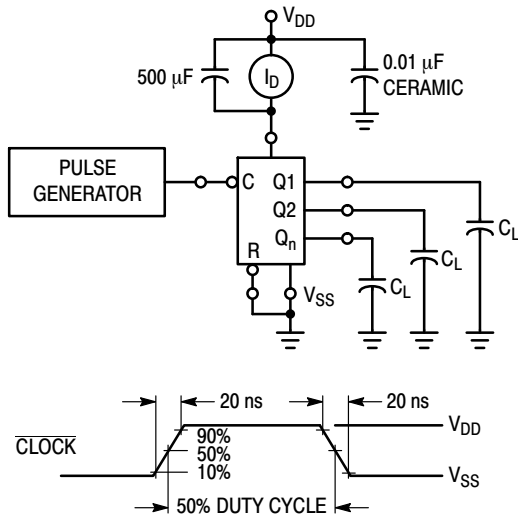
Figure 1. Power Dissipation Test Circuit and Waveform
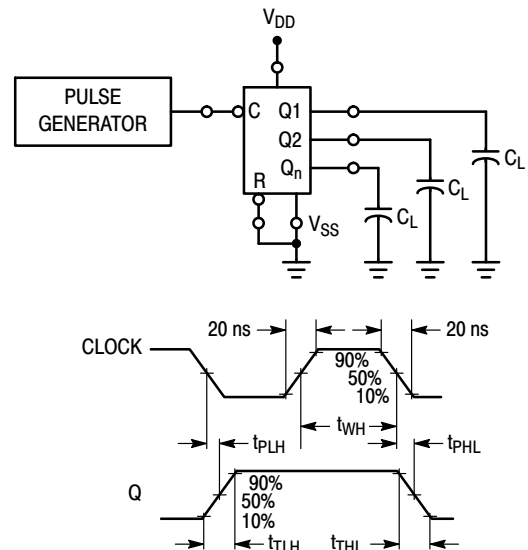
Figure 2. Switching Time Test Circuit and Waveforms

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4
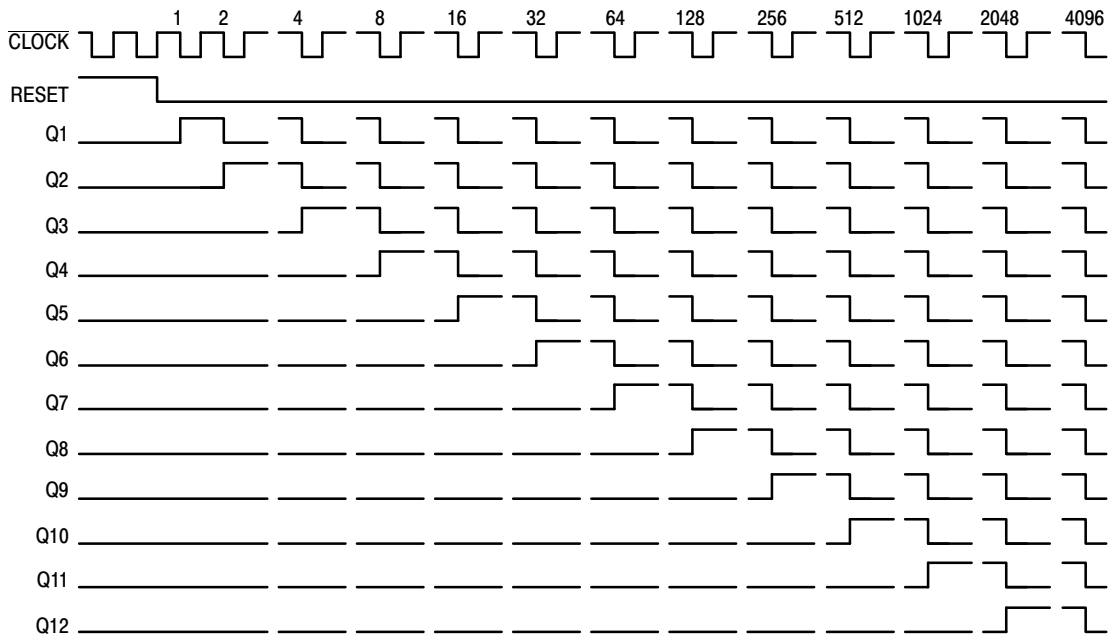
MC14040B

Figure 3. Timing Diagram

APPLICATIONS INFORMATION

TIME−BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040B. By selecting outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC14012B decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.
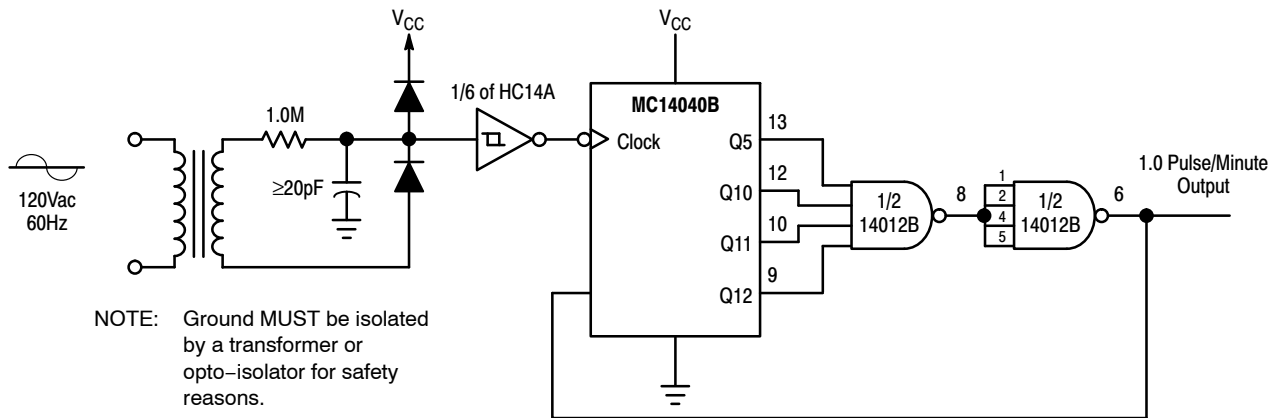

NOTE: Ground MUST be isolated by a transformer or opto−isolator for safety reasons.

Figure 4. Time−Base Generator

onsemi™

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
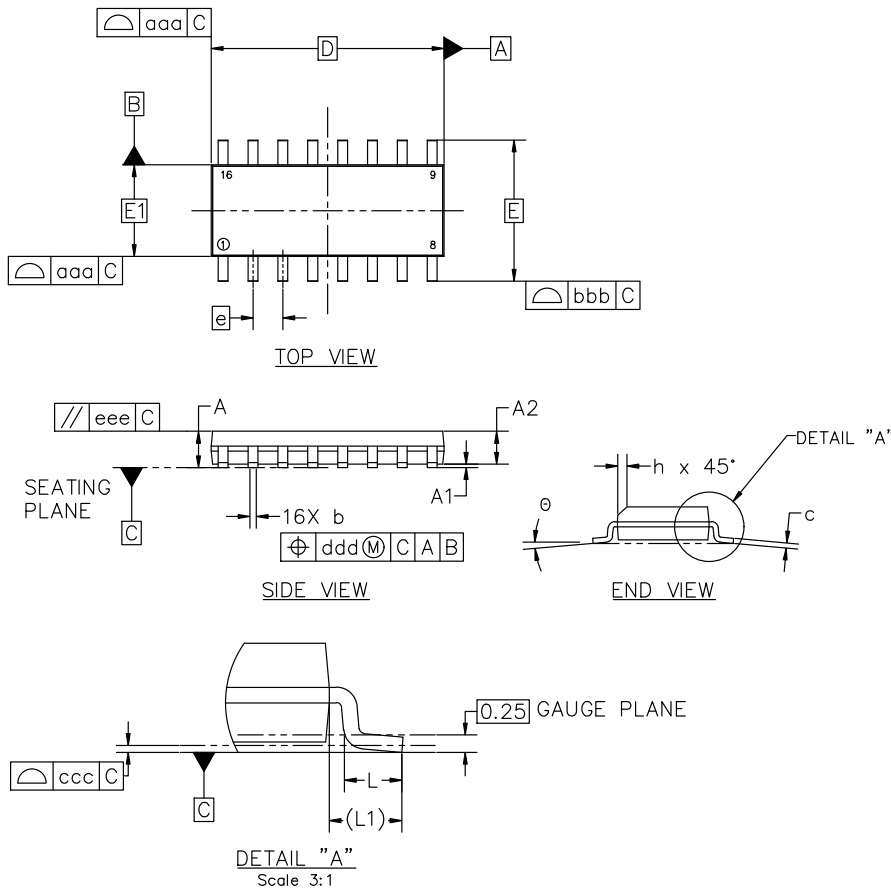
MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	———	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	———	7°

TOLERANCE OF FORM AND POSITION	
aaa	0.10
bbb	0.20
ccc	0.10
ddd	0.25
eee	0.10

TOP VIEW

SIDE VIEW

END VIEW

DETAIL "A"
Scale 3:1

0.25 GAUGE PLANE

SEATING PLANE

DETAIL "A"

8X
6.40

16X
0.58

1.270
PITCH

1.120

RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	98ASB42566B		
DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P		PAGE 1 OF 2

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

GENERIC
MARKING DIAGRAM*

```
16 ┌─────────────────┐
   │ XXXXXXXXXXXXG   │
   │ XXXXXXXXXXXXX   │
   │ ○    AWLYWW     │
 1 └─────────────────┘
```

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
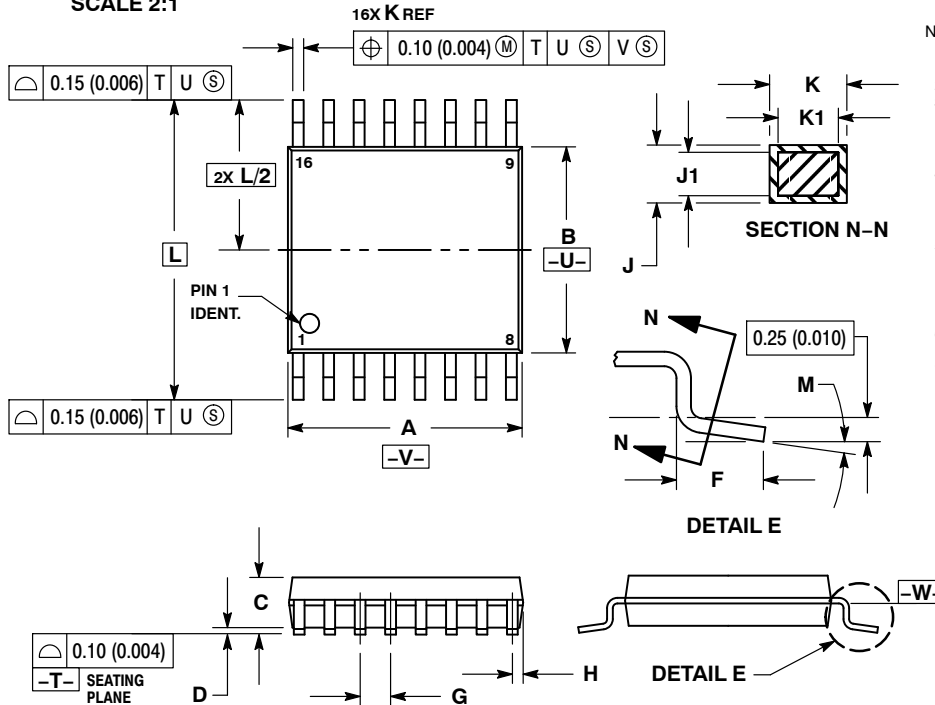15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P		PAGE 2 OF 2

onsemi™

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006

16

1

SCALE 2:1

16X K REF

⊕ | 0.10 (0.004) Ⓜ | T U Ⓢ V Ⓢ

▱ | 0.15 (0.006) | T U Ⓢ

2X L/2

L

16   9

B

−U−

PIN 1
IDENT.

1   8

A

−V−

▱ | 0.15 (0.006) | T U Ⓢ

C

▱ | 0.10 (0.004)

−T− SEATING PLANE

D   G   H

K
K1
J1
J

SECTION N−N

N

0.25 (0.010)

N   M

F

DETAIL E

−W−

DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	–––	1.20	–––	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

**RECOMMENDED
SOLDERING FOOTPRINT***

7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS

**GENERIC
MARKING DIAGRAM***

16

XXXX
XXXX
○ ALYW

1

XXXX   = Specific Device Code
A   = Assembly Location
L   = Wafer Lot
Y   = Year
W   = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98ASH70247A		
DESCRIPTION:	TSSOP−16		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical–documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

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