MC74HC4040A

12-Stage Binary Ripple Counter

High−Performance Silicon−Gate CMOS

The MC74C4040A is identical in pinout to the standard CMOS MC14040. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 12 master−slave flip−flops. The output of each flip−flop feeds the next and the frequency at each output is half of that of the preceding one. The state counter advances on the negative−going edge of the Clock input. Reset is asynchronous and active−high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4040A for some designs.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With JEDEC Standard No. 7A Requirements
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

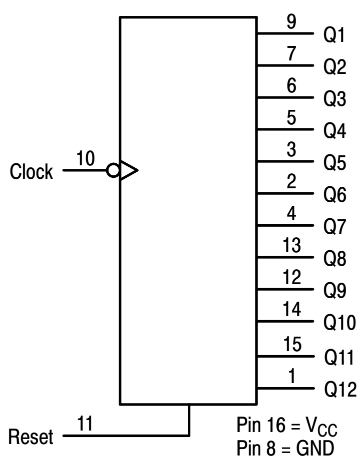

Figure 1. Logic Diagram

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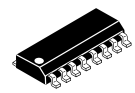
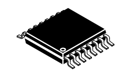
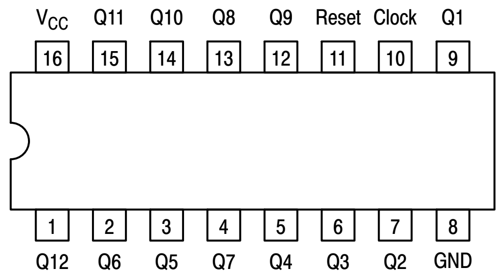


SOIC−16
D SUFFIX
CASE 751B



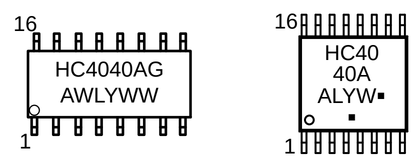
TSSOP−16
DT SUFFIX
CASE 948F

PIN ASSIGNMENT



16−Lead Package (Top View)

MARKING DIAGRAMS



SOIC−16 **TSSOP−16**

A	=	Assembly Location
L, WL	=	Wafer Lot
Y, YY	=	Year
W, WW	=	Work Week
G or ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Clock	Reset	Output State
↑	L	No Charge
↓	L	Advance to Next State
X	H	All Outputs Are Low

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds SOIC or TSSOP Package	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: –7 mW/°C from 65° to 125°C
TSSOP Package: −6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types	–55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 2) V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit −55 to 25°C	≤85°C	≤125°C	Unit
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1V or V_{CC} −0.1V $\lvert I_{out}\rvert$ ≤ 20μA	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1V or V_{CC} − 0.1V $\lvert I_{out}\rvert$ ≤ 20μA	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert$ ≤ 20μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert$ ≤ 2.4mA $\lvert I_{out}\rvert$ ≤ 4.0mA $\lvert I_{out}\rvert$ ≤ 5.2mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert$ ≤ 20μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert$ ≤ 2.4mA $\lvert I_{out}\rvert$ ≤ 4.0mA $\lvert I_{out}\rvert$ ≤ 5.2mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0μA	6.0	4	40	160	μA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit −55 to 25°C	≤85°C	≤125°C	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 5)	2.0 3.0 4.5 6.0	10 15 30 50	9.0 14 28 45	8.0 12 25 40	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q1* (Figures 2 and 5)	2.0 3.0 4.5 6.0	96 63 31 25	106 71 36 30	115 88 40 35	ns
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 3 and 5)	2.0 3.0 4.5 6.0	65 30 30 26	72 36 35 32	90 40 40 35	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Qn to Qn+1 (Figures 4 and 5)	2.0 3.0 4.5 6.0	69 40 17 14	80 45 21 15	90 50 28 22	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 5)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 15	110 36 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

* For T_A = 25°C and C_L = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:
V_{CC} = 2.0 V: t_P = [93.7 + 59.3 (n−1)] ns
V_{CC} = 4.5 V: t_P = [30.25 + 14.6 (n−1)] ns
V_{CC} = 3.0 V: t_P = [61.5 + 34.4 (n−1)] ns
V_{CC} = 6.0V: t_P = [24.4 + 12 (n−1)] ns

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	31	pF

* Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit −55 to 25°C	≤85°C	≤125°C	Unit
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 3)	2.0 3.0 4.5 6.0	30 20 5 4	40 25 8 6	50 30 12 9	ns
t_w	Minimum Pulse Width, Clock (Figure 2)	2.0 3.0 4.5 6.0	70 40 15 13	80 45 19 16	90 50 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 3)	2.0 3.0 4.5 6.0	70 40 15 13	80 45 19 16	90 50 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 2)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

PIN DESCRIPTIONS

INPUTS

Clock (Pin 10)

Negative−edge triggering clock input. A high−to−low transition on this input advances the state of the counter.

Reset (Pin 11)

Active−high reset. A high level applied to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.

OUTPUTS

Q1 thru Q12 (Pins 9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1)

Active−high outputs. Each Qn output divides the Clock input frequency by 2^N.

SWITCHING WAVEFORMS

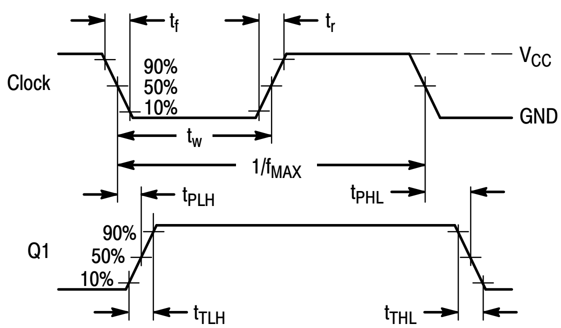


Figure 2.

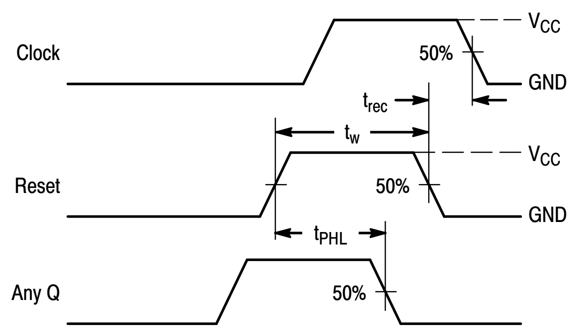


Figure 3.

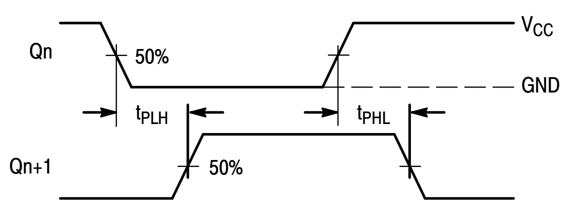
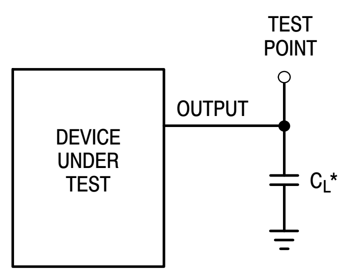


Figure 4.



*Includes all probe and jig capacitance

Figure 5. Test Circuit

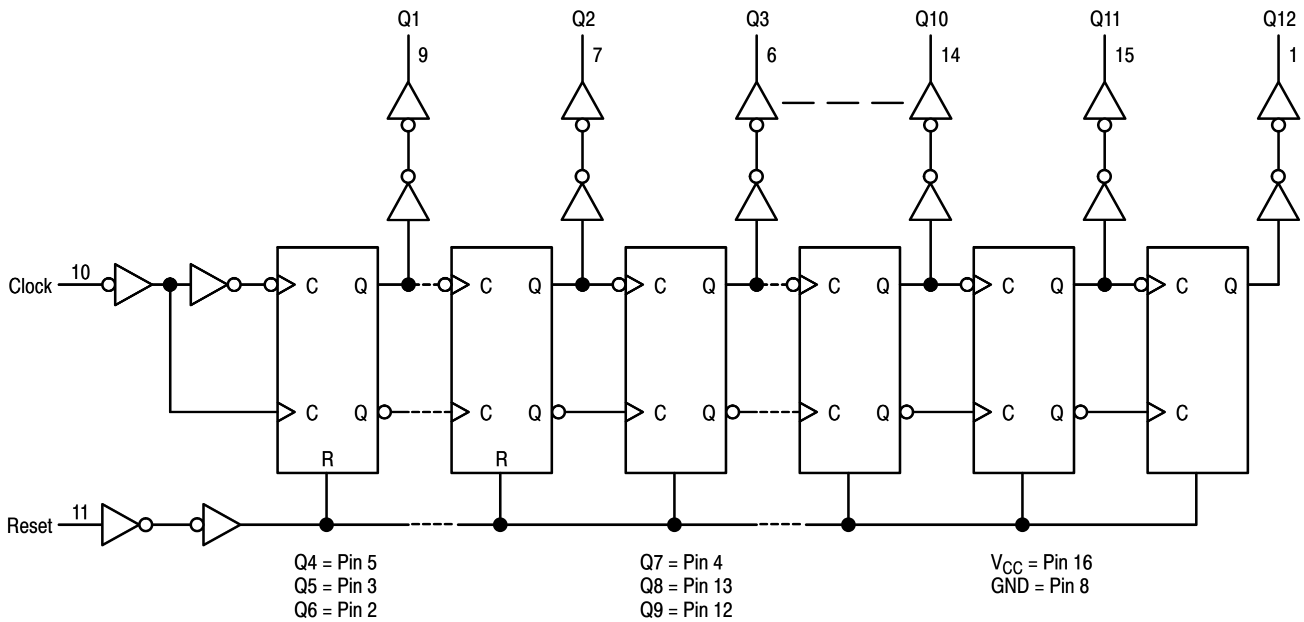


Figure 6. Expanded Logic Diagram

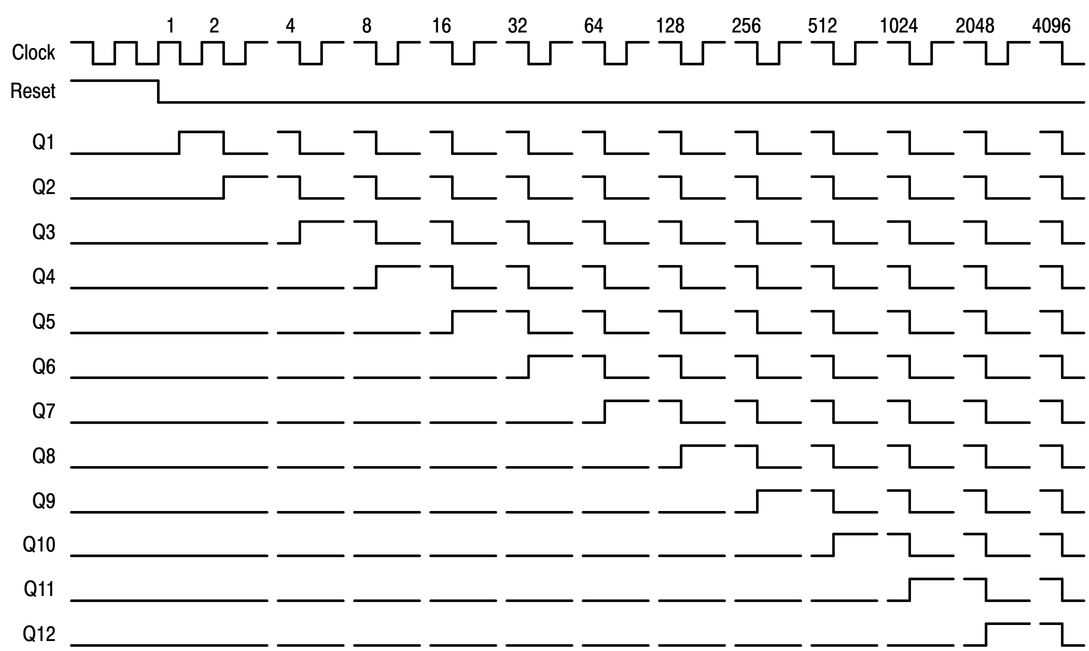
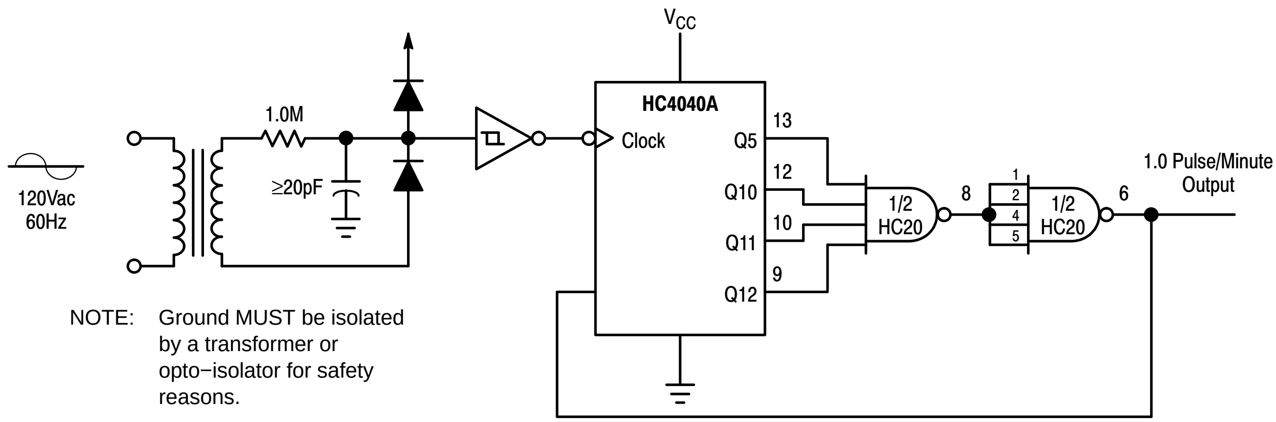


Figure 7. Timing Diagram

APPLICATIONS INFORMATION

Time−Base Generator

A 60Hz sinewave obtained through a 100 K resistor connected to a 120 Vac power line through a step down transformer is applied to the input of the MC54/74HC14A, Schmitt-trigger inverter. The HC14A squares−up the input waveform and feeds the HC4040A. Selecting outputs Q5, Q10, Q11, and Q12 causes a reset every 3600 clocks. The HC20 decodes the counter outputs, produces a single (narrow) output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



NOTE: Ground MUST be isolated by a transformer or opto−isolator for safety reasons.

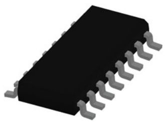
Figure 8. Time−Base Generator

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC4040ADG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74HC4040ADR2G	SOIC−16 (Pb−Free)	2500 Units / Reel
NLV74HC4040ADR2G*	SOIC−16 (Pb−Free)	2500 Units / Reel
MC74HC4040ADTR2G	TSSOP−16 (Pb−Free)	2500 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

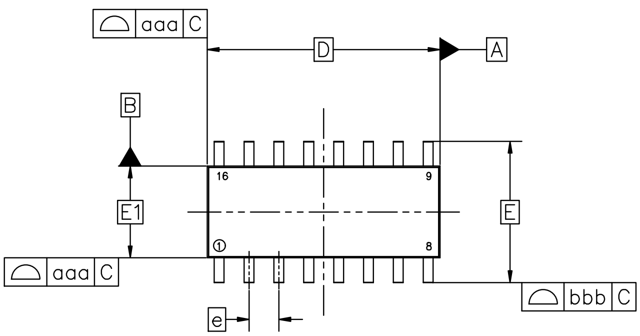


SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

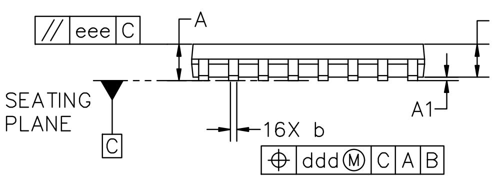
DATE 29 MAY 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

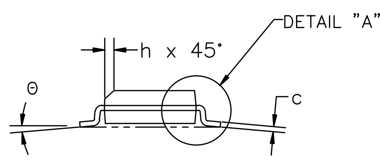
MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



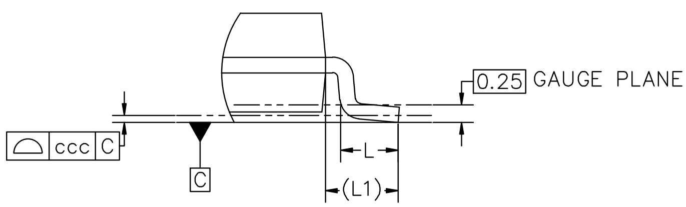
TOP VIEW



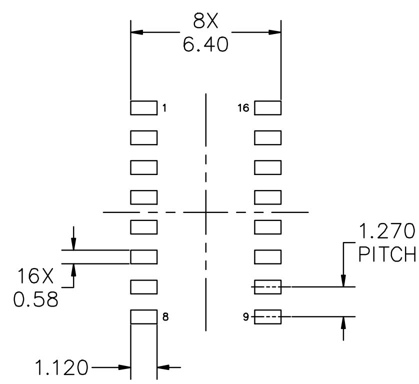
SIDE VIEW



END VIEW



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

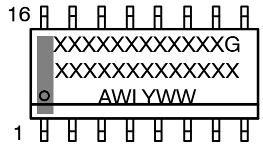
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	**98ASB42566B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−16 9.90X3.90X1.50 1.27P**	**PAGE 1 OF 2**

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

PIN	STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:
PIN 1.	COLLECTOR	CATHODE	COLLECTOR, DYE #1	COLLECTOR, DYE #1
2.	BASE	ANODE	BASE, #1	COLLECTOR, #1
3.	EMITTER	NO CONNECTION	EMITTER, #1	COLLECTOR, #2
4.	NO CONNECTION	CATHODE	COLLECTOR, #1	COLLECTOR, #2
5.	EMITTER	CATHODE	COLLECTOR, #2	COLLECTOR, #3
6.	BASE	NO CONNECTION	BASE, #2	COLLECTOR, #3
7.	COLLECTOR	ANODE	EMITTER, #2	COLLECTOR, #4
8.	COLLECTOR	CATHODE	COLLECTOR, #2	COLLECTOR, #4
9.	BASE	CATHODE	COLLECTOR, #3	BASE, #4
10.	EMITTER	ANODE	BASE, #3	EMITTER, #4
11.	NO CONNECTION	NO CONNECTION	EMITTER, #3	BASE, #3
12.	EMITTER	CATHODE	COLLECTOR, #3	EMITTER, #3
13.	BASE	CATHODE	COLLECTOR, #4	BASE, #2
14.	COLLECTOR	NO CONNECTION	BASE, #4	EMITTER, #2
15.	EMITTER	ANODE	EMITTER, #4	BASE, #1
16.	COLLECTOR	CATHODE	COLLECTOR, #4	EMITTER, #1

PIN	STYLE 5:	STYLE 6:	STYLE 7:
PIN 1.	DRAIN, DYE #1	CATHODE	SOURCE N-CH
2.	DRAIN, #1	CATHODE	COMMON DRAIN (OUTPUT)
3.	DRAIN, #2	CATHODE	COMMON DRAIN (OUTPUT)
4.	DRAIN, #2	CATHODE	GATE P-CH
5.	DRAIN, #3	CATHODE	COMMON DRAIN (OUTPUT)
6.	DRAIN, #3	CATHODE	COMMON DRAIN (OUTPUT)
7.	DRAIN, #4	CATHODE	COMMON DRAIN (OUTPUT)
8.	DRAIN, #4	CATHODE	SOURCE P-CH
9.	GATE, #4	ANODE	SOURCE P-CH
10.	SOURCE, #4	ANODE	COMMON DRAIN (OUTPUT)
11.	GATE, #3	ANODE	COMMON DRAIN (OUTPUT)
12.	SOURCE, #3	ANODE	COMMON DRAIN (OUTPUT)
13.	GATE, #2	ANODE	GATE N-CH
14.	SOURCE, #2	ANODE	COMMON DRAIN (OUTPUT)
15.	GATE, #1	ANODE	COMMON DRAIN (OUTPUT)
16.	SOURCE, #1	ANODE	SOURCE N-CH

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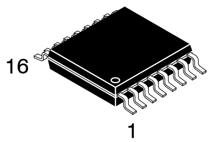
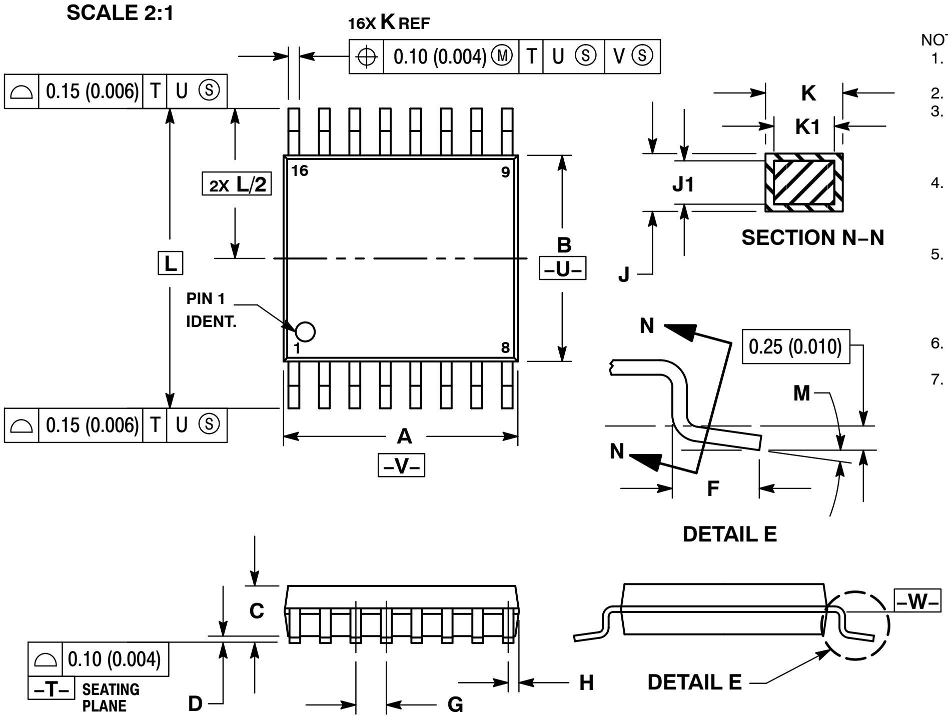


SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

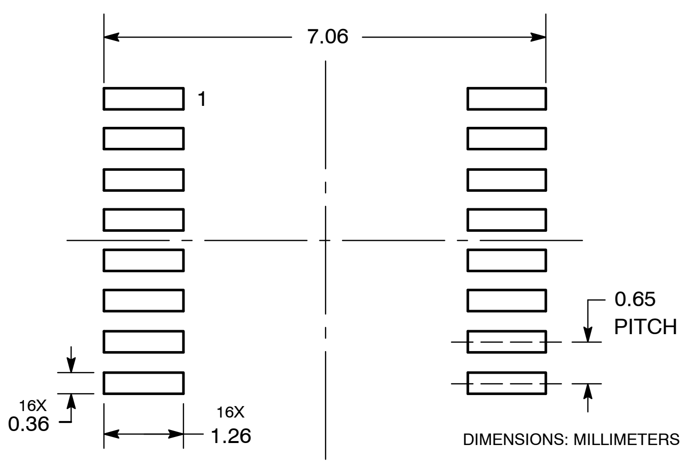
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

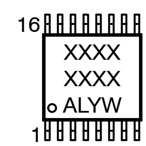
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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