Dual D-Type Flip-Flop with Preset and Clear

MM74HC74A

The MM74HC74A utilizes advanced silicon−gate CMOS technology to achieve operating speeds similar to the equivalent LS−TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS−TTL loads.

This flip−flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive−going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

The 74HC logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical Propagation Delay: 12 ns
- Wide Power Supply Range: 2 V – 6 V
- Low Quiescent Current: 80 μA maximum (74HC Series)
- Low Input Current: 1 μA Maximum
- Fanout of 10 LS−TTL Loads
- These Devices are Pb−Free, Halide Free and are RoHS Compliant

Connection Diagram

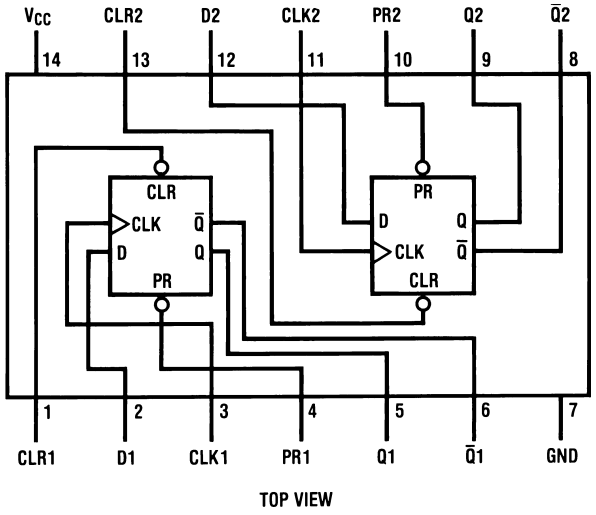
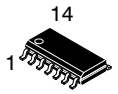
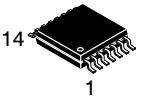


Figure 1. Pin Assignments for SOIC and TSSOP

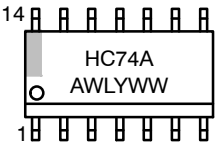


SOIC−14
CASE 751EF

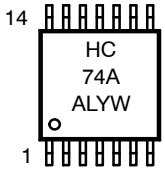


TSSOP−14 WB
CASE 948G

MARKING DIAGRAM



SOIC−14 NB



TSSOP−14 WB

HC74A = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week

TRUTH TABLE

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note1)	H (Note1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

Q0 = the level of Q before the indicated input conditions were established.

1. This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (HIGH) level.

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

Logic Diagram

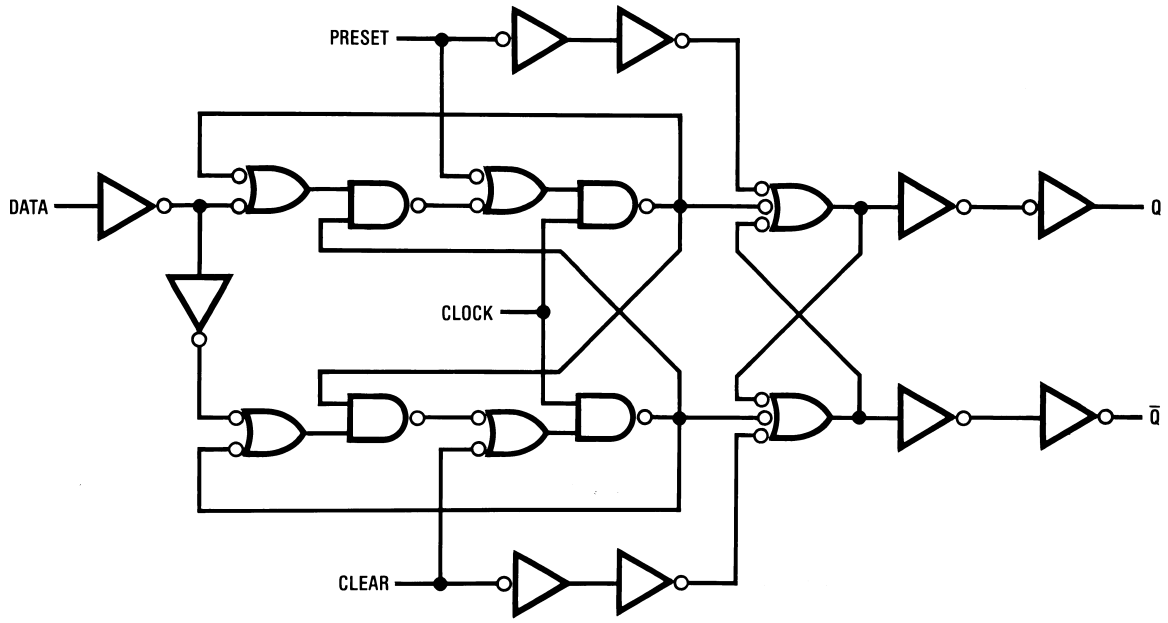


Figure 2. Logic Diagram

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5 to +6.5 V
V_{IN}	DC Input Voltage	–0.5 to V_{CC} + 0.5 V
V_{OUT}	DC Output Voltage	–0.5 to V_{CC} + 0.5 V
I_{IK}, I_{OK}	Clamp Diode Current	±20 mA
I_{OUT}	DC Output Current, per Pin	±25 mA
I_{CC}	DC V_{CC} or GND Current, per Pin	±50 mA
T_{STG}	Storage Temperature Range	–65°C to +150°C
P_D	Power Dissipation SOIC–14 TSSOP–14	1077 mW 833 mW
T_L	Lead Temperature (Soldering 10 Seconds)	260°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range		–55	+125	°C
t_r, t_f	Input Rise or Fall Times	V_{CC} = 2.0 V	–	1000	ns
		V_{CC} = 4.5 V	–	500	ns
		V_{CC} = 6.0 V	–	400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC CHARACTERISTICS (Note 3)

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C	T_A = −40°C to 85°C	T_A = −55°C to 125°C	Unit
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	2.0		–	1.5	1.5	1.5	V
		4.5		–	3.15	3.15	3.15	
		6.0		–	4.2	4.2	4.2	
V_{IL}	Maximum LOW Level Input Voltage	2.0		–	0.5	0.5	0.5	V
		4.5		–	1.35	1.35	1.35	
		6.0		–	1.8	1.8	1.8	
V_{OH}	Minimum HIGH Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 20$ μA	2.0	1.9	1.9	1.9	V
		4.5		4.5	4.4	4.4	4.4	
		6.0		6.0	5.9	5.9	5.9	
		4.5	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 4.0$ mA	4.3	3.98	3.84	3.7	
		6.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 5.2$ mA	5.2	5.48	5.34	5.2	
V_{OL}	Maximum LOW Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 20$ μA	0	0.1	0.1	0.1	V
		4.5		0	0.1	0.1	0.1	
		6.0		0	0.1	0.1	0.1	
		4.5	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 4.0$ mA	0.2	0.26	0.33	0.4	
		6.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 5.2$ mA	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	6.0	$V_{IN} = V_{CC}$ or GND	–	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND, I_{OUT} = 0 μA	–	4.0	40	80	μA

3. For a power supply of 5 V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

AC CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
f_{MAX}	Maximum Operating Frequency		72	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		10	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset or Clear to Q or $\overline{Q}$		17	40	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock		6	5	ns
t_s	Minimum Setup Time, Data to Clock		10	20	ns
t_H	Minimum Hold Time, Clock to Data		0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC CHARACTERISTICS (C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified))

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C	T_A = −40°C to 85°C	T_A = −55°C to 125°C		Unit
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	2.0		22	6	5	4	ns
		4.5		72	30	24	20	
		6.0		94	35	28	24	
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$	2.0		34	110	140	165	ns
		4.5		12	22	28	33	
		6.0		10	19	24	28	
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset or Clear to Q or $\overline{Q}$	2.0		66	150	190	225	ns
		4.5		20	30	38	45	
		6.0		16	26	33	38	
t_{REM}	Minimum Removal Time, Preset or Clear to Clock	2.0		20	50	65	75	ns
		4.5		6	10	13	15	
		6.0		5	9	11	13	
t_s	Minimum Setup Time, Data to Clock	2.0		35	80	100	120	ns
		4.5		10	16	20	24	
		6.0		8	14	17	20	
t_H	Minimum Hold Time, Clock to Data	2.0		–	0	0	0	ns
		4.5		–	0	0	0	
		6.0		–	0	0	0	
t_W	Minimum Pulse Width Clock, Preset or Clear	2.0		30	80	101	119	ns
		4.5		9	16	20	24	
		6.0		8	14	17	20	
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	2.0		25	75	95	110	ns
		4.5		7	15	19	22	
		6.0		6	13	16	19	
t_r, t_f	Maximum Input Rise and Fall Time	2.0		–	1000	1000	1000	ns
		4.5		–	500	500	500	
		6.0		–	400	400	400	
C_{PD}	Power Dissipation Capacitance (Note 4)		(per flip−flop)	80	–	–	–	pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

ORDERING INFORMATION

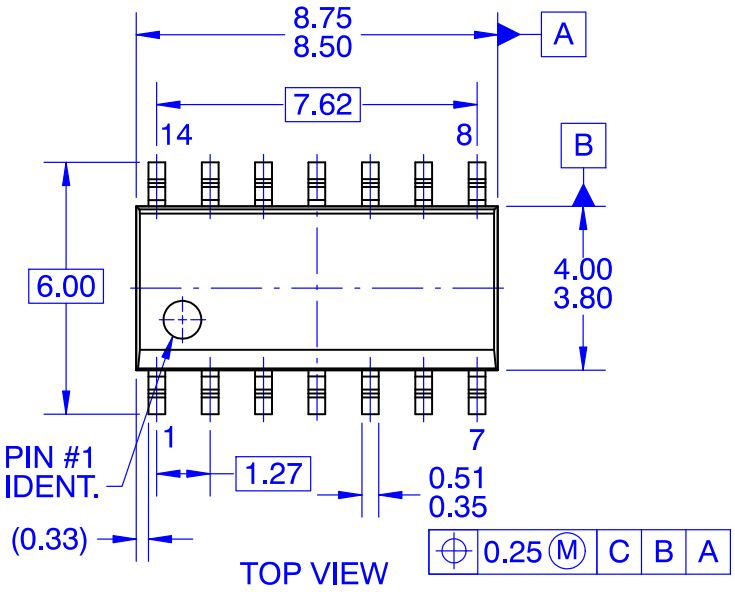
Part Number	Package	Shipping†
MM74HC74AM	SOIC−14, Case 751EF (Pb−Free, Halide Free)	55 Units / Tube
MM74HC74AMTC	TSSOP−14, Case 948G−01 (Pb−Free, Halide Free)	96 Units / Tube
MM74HC74AMX	SOIC−14, Case 751EF (Pb−Free, Halide Free)	2500 / Tape & Reel
MM74HC74AMTCX	TSSOP−14 WB, Case 948G−01 (Pb−Free, Halide Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

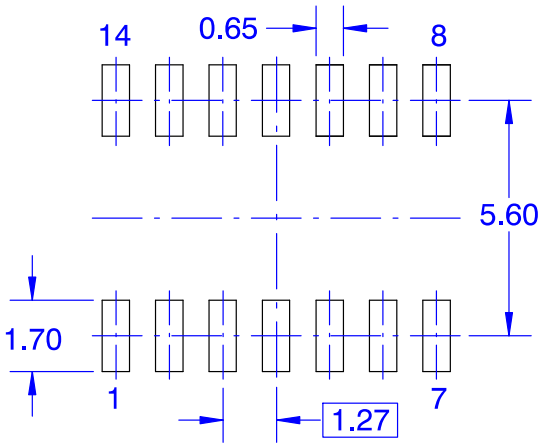
NOTE: Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

SOIC14
CASE 751EF
ISSUE O

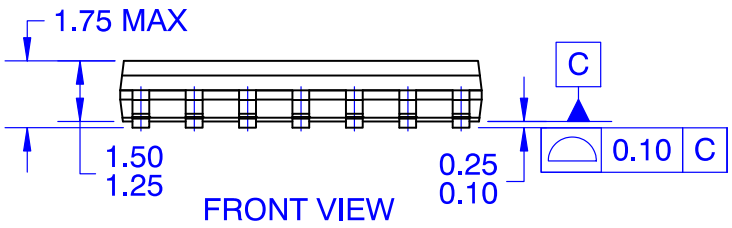
DATE 30 SEP 2016



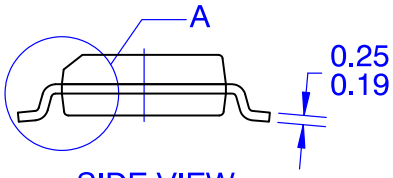
TOP VIEW



LAND PATTERN RECOMMENDATION

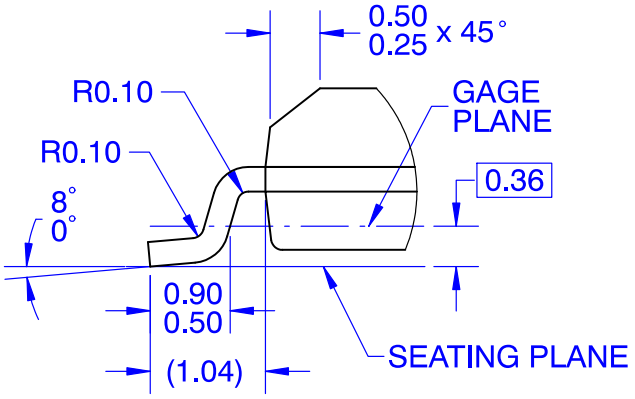


FRONT VIEW



SIDE VIEW

NOTES:
A. CONFORMS TO JEDEC MS−012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145−14M
E. CONFORMS TO ASME Y14.5M, 2009



DETAIL A
SCALE 16 : 1

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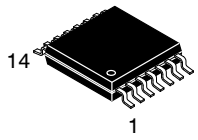
DESCRIPTION:	**SOIC14**	**PAGE 1 OF 1**

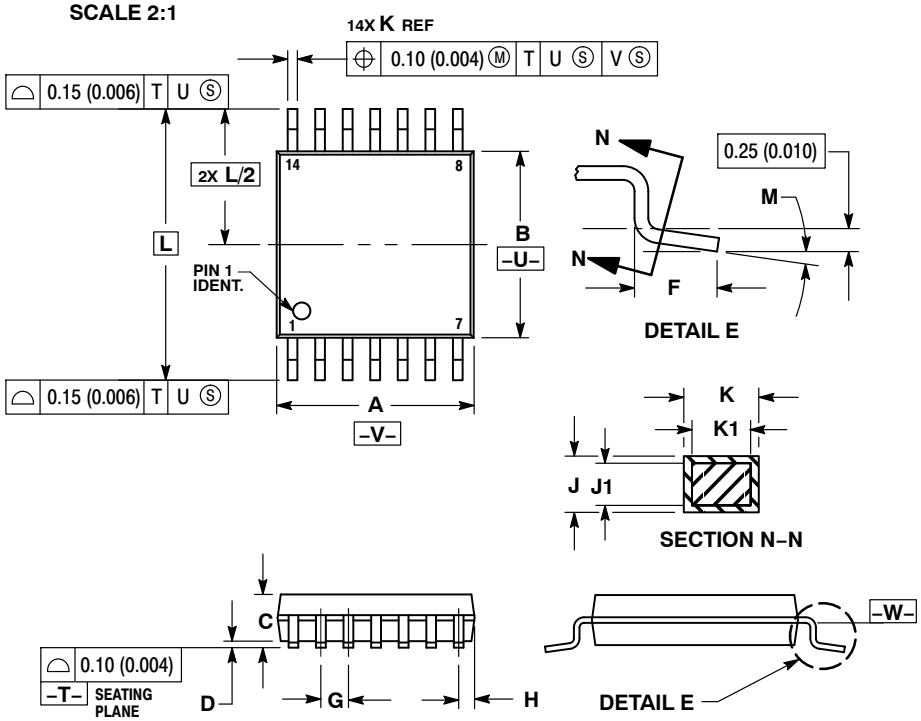
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



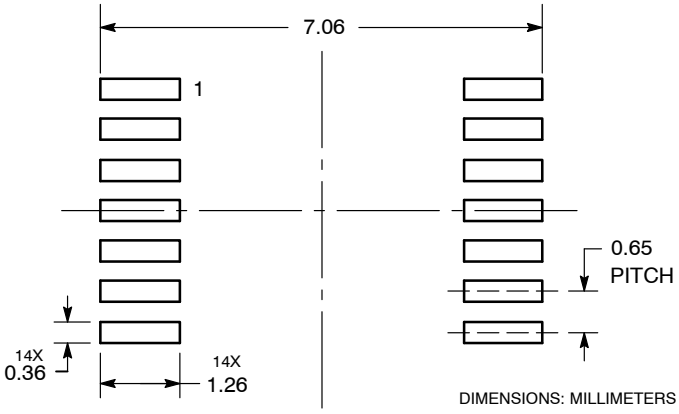
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

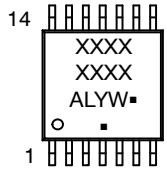
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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onsemi Website: www.onsemi.com

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