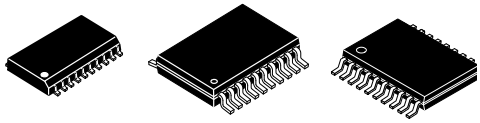
Octal 3-State Transceiver

MM74HCT245



SOIC−20 WB
CASE 751D−05

TSSOP−20 WB
CASE 948E

TSSOP−20 WB
CASE 948AQ

Description

The MM74HCT245 3−STATE bi−directional buffer utilizes advanced silicon−gate CMOS technology and is intended for two−way asynchronous communication between data buses. It has high drive current outputs which enable high speed operation even when driving large bus capacitances. This circuit possesses the low power consumption of CMOS circuitry, yet has speeds comparable to low power Schottky TTL circuits.

This device is TTL input compatible and can drive up to 15 LS−TTL loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

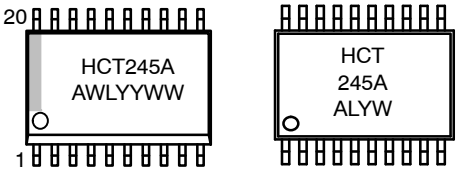
The MM74HCT245 has one active low enable input (G), and a direction control (DIR). When the DIR input is HIGH, data flows from the A inputs to the B outputs. When DIR is LOW, data flows from B to A.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug−in replacements for LS−TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL Input Compatible
- 3−STATE Outputs for connection to system busses
- High Output Drive Current: 6 mA (min)
- High Speed: 16 ns Typical propagation delay
- Low Power: 160 μA (74HCT Series)

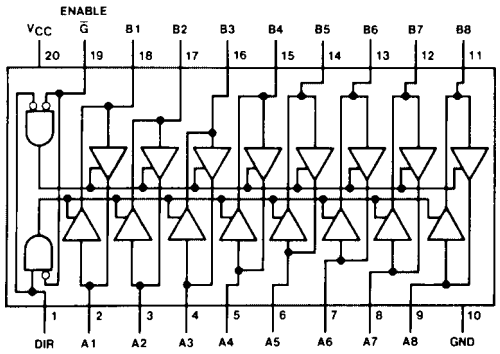
MARKING DIAGRAMS



(SOIC−20 WB) (TSSOP−WB)

HCT245A = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

CONNECTION DIAGRAM



Top View

TRUTH TABLE

Control Inputs		Operation
$\overline{G}$	DIR	245
L	L	B data to A bus
L	L	A data to B bus
H	H	isolation

H = HIGH Level
L = LOW Level
X = Irrelevant

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

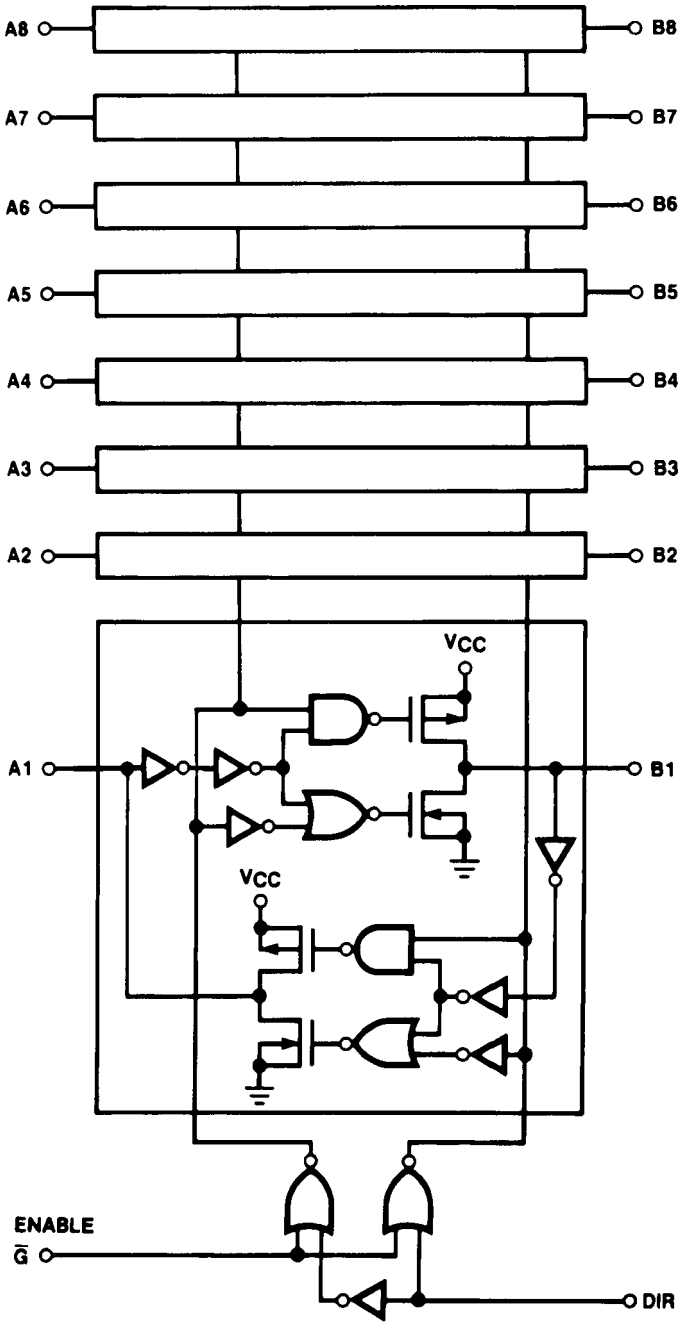


Figure 1. Logic Diagram

ABSOLUTE MAXIMUM RATINGS (Note 1) (Note 2)

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	−0.5 to +7.0	V
V_{IN}	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_{OUT}	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}, I_{OK}	Clamp Diode Current	±20	mA
I_{OUT}	DC Output Current, per pin	±35	mA
I_{CC}	Maximum Junction Temperature	±70	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
P_D	Power Dissipation S.O. Package only	500	mW
T_L	Lead Temperature (Soldering 10 seconds)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING RANGES

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	−55	+125	°C
t_r, t_f	Input Rise or Fall Times	–	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10%, unless otherwise specified.)

Symbol	Parameter	Test Conditions	T_A = 25°C	T_A = –40°C to 85°C	T_A = –55°C to 125°C	Unit
			Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	–	–	2.0	2.0	2.0	V
V_{IL}	Maximum LOW Level Input Voltage	–	–	0.8	0.8	0.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 20 μA $\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5 V $\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5 V	V_{CC} 4.2 5.2	V_{CC} – 0.1 3.98 4.98	V_{CC} – 0.1 3.84 4.84	V_{CC} – 0.1 3.7 4.7	V
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 20 μA $\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5 V $\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5 V	0 0.2 0.2	0.1 0.26 0.26	0.1 0.33 0.33	0.1 0.4 0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND V_{IH} or V_{IL}, Pin 1or 19	–	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum 3–STATE Output Leakage Current	V_{out} = V_{CC} or GND $\overline{G}$ = V_{IH}	–	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA	–	8	80	160	μA
		V_{IN} = 2.4 V or 0.5 V (Note 4)	0.6	1.0	1.3	1.5	mA

3. Measured per input. All other inputs at V_{CC} or ground.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, t_r = t_f = 6 ns, T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Typ.	Guaranteed Limit	Unit
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 45 pF	16	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L = 45 pF R_L = 1 kQ	29	40	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L = 5 pF R_L = 1 kQ	20	25	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±10%, $t_r = t_f$ = 6 ns, unless otherwise specified)

Symbol	Parameter	Test Conditions	T_A = 25°C		T_A = –40°C to 85°C	T_A = –55°C to 125°C	Unit
			Typ.	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF	17	23	29	34	ns
		C_L = 150 pF	24	30	38	45	
t_{PZL}	Maximum Output Enable Time	R_L = 1 kQ C_L = 50 pF	31	42	53	63	ns
t_{PZH}	Maximum Output Enable Time	R_L = 1 kQ C_L = 50 pF	23	33	41	49	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kQ C_L = 50 pF	21	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	8	12	15 NIL	18	ns
C_{IN}	Maximum Input Capacitance	–	10	15	15	15	pF
C_{OUT}	Maximum Output/Input Capacitance	–	20	25	25	25	pF
C_{PD}	Power Dissipation Capacitance	$\overline{G}$ = V_{CC} (Note 5) $\overline{G}$ = GND	7 100	–	–	–	pF pF

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

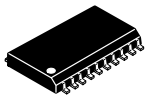
ORDERING INFORMATION

Product Number	Package	Shipping†
MM74HCT245MTC	TSSOP–20 WB,Case, 948E (Pb–Free)	75 Units / Tube
MM74HCT245MTCX	TSSOP–20 WB, 948AQ (Pb–Free)	2500 Units / Tape and Reel
MM74HCT245WM	SOIC–20 WB (Pb–Free)	38 Units / Tube
MM74HCT245WMX	SOIC–20 WB (Pb–Free)	1000 Units / Tape and Reel

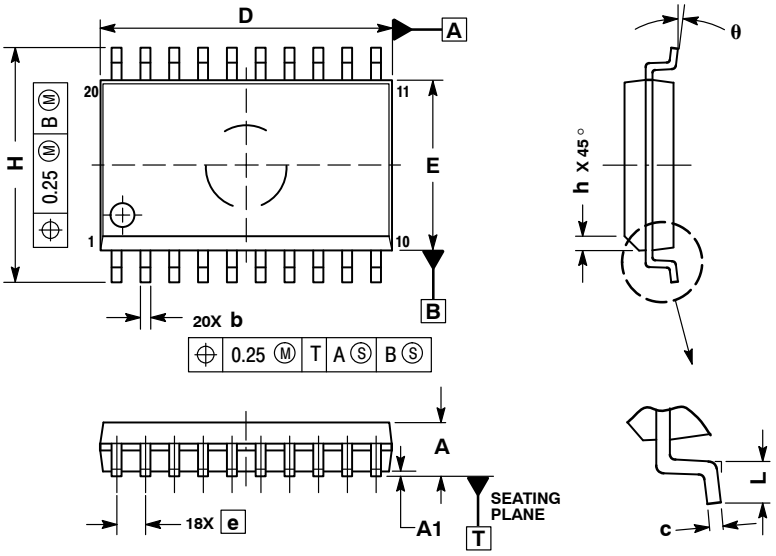
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015



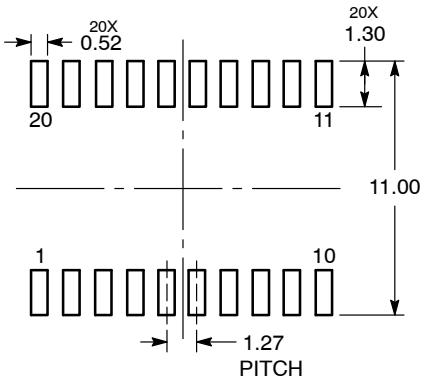
SCALE 1:1



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

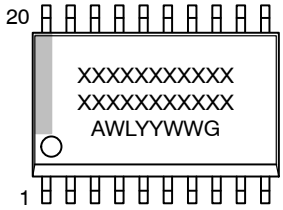
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

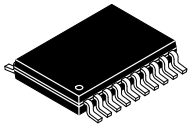
DOCUMENT NUMBER:	**98ASB42343B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−20 WB**		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016



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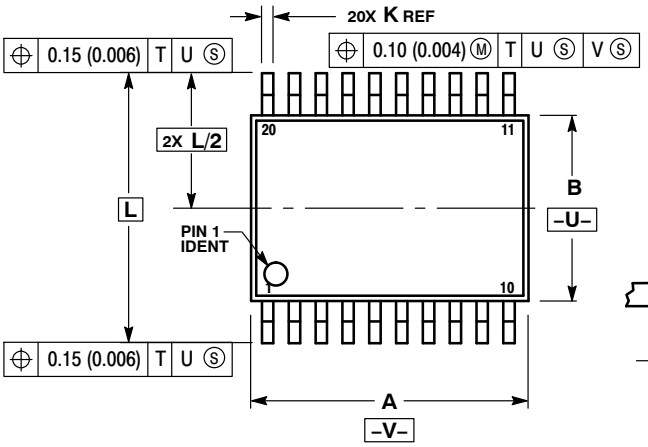
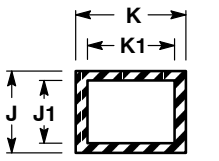
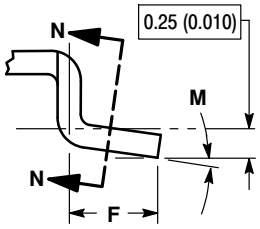
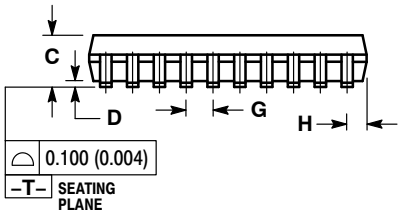


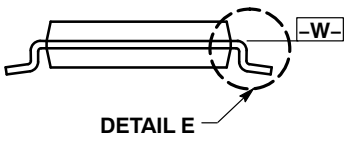


SECTION N−N



DETAIL E

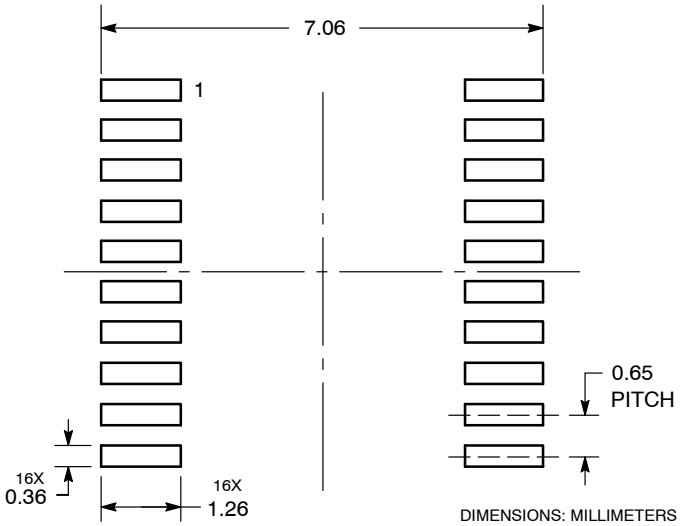




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

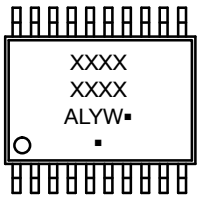
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

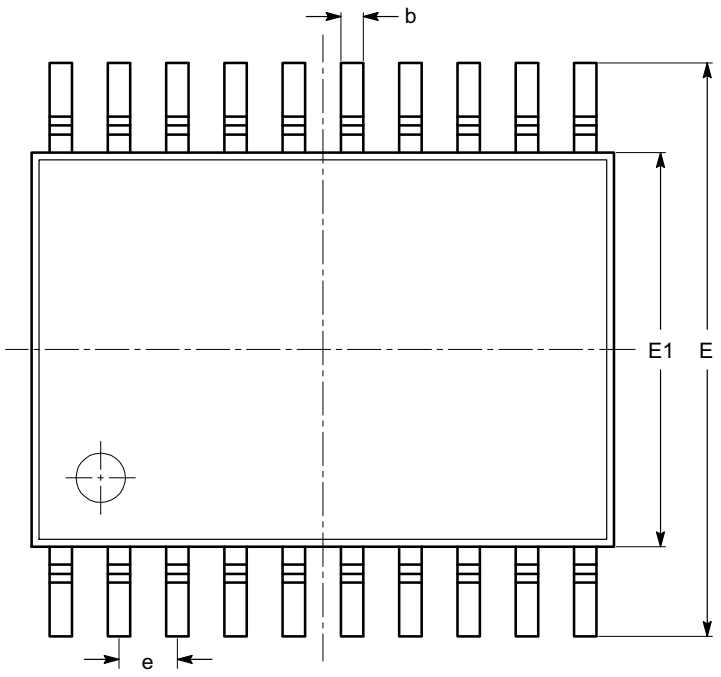
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98ASH70169A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	TSSOP−20 WB	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

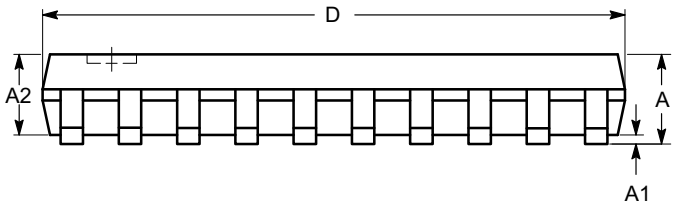
TSSOP20, 4.4x6.5
CASE 948AQ
ISSUE A

DATE 19 MAR 2009

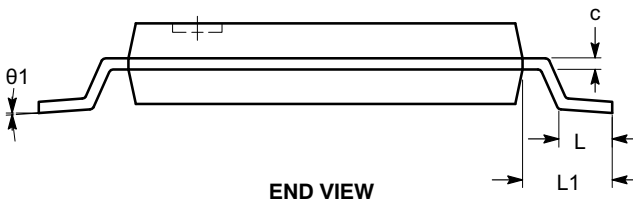


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

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DESCRIPTION:	TSSOP20, 4.4X6.5	PAGE 1 OF 1

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