The Future of Analog IC Technology

MP6543

22V, 2A three-phase power stage

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP6543 family products are all 3-phase brushless DC motor driver. They integrate 3 half bridges, consisting of 6 N-channel Power MOSFETs, along with pre-drivers, gate drive power supplies, and current sense amplifiers.

The MP6543 has ENABLE and PWM inputs for each ½-H-bridge; the MP6543A has separate high-side and low-side inputs; the MP6543B has hall-element inputs. Otherwise, they are similar. References to the MP6543 in this document also apply to the other parts unless otherwise noted.

The MP6543 is able to deliver up 2A continuously (depending on thermal and PCB conditions), with the adjustable over current protection threshold. It uses an internal charge pump to generate the gate drive supply voltage for the high-side MOSFETs, and a trickle charge circuit that maintains sufficient gate drive voltage to operate at 100% duty cycle.

Internal safety features include thermal shutdown, under-voltage lockout and over-current protection.

The MP6543, MP6543A and MP6543B is available in a 24-pin, 3mm x 4mm QFN with an exposed thermal pad.

FEATURES

- 3V to 22V Operating Supply Voltage
- Three integrated half-bridge drivers
- 2A Continuous Output Current
- MOSFET On-Resistance: 110mΩ per FET
- MP6543: PWM & ENBL inputs (QFN3x4-24)

Options:

- MP6543A: HS & LS inputs (QFN3x4-24)
- MP6543B: Hall Signal Interface(QFN3x4-24)
- Built-In 3.3-V, 100-mA LDO Regulator
- Internal Charge Pump Supports 100% Duty Cycle Operation
- Automatic Synchronous Rectification
- UVLO and Thermal Shutdown Protection
- Over-current Protection, and threshold programmable
- Integrated Bi-directional Current Sense Amplifiers
- Available in QFN-24 (3mmx4mm) package

APPLICATIONS

- 3-Phase BLDC Motor Drive

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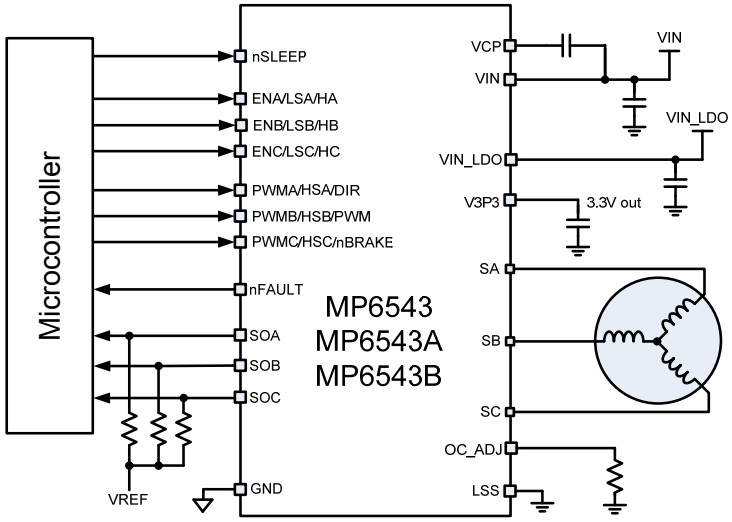
TYPICAL APPLICATION



MP6543/6543A/6543B Typical Application Circuit (QFN3x4-24)

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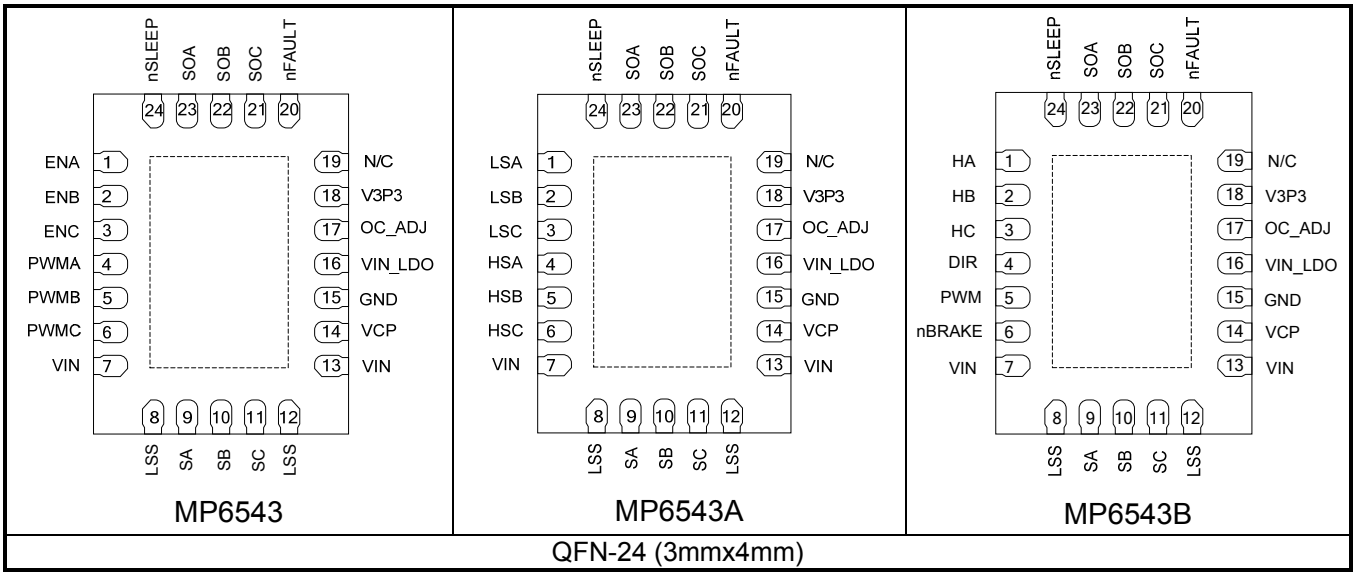
ORDERING INFORMATION

Part Number*	Package	Top Marking

PACKAGE REFERENCE



QFN-24 (3mmx4mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN}, V_{IN_LDO} .....–0.3V to +25V
V_{Sx}..... –0.3V to V_{IN} +0.3V
V_{CP} ..... –0.3V to V_{IN} +5V
AGND to PGND .....–0.3V to +0.3V
Voltage at all other pins ..... –0.3 to +5V
Continuous Power Dissipation (T_A = +25°C) **(2)**
QFN-24(3mmx4mm)……...2.6W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....3V to 22V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-24 (3mm×4mm)…..…..... 48 .....10.....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Continuous current depends on PCB layout and ambient temperature.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 18V, T_A = 25°C, LSS = GND = 0V, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}, V_{IN_LDO}		3		22	V
Quiescent current	I_Q	nSLEEP = 1, ENx = 0		1	5	mA
	I_{SLEEP}	nSLEEP = 0		50		µA
Control Logic						
Input logic 'low' threshold	V_{IL}				0.4	V
Input logic 'high' threshold	V_{IH}		1.5			V
Logic input current	$I_{IN(H)}$	V = 5V	-20		20	µA
	$I_{IN(L)}$	V = 0V	-20		20	µA
Power up delay	t_{PUD}	At V_{IN} rising or nSLEEP rising		1		mS
Internal pull down resistance	R_{PD}	All logic Inputs		500		kΩ
nFAULT pull down R_{ON}	$R_{ON(NFAULT)}$			15		Ω
V3P3 REGULATOR						
LDO output		IOUT = 0 to 100 mA	3	3.3	3.6	V
Protection Circuits						
UVLO threshold	V_{UVLO}	V_{IN} rising	2.5	2.7	2.9	V
UVLO hysteresis	ΔV_{UVLO}			150		mV
OCP threshold	I_{OCP}	ROCP=0	5	6	7	A
		ROCP=float	7	8	9	A
OCP deglitch time	t_{OCD}			1		µs
OCP retry time	t_{OCR}			4		ms
Thermal Shutdown[6]	T_{TSD}	TJ Rising		160		°C
Thermal Shutdown Hysteresis[6]	ΔT_{TSD}			25		°C
Current sense						
Current sense ratio			1/3600	1/4000	1/4400	A/A
Current sense output current		LS FET current = 1A	90	100	110	µA
		LS FET current = -1A	-90	-100	-110	µA
Current sense output current		LS FET current = 100mA	90	100	110	µA
		LS FET current = -100mA	-9	-10	-11	µA
positive and negative matching (ratio of positive to negative)		LS FET current = +-1A, +-100mA	95%	1	105%	
Phase matching (ratio of phase to phase)		LS FET current = +-1A, +-100mA	95%	1	105%	
Current sense output voltage swing		LS FET current = +-2A, 9k	0		3.6	V
Output						
HS FET on resistance	$R_{ON(HS)}$	IOUT= 1A		110		mΩ
LS FET on resistance	$R_{ON(LS)}$	IOUT= 1A		110		
Output rise time		R_{LOAD} = 50Ω		25		nS
Output fall time		R_{LOAD} = 50Ω		25		nS
Dead Time[6]		R_{LOAD} = 50Ω		40		nS

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 18V, T_A = 25°C, LSS = GND = 0V, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PWMx to Sx Delay Time Rising				70		nS
PWMx to Sx Delay Time Falling				70		nS
Charge pump						
Charge pump output voltage	V_{CP}			V_{IN} + 3.6		V

Note:
6) Guaranteed by design.

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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 18V, T_A = 25°C, unless otherwise noted.

TBD

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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 18V, T_A = 25°C, unless otherwise noted.

TBD

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PIN FUNCTIONS

QFN3x4-24 Pin #	MP6543 Name	MP6543A Name	MP6543B Name	Description
1	ENA	-	-	Enable Input for Phase A.
	-	LSA	-	Enable Low-side FET for Phase A.
	-	-	HA	Hall-sensor input, phase A.
2	ENB	-	-	Enable Input for Phase B.
	-	LSB	-	Enable Low-side FET for Phase B.
	-	-	HB	Hall-sensor input, phase B.
3	ENC	-	-	Enable Input for Phase C.
	-	LSC	-	Enable Low-side FET for Phase C.
	-	-	HC	Hall-sensor input, phase C.
4	PWMA	-	-	PWM Input Pin for Phase A
	-	HSA	-	Enable High-side FET for Phase A.
	-	-	DIR	A logic input to determine the direction of motor torque output.
5	PWMB	-	-	PWM Input Pin for Phase B
	-	HSB	-	Enable High-side FET for Phase B.
	-	-	PWM	External PWM control for speed/torque.
6	PWMC	-	-	PWM Input Pin for Phase C
	-	HSC	-	Enable High-side FET for Phase C.
	-	-	nBRAKE	An active-low logic input for a braking function.
7	VIN			Input Power
8	LSS			Low-side Source Connection for Phase A, B, C. Must be connected directly to GND.
9	SA			Phase A output
10	SB			Phase B output
11	SC			Phase C output
12	LSS			Low-side Source Connection for Phase A, B, C. Must be connected directly to GND.
13	VIN			Input Power
14	VCP			Charge Pump Output. Connect a 1uF 16V X7R ceramic capacitor to VIN
15	GND			Ground
16	VIN_LDO			LDO input.
17	OC_ADJ			Over-Current threshold programming pin
18	V3P3			3.3V regulator output, and low-side gate drive voltage bypass. Bypass to GND with a 0.47uF capacitor.
19	N/C			No Connection.
20	nFAULT			Fault Indication. Open-drain output type, logic low when in fault condition.
21	SOC			Current Sense Output for Phase C
22	SOB			Current Sense Output for Phase B

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PIN FUNCTIONS *(continued)*

QFN3x4-24 Pin #	MP6543 Name	MP6543A Name	MP6543B Name	Description
23	SOA			Current Sense Output for Phase A
24	nSLEEP			Sleep Mode Input. Logic high to enter low-power sleep mode. Internal pull down.

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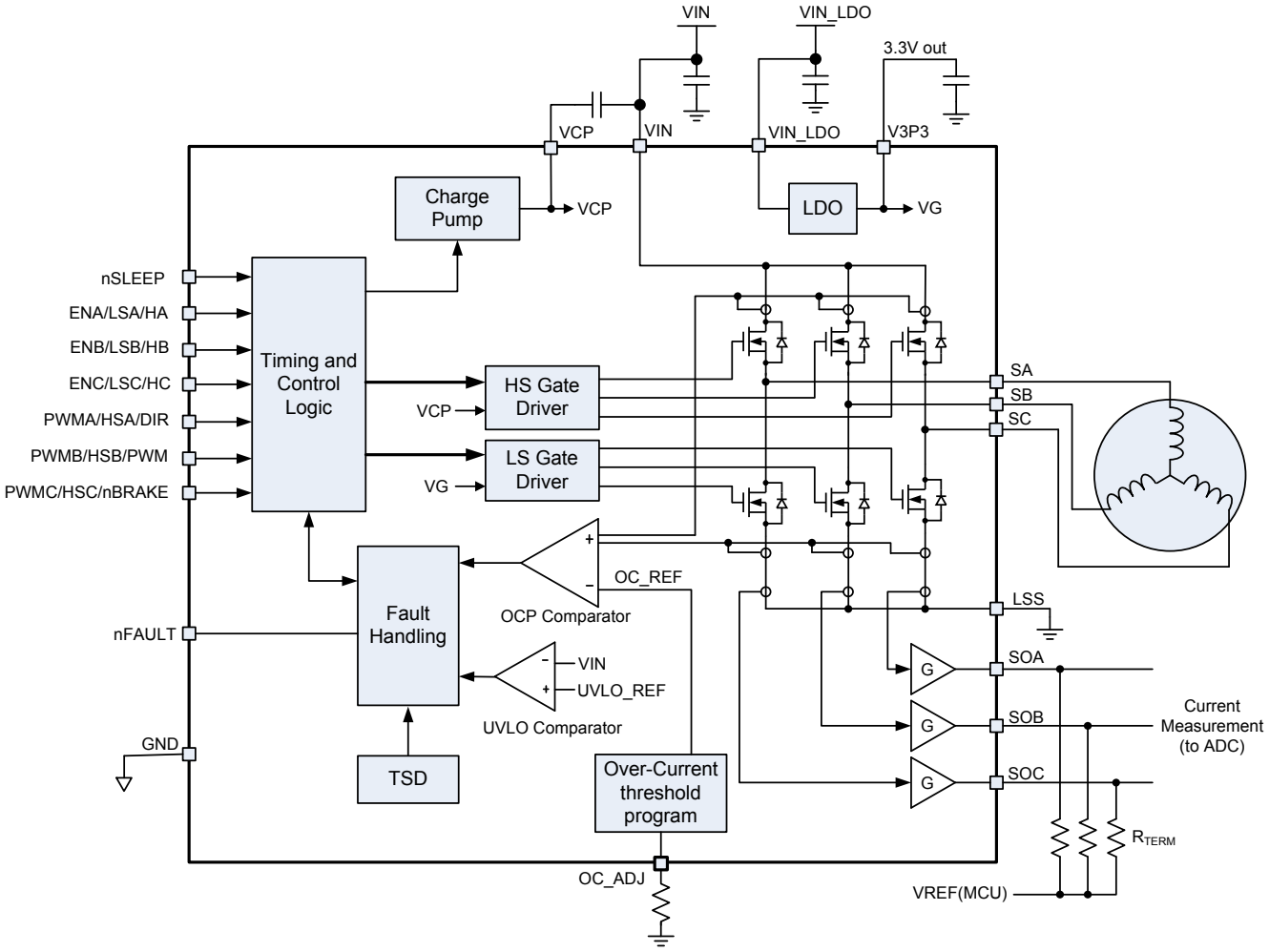
BLOCK DIAGRAM (MP6543/MP6543A/MP6543B)



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OPERATION

The MP6543 is a 3-channel half-bridge driver intended to drive a brushless DC motor.

Input Logic

The MP6543 has logic input pins ENA, ENB, and ENC, which enable the outputs SA, SB, and SC. When ENx is low, the corresponding output is disabled (output is high impedance), and the PWM input on that phase is ignored. When ENx is high, the output is enabled, and the PWM input controls the state of the output. Refer to Table 1 for the logic truth table.

Table 1: Input Logic Truth Table of MP6543

ENx	PWMx	Sx
H	H	VIN
H	L	GND
L	X	High Impedance

The MP6543A has separate inputs that are used to enable the HS and LS FETs of each phase independently. Refer to Table 2 for the logic truth table.

Table 2: Input Logic Truth Table of MP6543A

HSx	LSx	Sx
L	L	High Impedance
L	H	GND
H	L	VIN
H	H	High Impedance

The MP6543B has three Hall-element inputs, which commutation logic is determined by three Hall-element inputs spaced at 120° . The PWM, DIR, and nBRAKE inputs are used to control motor speed, direction, and brake engagement.

Table 3: Input Logic Truth Table of MP6543B

PWM	nBRAKE	Mode of Operation
0	1	PWM chop mode, and the load current decays
0	0	Brake mode – All low-side gates on
1	1	Selected drivers on
1	0	Brake mode – All low-side gates on

Table 2: Commutation Table of MP6543B (nBRAKE=1)

Logic Inputs				Motor Terminals		
HA	HB	HC	DIR	SA	SB	SC
1	0	1	1	PWM	Z	L
1	0	0	1	Z	PWM	L
1	1	0	1	L	PWM	Z
0	1	0	1	L	Z	PWM
0	1	1	1	Z	L	PWM
0	0	1	1	PWM	L	Z
1	0	1	0	L	Z	PWM
0	0	1	0	L	PWM	Z
0	1	1	0	Z	PWM	L
0	1	0	0	PWM	Z	L
1	1	0	0	PWM	L	Z
1	0	0	0	Z	L	PWM
0	0	0	x	Z	Z	Z
1	1	1	x	Z	Z	Z

Note that the logic inputs have internal weak pulldown resistors.

nSLEEP Operation

Driving nSLEEP low will put the device into a low power sleep state. In this state, all the internal circuits are disabled. All inputs are ignored when nSLEEP is active low. When waking up from sleep mode, some time (approximately 1 ms) needs to pass before the device will respond to inputs. The nSLEEP input has a weak pulldown resistor.

Current Sense Amplifiers

The current flowing in each of the three outputs is sensed by internal current sensing circuits. An output pin for each phase sources or sinks a current that is proportional to the current flowing in each phase. Note that only current flowing in the low-side FET is sensed, and that it is sensed in both the forward and reverse direction.

To convert this current into a voltage (to input to an A/D converter, for example) a termination resistor (R_{TERM}) is used to a reference voltage. When there is no current flowing, the resultant output will be equal to the reference voltage; when current is flowing, the voltage will be above or below the reference voltage according to the following equation:

$$V = V_{TERM} + (R_{TERM} * I_{OUT}) / 4000$$

To terminate the outputs when using an A/D converter with inputs that are ratiometric to its

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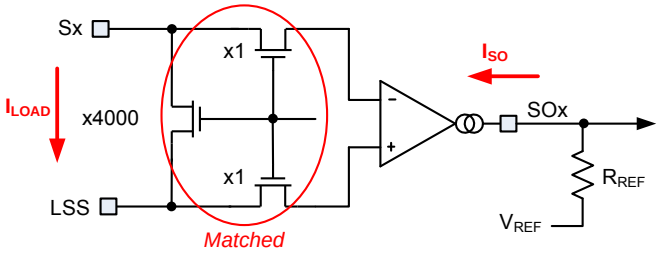
supply voltage, use two equal value resistors to the ADC supply and ground. The resulting ADC code will be half scale at zero current.

The diagram below shows a simplified drawing of the current measurement circuit.



$I_{SO} = I_{LOAD} / 4000$

$V_{SO} = V_{REF} + (I_{SO} * R_{REF})$

$= V_{REF} + ((I_{LOAD} * R_{REF}) / 4000)$

Automatic Synchronous Rectification

When driving current through an inductive load, when the output MOSFETs are both turned off, recirculation current must continue to flow. This current normally is passed through the MOSFET body diodes. To prevent excess power dissipation in the body diodes, the MP6543 implements an automatic synchronous rectification feature.

When both the HS and LS MOSFETSs are turned off, if the voltage on an Sx output pin is driven below ground, the LS MOSFET is turned on until the current flowing through it reaches near zero, or until the HS MOSFET is commanded to turn on. Similarly, if the Sx pin rises above VIN, the HS MOSFET is turned on until the current reaches near zero, or the LS MOSFET is turned on.

nFAULT Output

MP6543 provides an nFAULT output pin which is driven active low in the case of a fault condition, such as overcurrent (OCP) or overtemperature (OTP). This pin is an open-drain output and must be pulled up by an external pullup resistor.

Input UVLO Protection

If at any time the voltage on the VIN pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when VIN rises above the UVLO threshold.

Thermal Shutdown

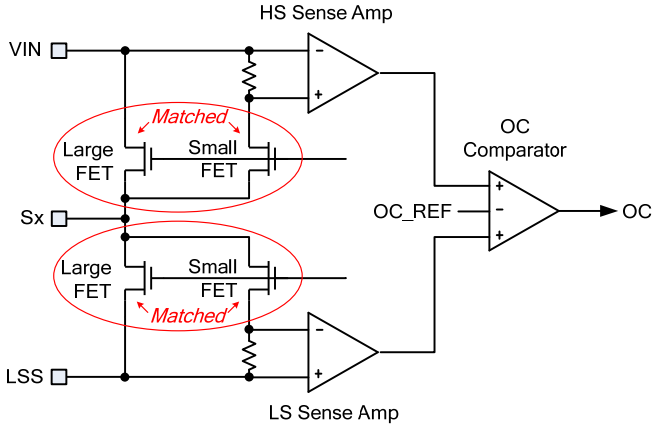
If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

Overcurrent Protection

The overcurrent protection circuit limits the current through each FET by disabling its gate driver. If the overcurrent limit threshold is reached and lasts for longer than the overcurrent deglitch time, all six output FETs will be disabled (outputs become high impedance) and the nFAULT pin will be driven low. During this time current will be recirculated through the body diodes. The outputs will be disabled for 2ms (typ), then are automatically re-enabled.

Over-current conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an over-current shutdown.

A simplified diagram of the OCP circuit for one output is shown below.



OC_ADJ values outside specified value range for Over-Current threshold.

Table 2: Over-Current Threshold

OC_ADJ Resistor Value	Min. OC Threshold
0	5A
30 kΩ	7A
>=64 kΩ or float	No OCP

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3.3V LDO output

An internal LDO regulator generates a 3.3V voltage with 100mA capacity, which could be used to power a small low-power microcontroller. A bypass capacitor of 4.7μF – 10μF is required from the V3P3 pin to ground.

Charge Pump

A charge pump is used to generate the gate drive for the high-side FETs. The charge pump requires one external capacitor: a 1μF ceramic capacitor rated for at least 10V between VIN and VCP.

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TYPICAL APPLICATION CIRCUITS

TBD

Figure 1: Application Circuit Name

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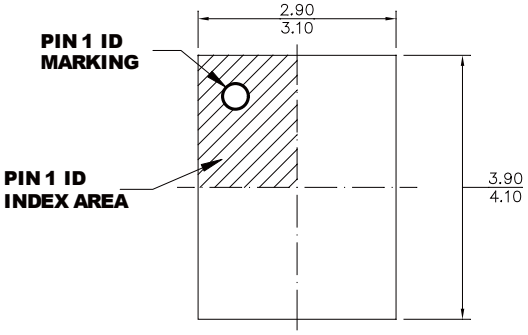
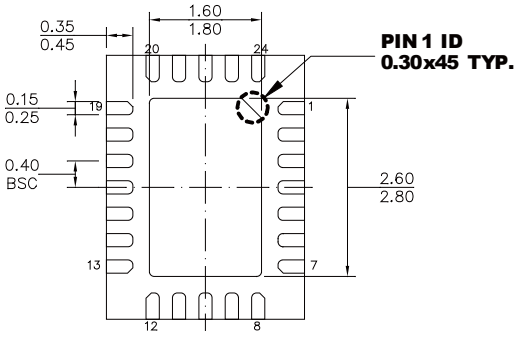
PACKAGE INFORMATION

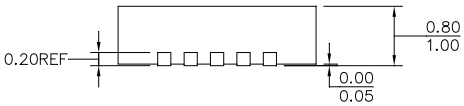
QFN-24 (3mmx4mm)



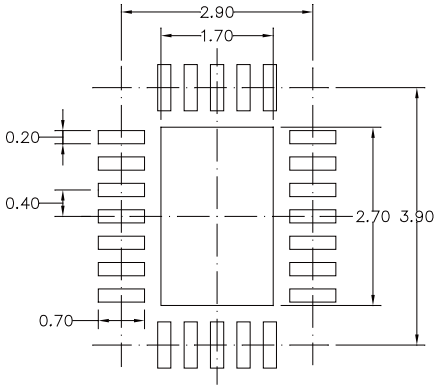
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE

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