MP6910A

CCM/DCM Flyback Ideal Diode with Integrated 100V MOSFET for up to 2.5A Output

DESCRIPTION

The MP6910A is a fast turn-off intelligent rectifier for flyback converters that combines a 100V power switch that replaces diode rectifiers for high efficiency. The chip regulates the forward voltage drop of the internal power switch to about 65mV and turns off before the voltage goes negative.

FEATURES

- Integrated 15mΩ, 100V Power Switch
- Compatible with Energy Star
- VDD Range from 8V to 24V
- 65mV V_{DS} Regulation Function (1)
- Max 250kHz Switching Frequency
- Light-Load Mode Function (1) with <300μA Quiescent Current
- Supports High-Side and Low-Side Rectification
- Power Savings of Up to 1.5W in a Typical Notebook Adapter
- Available in a SOIC8 Package

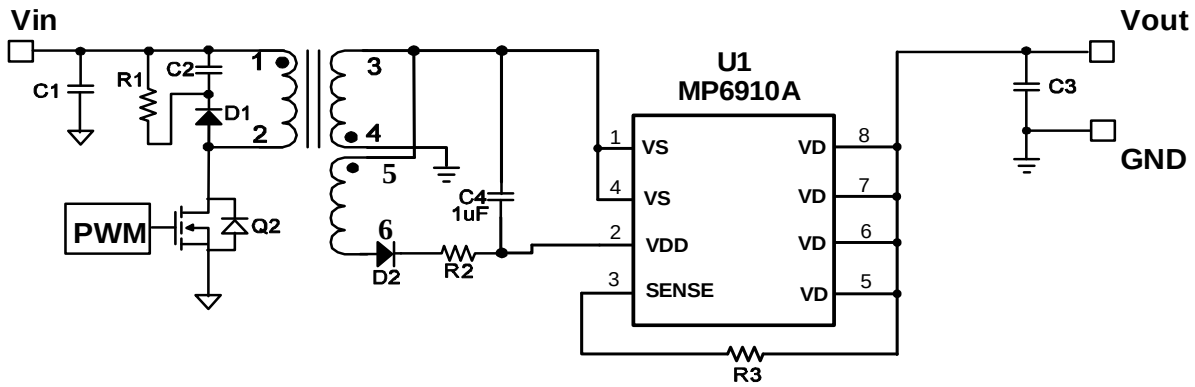
APPLICATIONS

- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems
- Flyback Converters

NOTE:

1) Related issued patent: US Patent US8, 067,973; US8,400,790. CN Patent ZL201010504140.4; ZL200910059751.X. Other patents pending.

TYPICAL APPLICATION

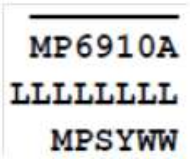


ORDERING INFORMATION

Part Number	Package	Top Marking
MP6910AGS*	SOIC-8	*See Below*

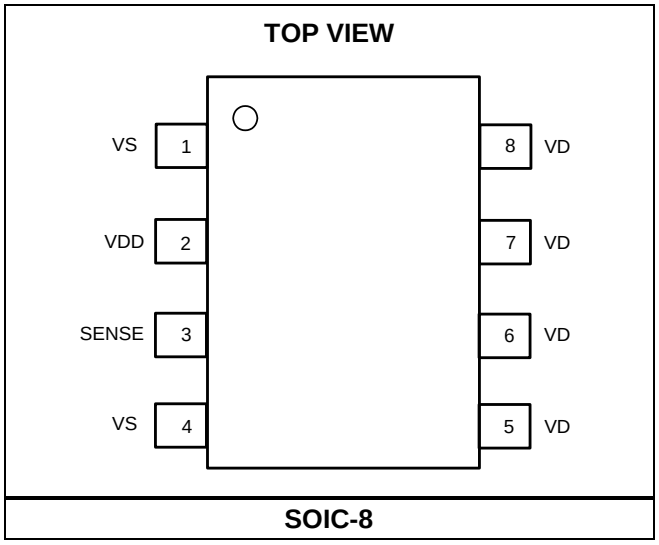
* For Tape & Reel, add suffix –Z (e.g. MP6910AGS–Z)

TOP MARKING



MP6910A: Part code of MP6910AGS
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (2)

VDD to VS ..... -0.3V to +25V
VD to VS..... -0.7V to +100V
SENSE to VS..... -0.7V to +180V
Maximum operating frequency.....250kHz
Continuous drain current (T_C = 25°C) 25A
Continuous drain current (T_C = 100°C) 15A
Maximum power dissipation (3) 2.7W
Junction temperature.....150°C
Lead temperature (solder) .....260°C
Storage temperature .....-55°C to +150°C

Recommended Operation Conditions (4)

VDD to VS ..... 8V to 24V
Operating junction temp. (T_J). ..-40°C to +125°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}	
SOIC-8	67	30	°C/W

NOTES:

2) Exceeding these ratings may damage the device.
3) T_A = +25°C. The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD = 12V, T_J = -40 ~ 125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	$V_{(BR)DSS}$	T_J = 25°C	100			V
VDD UVLO rising			4.8	5.8	6.8	V
VDD UVLO hysteresis			0.7	1	1.3	V
Operating current	I_{CC}	F_{SW} = 100kHz		2.6	4	mA
Light-load mode current				255	350	µA
Control Circuitry Section						
VSS - VD forward voltage	V_{fwd}		45	65	85	mV
Turn-on delay (6)	T_{Don}			100		ns
Turn off threshold (VSS - VD) (7)				30		mV
Turn-off delay (7)	T_{Doff}	VD = VSS		30		ns
Minimum on-time (6)	T_{MIN}			1		µs
Light-load enter delay	$T_{LL-Delay}$		60	110	160	µs
Light-load enter pulse width	T_{LL}		1.4	2.2	3.6	µs
Light-load enter pulse width hysteresis	T_{LL-H}			0.27		µs
Light-load mode exit pulse width threshold (V_{DS})	V_{LL-DS}		-450	-250	-110	mV
Power Switch Section						
Single pulse avalanche energy	E_{AS}	VDD=50V, V_{GS} = 10V, L = 1.0mH, T_J = 25°C		100		mJ
Drain-source on state resistance	$R_{DS(ON)}$	VDD = 12V, I_D = 2A, T_J = 25°C		15	20	mΩ
Input capacitance	C_{iss}	V_{DS} =40V, V_{GS} = 0V, f = 1MHz		1925		pF
Output capacitance	C_{oss}			307		pF
Reverse transfer capacitance	C_{rss}			20		pF
Source-Drain Diode Characteristics						
Source-Drain diode forward voltage	V_{SD}	I_S = 20A, V_{GS} = 0V		0.8	1.2	V
Reverse recovery time	t_{rr}	I_F = 10A, dI/dt = 100A/µs		78.8		ns
Diode reverse change	Q_{rr}			105.6		nC

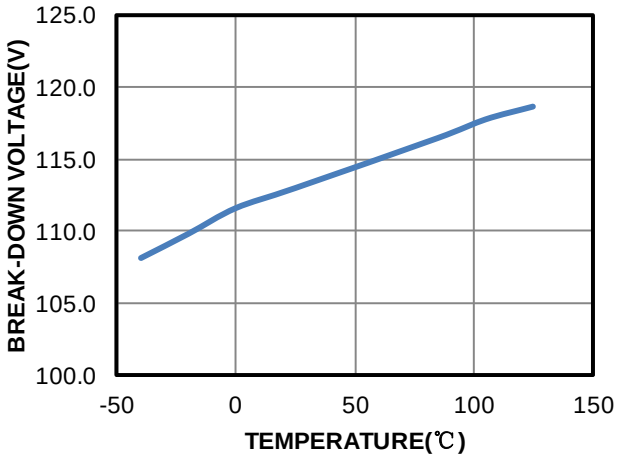
NOTES:

6) Guaranteed by characterization.
7) Guaranteed by design.

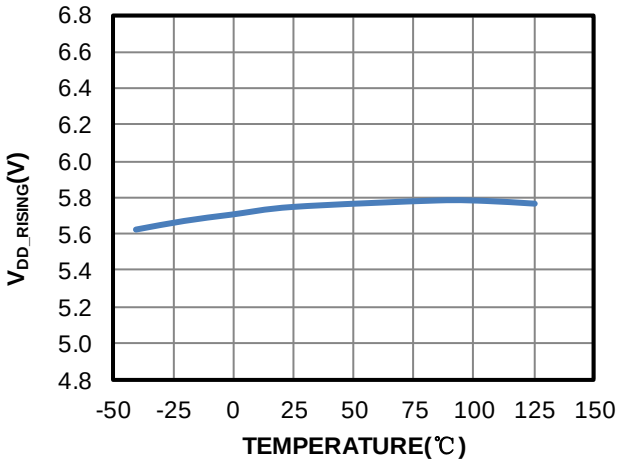
TYPICAL CHARACTERISTICS

VDD = 12V, unless otherwise noted.

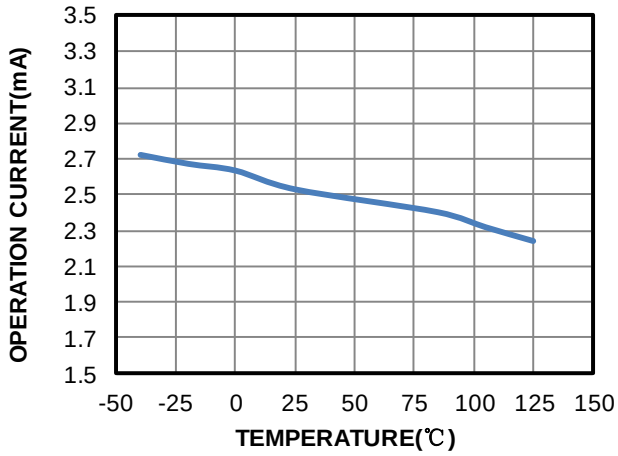
Break-Down Voltage vs. Temperature



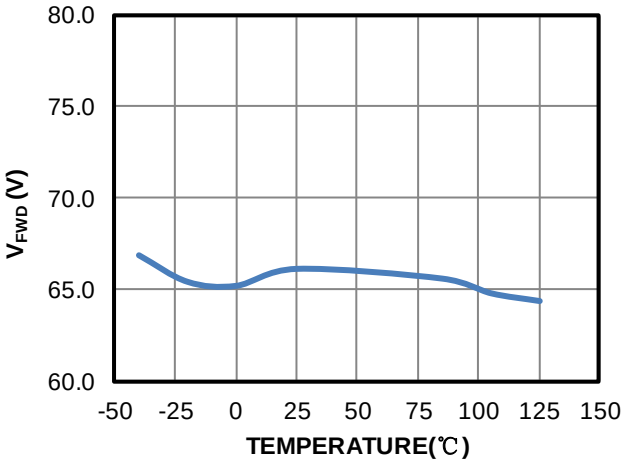
VDD Rising vs. Temperature



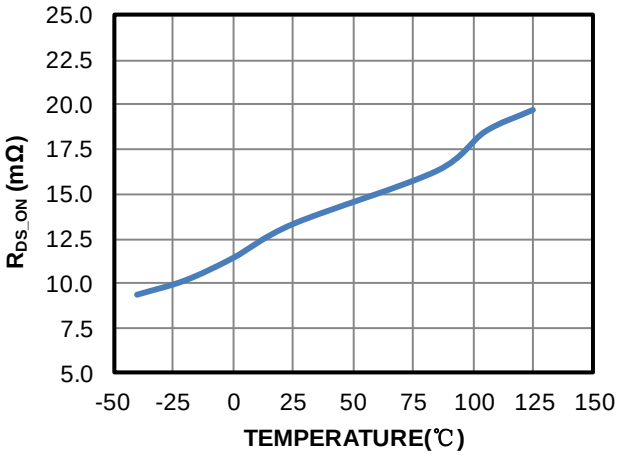
Operation Current vs. Temperature



V_{FWD} vs. Temperature



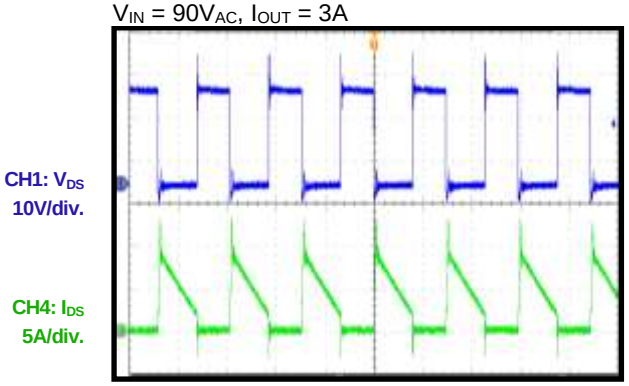
$R_{DS(ON)}$ vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

Operation in 30W Flyback Application

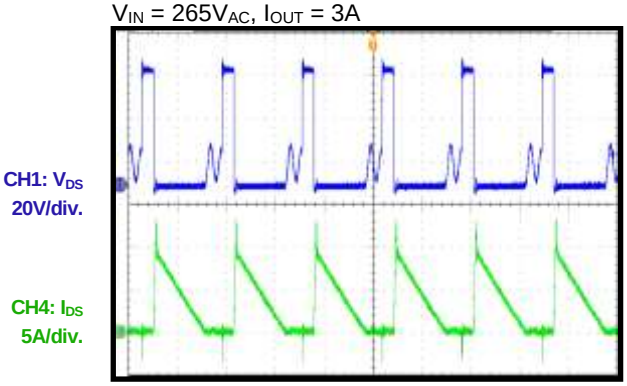
V_{IN} = 90V_{AC}, I_{OUT} = 3A



10µs/div.

Operation in 30W Flyback Application

V_{IN} = 265V_{AC}, I_{OUT} = 3A



10µs/div.

PIN FUNCTIONS

Pin #	Name	Description
1, 4	VS	**MOSFET source.** VS is also used as a reference for VDD.
2	VDD	**Supply voltage.**
3	SENSE	**MOSFET drain voltage sensing.**
5 - 8	VD	**MOSFET drain.**

BLOCK DIAGRAM

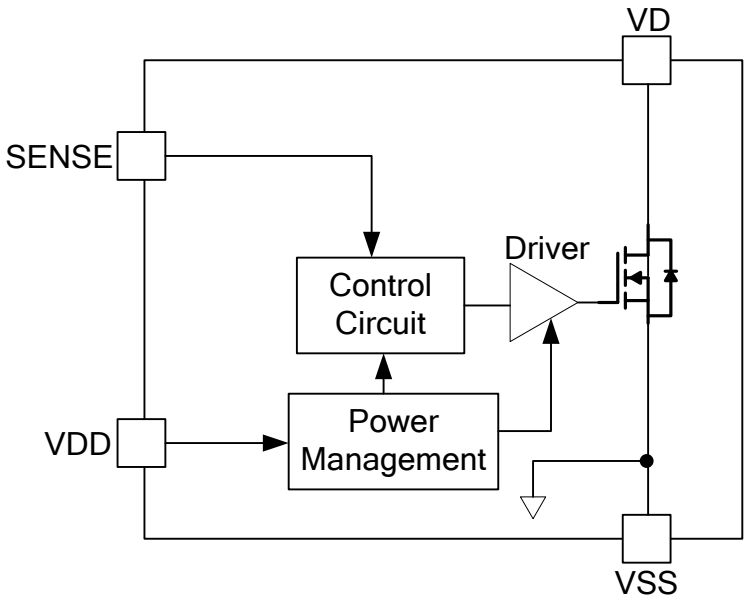


Figure 1: Function Block Diagram

OPERATION

The MP6910A supports operation in flyback converters. The control circuitry controls the gate in forward mode and turns the gate off when the MOSFET current is fairly low.

Blanking

The control circuitry contains a blanking function. When the integrated MOSFET is pulled on or off, the circuitry ensures that the on/off state lasts for a specific amount of time. The turn-on blanking time is ~1.0µs, which determines the minimum on time. During the turn-on blanking period, the turn-off threshold is not blanked completely, but changes the threshold voltage to about +50mV (instead of -30mV). This assures that the MP6910A can always be turned off, even during the turn-on blanking period (albeit it does so slower).

Under-Voltage Lockout (UVLO)

When the VDD is below the under-voltage lockout (UVLO) threshold, the MP6910A is in sleep mode, and the integrated MOSFET is never turned on.

Basic Operation

The basic operations of a flyback converter with the MP6910A are listed below.

1. Turn-On Phase: The switch current first flows through the body diode of the integrate MOSFET, which generates a negative V_{DS} across it (less than -500mV). The voltage is much smaller than the turn-on threshold of the control circuitry (-65mV), which turns on the integrated MOSFET after a 200ns turn-on delay (see Figure 2).

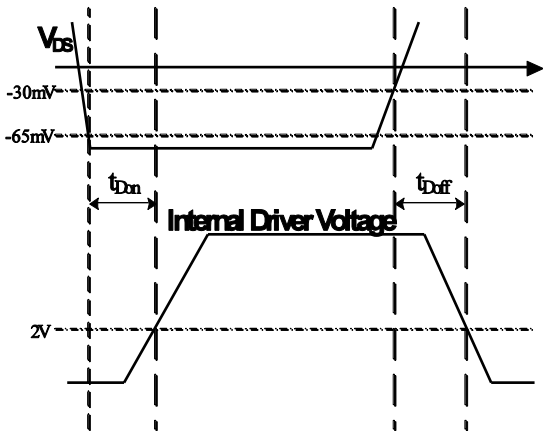


Figure 2: Turn-On and Turn-Off Delay

2. Conducting Phase: When the integrated MOSFET is turned on, V_{DS} starts to rise according to its on resistance. Once V_{DS} rises above the turn-on threshold (-65mV), the control circuitry regulates the gate voltage of the integrated MOSFET to keep V_{DS} around -65mV, even when the current through the switch is fairly small. This function can make the internal driver voltage fairly low when the MOSFET is turned off to quicken the turn-off speed. This function is still active during the turn-on blanking period, which means that the integrated MOSFET can still be turned off even with a very small duty.

   Figure 3 shows the synchronous rectification operation at heavy-load condition. Due to the high current, the internal driver voltage is saturated first. After V_{DS} rises above -65mV, the driver voltage decreases to adjust the V_{DS} to a typical -65mV.

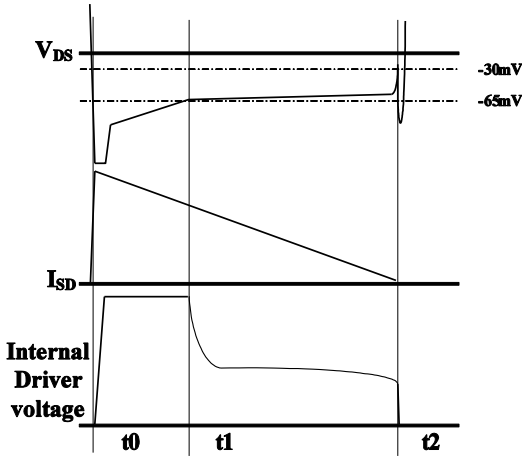


Figure 3: Synchronous Rectification Operation at Heavy Load

   Figure 4 shows the synchronous rectification operation at light-load condition. Due to the low current, the driver voltage never saturates, but begins to decrease once the integrated MOSFET is turned on and adjusts V_{DS}.

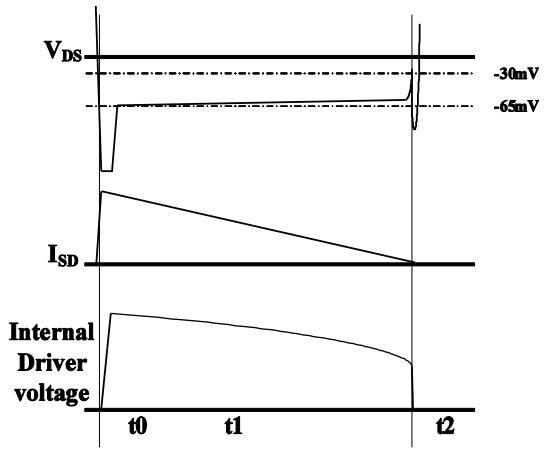


Figure 4: Synchronous Rectification Operation at Light Load

3. Turn-Off Phase: When V_{DS} rises to trigger the turn-off threshold (-30mV), the driver voltage of the switch is pulled low after about 30ns of turn-off delay time by the control circuitry (see Figure 2). Similar with the turn-on phase, a 200ns blanking time is added after the switch is turned off to avoid an erroneous trigger.

Light-Load Latch-Off Function

The gate driver of the integrated MOSFET in the MP6910A is latched to save the driver loss at light-load condition to improve efficiency. The light-load enter pulse width (T_{LL}) is fixed internally (~2.2μs). When the synchronous power switch conducting period is lower than T_{LL} for longer than the light-load enter delay (T_{LL_Delay}), the MP6910A enters light-load mode and latches off the integrated MOSFET (see Figure 5).

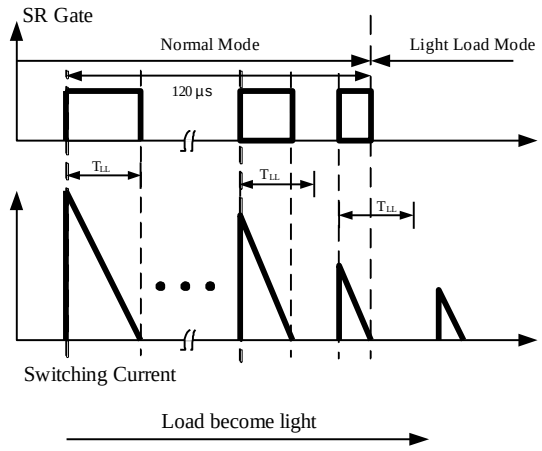


Figure 5: Enter Light Load Mode

During light-load mode, the MP6910A monitors the integrated MOSFET body diode conducting period by sensing V_{DS}. When V_{DS} exceeds the light-load mode exit pulse width threshold (V_{LL_DS}), the MP6910A considers the integrated MOSFET body diode conducting time to be completed. If the MOSFET body diode conduction time is longer than T_{LL} + T_{LL_H} (T_{LL_H}, light-load-enter pulse width hysteresis), the light-load mode is finished and the integrated MOSFET of the MP6910A is unlatched to restart synchronous rectification (see Figure 6).

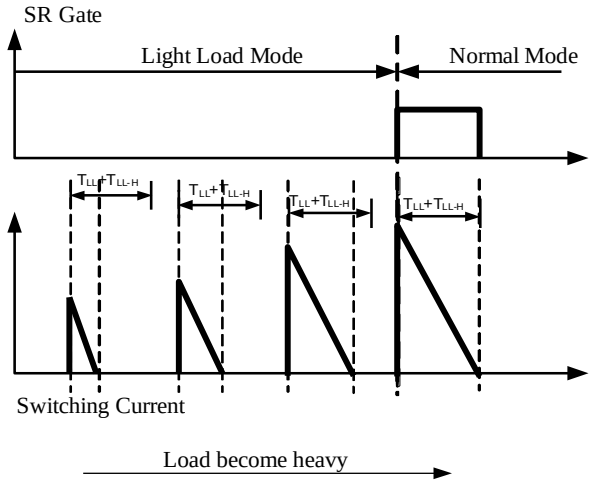


Figure 6: Exit Light Load Mode

Typical System Implementations

Figure 7 shows the typical system implementation for the IC supply derived from the output voltage, which is available in low-side rectification. The output voltage is recommended to be in the VDD range (from 8V to 24V).

If the output voltage is out of the VDD range or high-side rectification is used, it is recommended to use an auxiliary winding from the power transformer for the IC supply (see Figure 8 and Figure 9).

There is another non-auxiliary winding solution for the IC supply, which uses an external LDO circuit from the secondary transformer winding (see Figure 10 and Figure 11). Compared with an auxiliary winding for the IC supply, this solution has a slightly higher power loss, which is dissipated on the LDO circuit, especially when the secondary winding voltage is high.

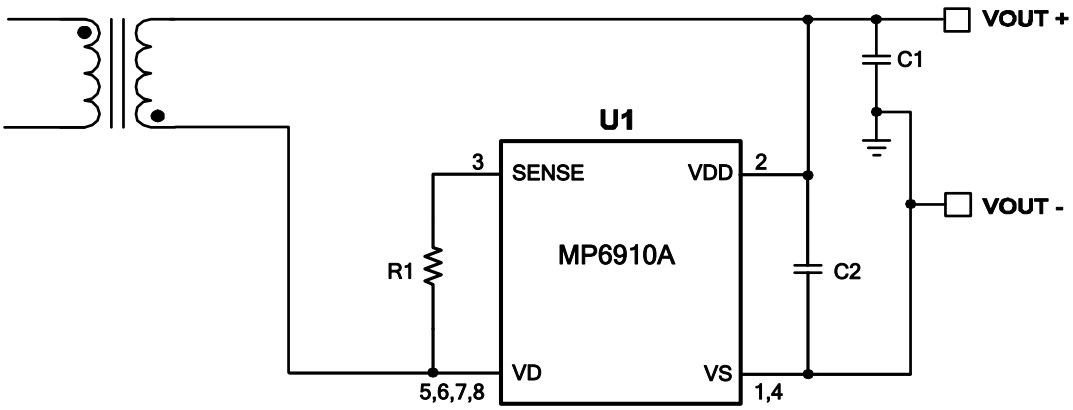


Figure 7: IC Supply Derived Directly from Output Voltage

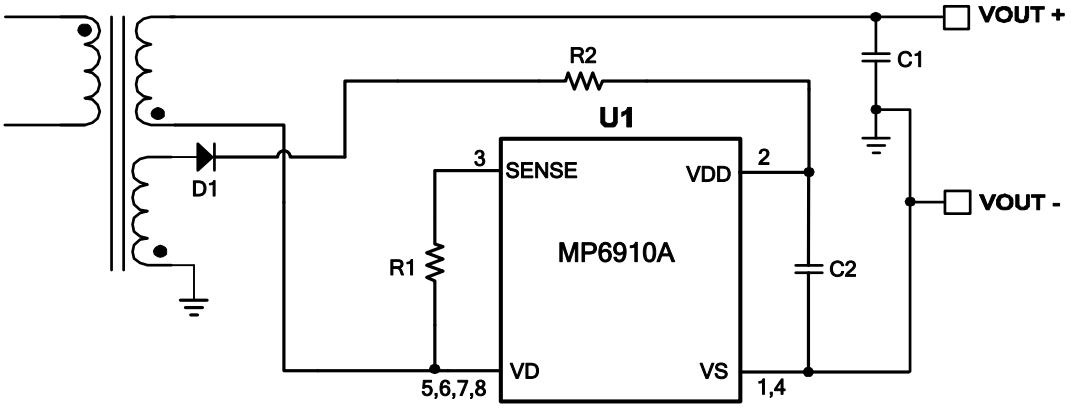


Figure 8: IC Supply Derived from Auxiliary Winding in Low-Side Rectification

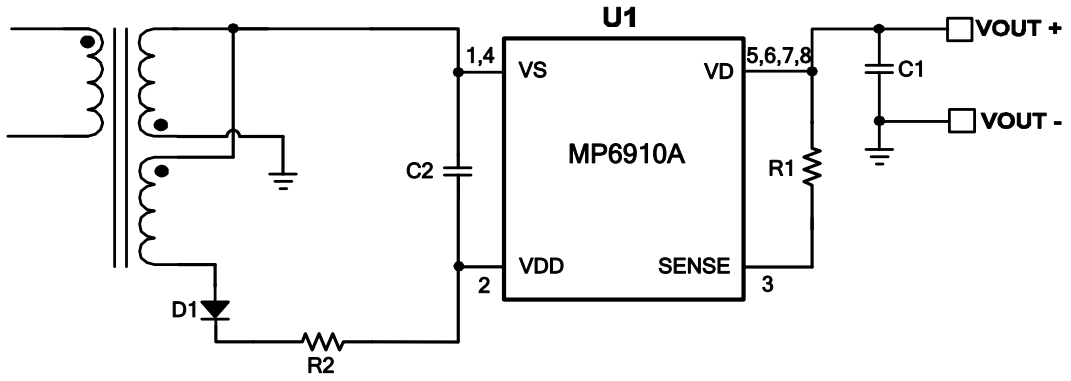


Figure 9: IC Supply Derived from Auxiliary Winding in High-Side Rectification

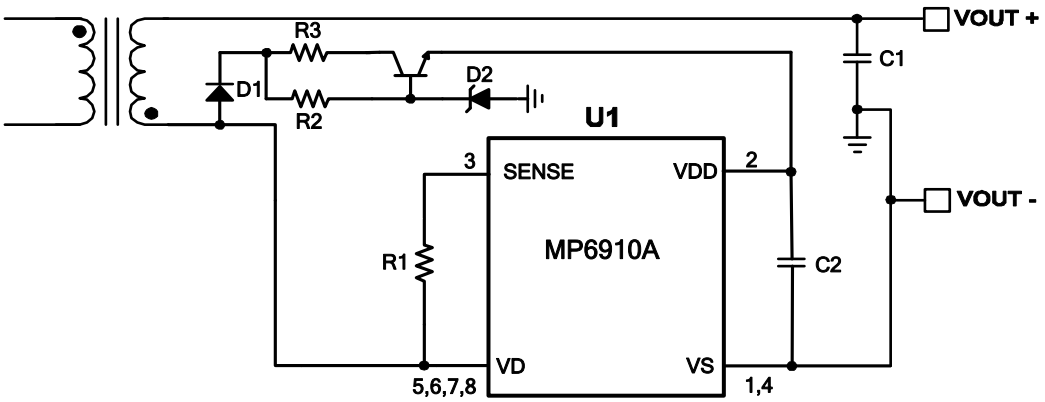


Figure 10: IC Supply Derived from Secondary Winding in Low-Side Rectification

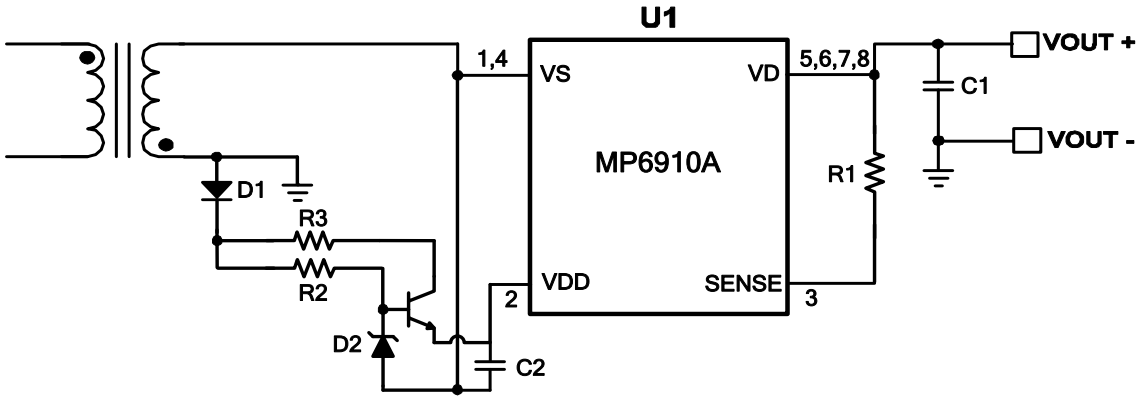
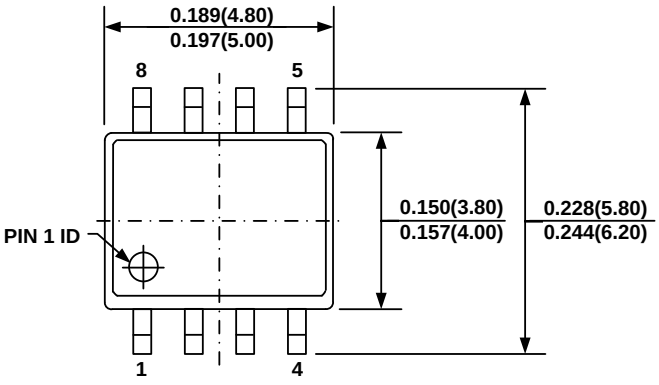


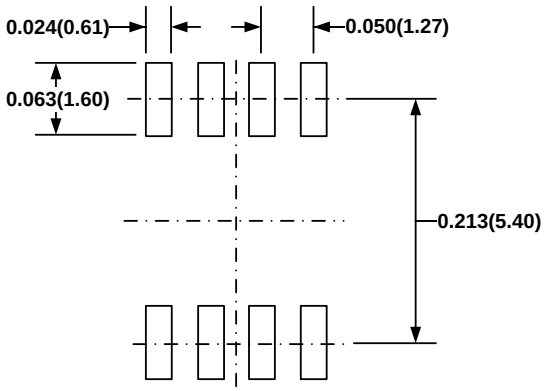
Figure 11: IC Supply Derived from Secondary Winding in High-Side Rectification

PACKAGE INFORMATION

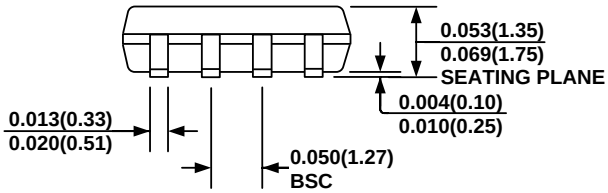
SOIC-8



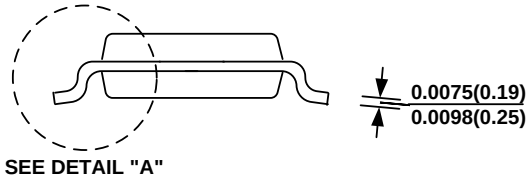
TOP VIEW



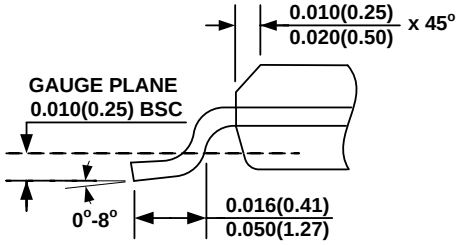
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.